Intel Atom® x6000E Series, and Intel® Pentium® and Celeron® N and J Series Processors for IoT Applications

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Platform Controller Hub (PCH)

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Revision Date	Revision Number	Description
February 2023	003	• Chapter 2, "Enhanced Serial Peripheral Interface (eSPI) Controller" — Section 2.1.29 - Updated bit range, default & access and field description, Manufacturer's ID (ESPI_MANID) - Offset F8h. • Chapter 5, "Converged Audio, Voice, Speech (cAVS) Controller" — Section 5.1.41 - Updated bit range, default & access and field description, Manufacturing Process (MANID) - Offset F8h • Chapter 6, "System Management Bus (SMBus) Controller" — Section 6.1.25 - Updated bit range, default & access and field description, Manufacturer's ID (MANID) - Offset F8h • Chapter 7, "Serial Peripheral Interface (SPI) Controller" — Section 7.1.10 - Updated bit range, default & access and field description, Manufacturer's ID (BIOS_SPI_MANID) - Offset F8h • Chapter 10, "TSN GbE Controller" — Section 10.2.52 - Updated field description on Bit16, MAC_GPIO_STATUS — Offset 20Ch • Chapter 13, "Secure Digital I/O (SDIO) Controller" — Section 13.3.7 - Added new table — Section 13.3.8 - Added new table — Section 13.3.9 - Added new table — Section 13.3.11 - Added new table • Chapter 16, "Host Embedded Controller Interface (HECI)" — Section 16.1.40 - Updated field description on Bit16, MAC_GPIO_STATUS — Offset 20Ch • Chapter 31, "ModPHY Configuration" — New chapter
August 2021	002	• Chapter 4, "Power Management Controller (PMC)" — Section 4.3.14 - Updated field description on Bit7, General Purpose Event 0 Status [127:96] (GPE0_STS_127_96) — Offset 6Ch. — Section 4.3.14 - Updated field description on Bit19, General Purpose Event 0 Status [127:96] (GPE0_STS_127_96) — Offset 6Ch. — Section 4.3.18 - Updated field description on Bit19, General Purpose Event 0 Enable [127:96] (GPE0_EN_127_96) — Offset 7Ch.
July 2021	001	Initial release.

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1 Introduction

The Intel Atom® x6000E series, Pentium® N and J series, and Celeron® N and J series processor is targeted towards various IoT segments, such as industrial, retail, and embedded. It features real time compute with technologies such as TSN, TCC, which are expected to drive the future of IoT.

Intel Atom® x6000E series, Pentium® N and J series, and Celeron® N and J series processor is an Intel Architecture (IA) Multi-Chip Processor (MCP) 2-Chip Package, built on a 10-nanometer Compute Die and a 14-nanometer Platform Controller Hub (PCH) into a single package. Both dies are connected via the On Package Interface (OPI).

1.1 About this Manual

This document is intended for Original Equipment Manufacturers (OEMs), Original Design Manufacturers (ODM) and BIOS vendors creating products based on the Elkhart Lake family Multi Chip Package (MCP).

Throughout this document, the name "Processor" is used as a general term and refers to all Elkhart Lake family SKUs, unless specifically noted otherwise. The compute die may be referred to simply as "Compute Die" and the Platform Controller Hub may be referred to simply as "PCH".

This manual assumes a working knowledge of the vocabulary and principles of interfaces and architectures such as PCI express* (PCIe*), Universal Serial Bus (USB), Advanced Host Controller Interface (AHCI), eXtensible Host Controller Interface (xHCI), and so forth.

This manual abbreviates PCI buses as Bn, devices as Dn and functions as Fn. For example, Device 31 Function 0 is abbreviated as D31:F0, and Bus 1 Device 8 Function 0 is abbreviated as B1:D8:F0. Generally, the bus number will not be used, and can be considered to be Bus 0. These numbers are shown as decimal unless otherwise indicated.

This is the core reference document for external design specifications. Information provided here takes precedence, if there are any discrepancies found in related documents.

1.2 References

Specification	Document #/Location
Intel Atom® x6000E Series, and Intel® Pentium® and Celeron® N and J Series Processors for IoT Applications Datasheet Volume 1	636112
Intel Atom® x6000E Series, and Intel® Pentium® and Celeron® N and J Series Processors for Internet of Things (IoT) Applications, Datasheet, Volume 2 (Book 1 of 3)	635255
Intel Atom® x6000E Series, and Intel® Pentium® and Celeron® N and J Series Processors for Internet of Things (IoT) Applications, Datasheet, Volume 2 (Book 3 of 3)	636723

2 Enhanced Serial Peripheral Interface (eSPI) Controller

2.1 eSPI Configuration Registers Summary

This chapter documents the registers in Bus: 0, Device 31, Function 0.

Summary of Bus: 0, Device: 31, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device and Vendor Identifiers (ESPI_DID_VID)	4B008086h
4h	4	Device Status and Command (ESPI_STS_CMD)	00000403h
6h	2	Primary Status (STS)	0200h
8h	4	Class Code and Revision ID (ESPI_CC_RID)	06010000h
Ch	4	Peripheral Channel Header Type and Primary Latency (ESPI_PCHT_PCPLT)	00800000h
Dh	1	Primary Latency Timer (PLT)	00h
Eh	1	Header Type (HTYPE)	80h
2Ch	4	Sub System Identifiers (ESPI_SS)	00000000h
34h	4	Capability List Pointer (ESPI_CAPP)	00000000h
64h	4	Peripheral Channel Serial IRQ Control (ESPI_PCSERIRQC)	00000000h
80h	4	I/O Decode Ranges and I/O Enables (ESPI_IOD_IOE)	00000000h
82h	2	I/O Enables (IOE)	0000h
84h	4	LPC Generic IO Range 1 (ESPI_LGIR1)	00000000h
88h	4	LPC Generic IO Range 2 (ESPI_LGIR2)	00000000h
8Ch	4	LPC Generic IO Range 3 (ESPI_LGIR3)	00000000h
90h	4	LPC Generic IO Range 4 (ESPI_LGIR4)	00000000h
94h	4	USB Legacy Keyboard/Mouse Control (ESPI_ULKMC)	00000000h
98h	4	LPC Generic Memory Range (ESPI_LGMR)	00000000h
A0h	4	eSPI CS1 IO Routing Enables (ESPI_CS1IORE)	00000000h
A4h	4	eSPI CS1 Generic IO Range 1 (ESPI_CS1GIR1)	00000000h
A8h	4	eSPI CS1 Generic Memory Range 1 (ESPI_CS1GMR1)	00000000h
D0h	4	FWH ID Select 1 (ESPI_PCFS1)	00000000h
D4h	4	FWH ID Select 2 (ESPI_PCFS2)	00000000h
D8h	4	BIOS Decode Enable (ESPI_BDE)	0000FFCFh
DCh	4	BIOS Control (ESPI_BC)	00000020h
E0h	4	PCI Clock Control (PCCTL)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
F0h	4	Unsupported Request Error Status (URES)	00000000h
F4h	4	Unsupported Request Error Control (UREC)	00000000h
F8h	4	Manufacturer's ID (ESPI_MANID)	00000F00h

2.1.1 Device and Vendor Identifiers (ESPI_DID_VID) - Offset 0h

Various Identifiers.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + 0h	4B008086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4B00h RO/V	**Device Identification (DID):** The default value of this is hardwired. The upper 9-bits of this field can be overridden by the SetID IOSF-SB Message.
15:0	8086h RO	**Vendor Identification (VID):** Indicates Intel

2.1.2 Device Status and Command (ESPI_STS_CMD) - Offset 4h

Device Status and Command.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + 4h	00000403h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the bridge detects a parity error on the internal backbone. This bit gets set even if CMD.PERE is not set.
30	0h RW/1C/V	**Signaled System Error (SSE):** Set when the LPC bridge signals a system error to the internal SERR# logic.
29	0h RW/1C/V	**Received Master Abort (RMA):** Set when the bridge receives a completion with unsupported request status from the backbone.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the bridge receives a completion with completer abort status from the backbone.
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set when the bridge generates a completion packet with target abort status on the backbone.
26:25	0h RO	**DEVSEL# Timing Status (DTS):** Indicates medium timing, although this has no meaning on the backbone.

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW/1C/V	**Data Parity Error Detected (DPD):** Set when the bridge receives a completion packet from the backbone from a previous request, and detects a parity error, and CMD.PERE is set.
23	0h RO	**Fast Back to Back Capable (FBC):** Reserved
22	0h RO	**Reserved**
21	0h RO	**66 MHz Capable (C66):** Reserved
20	0h RO	**Capabilities List (CLIST):** There is a capabilities list in the LPC bridge.
19	0h RO	**Interrupt Status (INTS):** The LPC bridge does not generate interrupts.
18:11	0h RO	**Reserved**
10	1h RO	**Interrupt Disable (INTD):** The LPC bridge has no interrupts to disable
9	0h RO	**Fast Back to Back Enable (FBE):** Reserved
8	0h RW	**SERR# Enable (SEE):** The LPC bridge generates SERR# if this bit is set.
7	0h RO	**Wait Cycle Control (WCC):** Reserved
6	0h RW	**Parity Error Response Enable (PERE):** When this bit is set to 1, it enables the LPC bridge to response to parity errors detected on backbone interface.
5	0h RO	**VGA Palette Snoop (VGA_PSE):** Reserved
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** Reserved
3	0h RO	**Special Cycle Enable (SCE):** Reserved
2	0h RW	**Bus Master Enable (BME):** Controls a device's ability to act as a master on the bus. A value of 0 disables the device from generating traffic. A value of 1 allows the device to behave as a bus master. State after RST# is 0.
1	1h RO	**Memory Space Enable (MSE):** Memory space cannot be disabled on LPC.
0	1h RO	**I/O Space Enable (IOSE):** I/O space cannot be disabled on LPC.

2.1.3 Primary Status (STS) - Offset 6h

Status.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:0] + 6h	0200h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**Detected Parity Error (DPE):** Set when the bridge detects a parity error on the internal backbone. This bit gets set even if CMD.PERE is not set.
14	0h RW/1C	**Signaled System Error (SSE):** Set when the LPC bridge signals a system error to the internal SERR# logic.
13	0h RO	**Received Master Abort (RMA):** Set when the bridge receives a completion with unsupported request status from the backbone. LPC is a target only controller.
12	0h RO	**Received Target Abort (RTA):** Set when the bridge receives a completion with completer abort status from the backbone. LPC is a target only controller.
11	0h RW/1C	**Signalled Target Abort (STA):** Set when the bridge generates a completion packet with target abort status on the backbone.
10:9	1h RO	**DEVSEL# Timing Status (DTS):** Indicates medium timing, although this has no meaning on the backbone.
8	0h RW/1C	**Data Parity Error Detected (DPD):** Set when the bridge receives a completion packet from the backbone from a previous request, and detects a parity error, and CMD.PERE is set.
7	0h RO	**Fast Back to Back Capable (FBC):** Reserved
6	0h RO	**Reserved**
5	0h RO	**66 MHz Capable (C66):** Reserved
4	0h RO	**Capabilities List (CLIST):** There is a capabilities list in the LPC bridge.
3	0h RO	**Interrupt Status (INTRSTS):** The LPC bridge does not generate interrupts.
2:0	0h RO	**Reserved**

2.1.4 Class Code and Revision ID (ESPI_CC_RID) - Offset 8h

Writing to this register controls what is reported in all of the RID registers in the component. The value written does not get directly loaded in this register. However, the value is checked to determine which value to report.

Once written, additional writes to this register must not have any effect until a core-well reset occurs. BIOS must always write to this register in order to guarantee that the functionality is locked.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + 8h	06010000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	06h RO	**Base Class Code (BCC):** Indicates the device is a bridge device.
23:16	01h RO	**Sub-Class Code (SCC):** Indicates the device a PCI to ISA bridge.
15:8	00h RO	**Programming Interface (PI):** The LPC bridge has no programming interface.
7:0	00h RO/V	**Revision ID (RID):** Indicates the part revision This will reset to 0 but is expected to be overridden by the SetID IOSF-SB message.

2.1.5 Peripheral Channel Header Type and Primary Latency (ESPI_PCHT_PCPLT) - Offset Ch

Peripheral Channel Header Type and Primary Latency.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + Ch	00800000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	1h RO	**Multi-function Device (MFD):** This bit is 1 to indicate that this PCI function is part of a multi-function device.
22:16	00h RO	**Header Type (HTYPE):** Identifies the header layout of the configuration space, which is a generic device.
15:11	00h RO	**Master Latency Count (MLC):** Reserved
10:0	0h RO	**Reserved**

2.1.6 Primary Latency Timer (PLT) - Offset Dh

Primary Latency Timer.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:31, F:0] + Dh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:3	00h RO	**Master Latency Count (MLC):** Reserved
2:0	0h RO	**Reserved**

2.1.7 Header Type (HTYPE) - Offset Eh

Header Type.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:31, F:0] + Eh	80h

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Multi-function Device (MFD):** This bit is 1 to indicate a multifunction device.
6:0	00h RO	**Header Type (HTYPE):** Identifies the header layout of the configuration space, which is a generic device.

2.1.8 Sub System Identifiers (ESPI_SS) - Offset 2Ch

This register is initialized to logic 0 by the assertion of PLTRST#. This register can be written only once after PLTRST# de-assertion.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken on this value.
15:0	0000h RW/O	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action taken on this value.

2.1.9 Capability List Pointer (ESPI_CAPP) - Offset 34h

Capability List Pointer.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + 34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Capability Pointer (CP):** Indicates the offset of the first Capability Item.

2.1.10 Peripheral Channel Serial IRQ Control (ESPI_PCSERIRQC) - Offset 64h

Peripheral Channel Serial IRQ Control.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + 64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

2.1.11 I/O Decode Ranges and I/O Enables (ESPI_IOD_IOE) - Offset 80h

I/O Decode Ranges and I/O Enables.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + 80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW	**Microcontroller Enable #2 (ME2):** Enables decoding of I/O locations 4Eh and 4Fh to LPC.
28	0h RW	**SuperI/O Enable (SE):** Enables decoding of I/O locations 2Eh and 2Fh to LPC.
27	0h RW	**Microcontroller Enable #1 (ME1):** Enables decoding of I/O locations 62h and 66h to LPC.
26	0h RW	**Keyboard Enable (KE):** Enables decoding of the keyboard I/O locations 60h and 64h to LPC.
25	0h RW	**High Gameport Enable (HGE):** Enables decoding of the I/O locations 208h to 20Fh to LPC.
24	0h RW	**Low Gameport Enable (LGE):** Enables decoding of the I/O locations 200h to 207h to LPC.

Bit Range	Default & Access	Field Name (ID): Description
23:20	0h RO	**Reserved**
19	0h RW	**Floppy Drive Enable (FDE):** Enables decoding of the FDD range to LPC. Range is selected by LIOD.FDE
18	0h RW	**Parallel Port Enable (PPE):** Enables decoding of the LPT range to LPC. Range is selected by LIOD.LPT.
17	0h RW	**Com Port B Enable (CBE):** Enables decoding of the COMB range to LPC. Range is selected LIOD.CB.
16	0h RW	**Com Port A Enable (CAE):** Enables decoding of the COMA range to LPC. Range is selected LIOD.CA.
15:13	0h RO	**Reserved**
12	0h RW	**FDD Range (FDD):** The following table describes which range to decode for the FDD Port Bits Decode Range 0 3F0h - 3F5h, 3F7h (Primary) 1 370h - 375h, 377h (Secondary)
11:10	0h RO	**Reserved**
9:8	0h RW	**LPT Range (LPT):** The following table describes which range to decode for the LPT Port: Bits Decode Range 00 378h - 37Fh and 778h - 77Fh 01 278h - 27Fh (port 279h is read only) and 678h - 67Fh 10 3BCh - 3BEh and 7BCh - 7BEh 11 Reserved
7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6:4	0h RW	**ComB Range (CB):** The following table describes which range to decode for the COMB Port Bits Decode Range 000 3F8h - 3FFh (COM 1) 001 2F8h - 2FFh (COM 2) 010 220h - 227h 011 228h - 22Fh 100 238h - 23Fh 101 2E8h - 2EFh (COM 4) 110 338h - 33Fh 111 3E8h - 3EFh (COM 3)
3	0h RO	**Reserved**
2:0	0h RW	**ComA Range (CA):** The following table describes which range to decode for the COMA Port Bits Decode Range 000 3F8h - 3FFh (COM 1) 001 2F8h - 2FFh (COM 2) 010 220h - 227h 011 228h - 22Fh 100 238h - 23Fh 101 2E8h - 2EFh (COM 4) 110 338h - 33Fh 111 3E8h - 3EFh (COM 3)

2.1.12 I/O Enables (IOE) - Offset 82h

I/O Enables.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:0] + 82h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Reserved**
13	0h RW	**Microcontroller Enable #2 (ME2):** Enables decoding of I/O locations 4Eh and 4Fh to LPC.
12	0h RW	**SuperI/O Enable (SE):** Enables decoding of I/O locations 2Eh and 2Fh to LPC.
11	0h RW	**Microcontroller Enable #1 (ME1):** Enables decoding of I/O locations 62h and 66h to LPC.
10	0h RW	**Keyboard Enable (KE):** Enables decoding of the keyboard I/O locations 60h and 64h to LPC.
9	0h RW	**High Gameport Enable (HGE):** Enables decoding of the I/O locations 208h to 20Fh to LPC.
8	0h RW	**Low Gameport Enable (LGE):** Enables decoding of the I/O locations 200h to 207h to LPC.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**Reserved**
3	0h RW	**Floppy Drive Enable (FDE):** Enables decoding of the FDD range to LPC. Range is selected by LIOD.FDE
2	0h RW	**Parallel Port Enable (PPE):** Enables decoding of the LPT range to LPC. Range is selected by LIOD.LPT.
1	0h RW	**Com Port B Enable (CBE):** Enables decoding of the COMB range to LPC. Range is selected LIOD.CB.
0	0h RW	**Com Port A Enable (CAE):** Enables decoding of the COMA range to LPC. Range is selected LIOD.CA.

2.1.13 LPC Generic IO Range 1 (ESPI_LGIR1) - Offset 84h

LPC Generic IO Range 1.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + 84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:18	00h RW	**Address[7:2] Mask (ADDR_MASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	0h RO	**Reserved**
15:2	0000h RW	**ADDR:** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
1	0h RO	**Reserved**
0	0h RW	**LPC Decode Enable (LDE):** When this bit is set to 1, then the range specified in this register is enabled for decoding to LPC.

2.1.14 LPC Generic IO Range 2 (ESPI_LGIR2) - Offset 88h

LPC Generic IO Range 2.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + 88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:18	00h RW	**Address[7:2] Mask (ADDR_MASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	0h RO	**Reserved**
15:2	0000h RW	**ADDR:** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
1	0h RO	**Reserved**
0	0h RW	**LPC Decode Enable (LDE):** When this bit is set to 1, then the range specified in this register is enabled for decoding to LPC.

2.1.15 LPC Generic IO Range 3 (ESPI_LGIR3) - Offset 8Ch

LPC Generic IO Range 3.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + 8Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:18	00h RW	**Address[7:2] Mask (ADDR_MASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	0h RO	**Reserved**
15:2	0000h RW	**ADDR:** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
1	0h RO	**Reserved**
0	0h RW	**LPC Decode Enable (LDE):** When this bit is set to 1, then the range specified in this register is enabled for decoding to LPC.

2.1.16 LPC Generic IO Range 4 (ESPI_LGIR4) - Offset 90h

LPC Generic IO Range 4.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + 90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:18	00h RW	**Address[7:2] Mask (ADDR_MASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	0h RO	**Reserved**
15:2	0000h RW	**ADDR:** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
1	0h RO	**Reserved**
0	0h RW	**LPC Decode Enable (LDE):** When this bit is set to 1, then the range specified in this register is enabled for decoding to LPC.

2.1.17 USB Legacy Keyboard/Mouse Control (ESPI_ULKMC) - Offset 94h

USB Legacy Keyboard/Mouse Control.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + 94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/V	**SMI Caused by End of Pass-through (SMIBYENDPS):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 7, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
14:12	0h RO	**Reserved**
11	0h RW/1C/V	**SMI Caused by Port 64 Write (TRAPBY64W):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 3, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch. Note that the A20Gate Pass-Through Logic allows specific port 64h Writes to complete without setting this bit.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/1C/V	**SMI Caused by Port 64 Read (TRAPBY64R):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 2, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
9	0h RW/1C/V	**SMI Caused by Port 60 Write (TRAPBY60W):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 1, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch. Note that the A20Gate Pass-Through Logic allows specific port 60h Writes to complete without setting this bit.
8	0h RW/1C/V	**SMI Caused by Port 60 Read (TRAPBY60R):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 0, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
7	0h RW	**SMI at End of Pass-through Enable (SMIATENDPS):** May need to cause SMI at the end of a pass-through. Can occur if an SMI is generated in the middle of a pass through, and needs to be serviced later.
6	0h RO/V	**Pass Through State (PSTATE):** This read-only bit indicates that the state machine is in the middle of an A20GATE pass-through sequence. If software needs to reset this bit, it should set Bit 5 0.
5	0h RW	**A20Gate Pass-Through Enable (A20PASSEN):** When enabled, allows A20GATE sequence Pass-Through function. When enabled, a specific cycle sequence involving writes to port 60h and port 64h do not result in the setting of the SMI status bits.SMI# will not be generated, even if the various enable bits are set.
4	0h RO	**Reserved**
3	0h RW	**SMI on Port 64 Writes Enable (S64WEN):** When set, a 1 in bit 11 will cause an SMI event.
2	0h RW	**SMI on Port 64 Reads Enable (S64REN):** When set, a 1 in bit 10 will cause an SMI event.
1	0h RW	**SMI on Port 60 Writes Enable (S60WEN):** When set, a 1 in bit 9 will cause an SMI event.
0	0h RW	**SMI on Port 60 Reads Enable (S60REN):** When set, a 1 in bit 8 will cause an SMI event.

2.1.18 LPC Generic Memory Range (ESPI_LGMR) - Offset 98h

LPC Generic Memory Range.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Memory Address[31:16] (MADDR):** This field specifies a 64KB memory block anywhere in the 4GB memory space that will be decoded to LPC as standard LPC Memory Cycle if enabled.
15:1	0h RO	**Reserved**
0	0h RW	**LPC Memory Range Decode Enable (LGMRD_EN):** When this bit is set to 1, then the range specified in this register is enabled for decoding to LPC.

2.1.19 eSPI CS1 IO Routing Enables (ESPI_CS1IORE) - Offset A0h

Note: This register is used to route fixed I/O transactions from the Host to the second Slave device (CS1#) over the Peripheral Channel on the eSPI bus.

Register Lock: This register is locked in a single Slave configuration (soft-strap espi_cs1_en = 0b). All writes to this register must be dropped and reads to this register must return the default (reset) values.

Implementation / Usage Note: PCIODE enables a given range if that is zero, all accesses to that range are U/R'd, irrespective of the settings for that range in this register. So PCIODE should be set/checked first. If a given range is enabled in PCIODE, then this register (PCCS1IORE) is used to select which eSPI Slave device to route the transactions to. When a second eSPI Slave device is not present, then PCCS1IORE is ignored and all IO transactions targeted to any range enabled in PCIODE are routed to CS0#.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14	0h RW/V	**Debug Port CS1# Routing Enable (DPRE):** Enables routing of I/O locations 80h, 84h-86h, 88h, 8Ch-8Eh, 90h, 94h-96h, 98h, 9Ch-9Eh to eSPI CS1#. This field is only writeable if the eSPI CS1 is enabled and is RO when eSPI CS1 is disabled.
13	0h RW/V	**Microcontroller #2 CS1# Routing Enable (MRE2):** Enables routing of I/O locations 4Eh and 4Fh to eSPI CS1#. This field is only writeable if the eSPI CS1 is enabled and is RO when eSPI CS1 is disabled.
12	0h RW/V	**SuperI/O CS1# Routing Enable (SRE):** Enables routing of I/O locations 2Eh and 2Fh to eSPI CS1#. This field is only writeable if the eSPI CS1 is enabled and is RO when eSPI CS1 is disabled.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/V	**Microcontroller #1 CS1# Routing Enable (MRE1):** Enables routing of I/O locations 62h and 66h to eSPI CS1#. This field is only writeable if the eSPI CS1 is enabled and is RO when eSPI CS1 is disabled.
10	0h RW/V	**Keyboard CS1# Routing Enable (KRE):** Enables routing of the keyboard I/O locations 60h and 64h to eSPI CS1#. This field is only writeable if the eSPI CS1 is enabled and is RO when eSPI CS1 is disabled.
9	0h RW/V	**High Gameport CS1# Routing Enable (HGRE):** Enables routing of the I/O locations 208h to 20Fh to eSPI CS1#. This field is only writeable if the eSPI CS1 is enabled and is RO when eSPI CS1 is disabled.
8	0h RW/V	**Low Gameport CS1# Routing Enable (LGRE):** Enables routing of the I/O locations 200h to 207h to eSPI CS1#. This field is only writeable if the eSPI CS1 is enabled and is RO when eSPI CS1 is disabled.
7:4	0h RO	**Reserved**
3	0h RW/V	**Floppy Drive CS1# Routing Enable (FDRE):** Enables routing of the FDD range to eSPI CS1#. Range is selected by LIOD.FDE. This field is only writeable if the eSPI CS1 is enabled and is RO when eSPI CS1 is disabled.
2	0h RW/V	**Parallel Port CS1# Routing Enable (PPRE):** Enables routing of the LPT range to eSPI CS1#. Range is selected by LIOD.LPT. This field is only writeable if the eSPI CS1 is enabled and is RO when eSPI CS1 is disabled.
1	0h RW/V	**Com Port B CS1# Routing Enable (CBRE):** Enables routing of the COMB range to eSPI CS1#. Range is selected by LIOD.CB. This field is only writeable if the eSPI CS1 is enabled and is RO when eSPI CS1 is disabled.
0	0h RW/V	**Com Port A CS1# Routing Enable (CARE):** Enables routing of the COMA range to eSPI CS1#. Range is selected by LIOD.CA. This field is only writeable if the eSPI CS1 is enabled and is RO when eSPI CS1 is disabled.

2.1.20 eSPI CS1 Generic IO Range 1 (ESPI_CS1GIR1) - Offset A4h

This register has the same bit definitions as PCLGIR1.

Note: This register is used to route variable IO transactions from the Host to the second Slave device (CS1#) over the Peripheral Channel on the eSPI bus.

Implementation Note: If this range is enabled (LPC Decode Enable = 1b) in a single Slave configuration (espi_cs1_en soft-strap = 0b), any IO accesses to the range must by U/Rd by eSPI-MC.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:18	00h RW	**Address[7:2] Mask (ADDR_MASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	0h RO	**Reserved**
15:2	0000h RW	**ADDR:** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
1	0h RO	**Reserved**
0	0h RW	**LPC Decode Enable (LDE):** When this bit is set to 1, then the range specified in this register is enabled for decoding to LPC.

2.1.21 eSPI CS1 Generic Memory Range 1 (ESPI_CS1GMR1) - Offset A8h

This register has the same bit definitions as PCLGMR.

Note: This register is used to route memory transactions from the Host to the second Slave device (CS1#) over the Peripheral Channel on the eSPI bus.

Implementation Note: If this range is enabled (LPC Decode Enable = 1b) in a single Slave configuration (espi_cs1_en soft-strap = 0b), any IO accesses to the range must by U/Rd by eSPI-MC.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Memory Address[31:16] (MADDR):** This field specifies a 64KB memory block anywhere in the 4GB memory space that will be decoded to LPC as standard LPC Memory Cycle if enabled.
15:1	0h RO	**Reserved**
0	0h RW	**LPC Memory Range Decode Enable (LGMRD_EN):** When this bit is set to 1, then the range specified in this register is enabled for decoding to LPC.

2.1.22 FWH ID Select 1 (ESPI_PCFS1) - Offset D0h

FWH ID Select 1.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

2.1.23 FWH ID Select 2 (ESPI_PCFS2) - Offset D4h

FWH ID Select 2.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

2.1.24 BIOS Decode Enable (ESPI_BDE) - Offset D8h

Note that this register affects the BIOS decode regardless of whether the BIOS is resident on SPI. The concept of Feature Space does not apply to SPI-based flash. PCH simply decodes these ranges as memory accesses when enabled for the SPI flash interface.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + D8h	0000FFCFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**BDE Lock Enable (BLE):** When this bit is set, the RW bits of this BDE register are locked down. Once set, this bit can only be cleared by PLTRST#. **Locked by:** ESPI_BDE.BLE
30:16	0h RO	**Reserved**
15	1h RO	**F8-FF Enable (EF8):** Enables decoding of 512K of the following BIOS range: Data space: FFF80000h - FFFFFFFFh Feature space: FFB80000h - FFBFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
14	1h RW/L	**F0-F8 Enable (EF0):** Enables decoding of 512K of the following BIOS range: Data space: FFF00000h - FFF7FFFFh Feature space: FFB00000h - FFB7FFFFh **Locked by:** ESPI_BDE.BLE
13	1h RW/L	**E8-EF Enable (EE8):** Enables decoding of 512K of the following BIOS range: Data space: FFE80000h - FFEFFFFFh Feature space: FFA80000h - FFAFFFFFh **Locked by:** ESPI_BDE.BLE
12	1h RW/L	**E0-E8 Enable (EE0):** Enables decoding of 512K of the following BIOS range: Data space: FFE00000h - FFE7FFFFh Feature Space: FFA00000h - FFA7FFFFh **Locked by:** ESPI_BDE.BLE
11	1h RW/L	**D8-DF Enable (ED8):** Enables decoding of 512K of the following BIOS range: Data space: FFD80000h - FFDFFFFFh Feature space: FF980000h - FF9FFFFFh **Locked by:** ESPI_BDE.BLE
10	1h RW/L	**D0-D7 Enable (ED0):** Enables decoding of 512K of the following BIOS range: Data space: FFD00000h - FFD7FFFFh Feature space: FF900000h - FF97FFFFh **Locked by:** ESPI_BDE.BLE
9	1h RW/L	**C8-CF Enable (EC8):** Enables decoding of 512K of the following BIOS range: Data space: FFC80000h - FFCFFFFFh Feature space: FF880000h - FF8FFFFFh **Locked by:** ESPI_BDE.BLE
8	1h RW/L	**C0-C7 Enable (EC0):** Enables decoding of 512K of the following BIOS range: Data space: FFC00000h - FFC7FFFFh Feature space: FF800000h - FF87FFFFh **Locked by:** ESPI_BDE.BLE
7	1h RW/L	**Legacy F Segment Enable (LFE):** This enables the decoding of the legacy 64KB range at F0000h - FFFFFh Note that decode for the BIOS legacy F segment is enabled by the LFE bit only, it is not affected by the GEN_PMCON_1.iA64_EN bit. **Locked by:** ESPI_BDE.BLE

Bit Range	Default & Access	Field Name (ID): Description
6	1h RW/L	**Legacy E Segment Enable (LEE):** This enables the decoding of the legacy 64KB range at E0000h - EFFFFh Note that decode for the BIOS legacy E segment is enabled by the LEE bit only, it is not affected by the GEN_PMCON_1.iA64_EN bit. **Locked by:** ESPI_BDE.BLE
5:4	0h RO	**Reserved**
3	1h RW/L	**70-7F Enable (E70):** Enables decoding of 1MB of the following BIOS range: Data space: FF700000h - FF7FFFFFh Feature space: FF300000h - FF3FFFFFh **Locked by:** ESPI_BDE.BLE
2	1h RW/L	**60-6F Enable (E60):** Enables decoding of 1MB of the following BIOS range: Data space: FF600000h - FF6FFFFFh Feature Space: FF200000h - FF2FFFFFh **Locked by:** ESPI_BDE.BLE
1	1h RW/L	**50-5F Enable (E50):** Enables decoding of 1MB of the following BIOS range: Data space: FF500000h - FF5FFFFFh Feature space: FF100000h - FF1FFFFFh **Locked by:** ESPI_BDE.BLE
0	1h RW/L	**40-4F Enable (E40):** Enables decoding of 1MB of the following BIOS range: Data space: FF400000h - FF4FFFFFh Feature space: FF000000h - FF0FFFFFh **Locked by:** ESPI_BDE.BLE

2.1.25 BIOS Control (ESPI_BC) - Offset DCh

BIOS Control.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + DCh	00000020h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW/L	**BIOS Write Reporting (Async-SMI) Enable (BWRE):** 1'b0: Disable reporting of BIOS Write event. 1'b1: Enable reporting of BIOS Write event (PCBC.BWRS = 1) using Async-SMI. **Locked by:** ESPI_BC.BILD
10	0h RW/1C/V	**BIOS Write Status (BWRS):** HW sets this bit if a memory write access is detected to a protected BIOS range. 1'b0: Memory writes to BIOS region not attempted or attempted with PCBC.WPD = 1. 1'b1: A memory writes transaction to BIOS region has been received with PCBC.WPD = 0. ***Note:*** An Async-SMI message is generated to report this event if PCBC.BWRE is set. ***Note:*** SW must write a 1 to this bit to clear it, which will also deassert the Async-SMI, if PCBC.BWRE is set.
9	0h RO	**Reserved**
8	0h RW/1C/V	**BIOS Write Protect Disable Status (BWPDS):** HW sets this bit if configuration write access is detected to protected PCBC.WPD bit. 1'b0: No attempt has been made to set PCBC.WPD with PCBC.LE = 1. 1'b1: A configuration write request has been received to set PCBC.WPD (0 1) with PCBC.LE = 1. ***Note:*** An IOSF-SB Sync-SMI (Assert_SSMI) message is generated to report this event if HW sets this bit. The unsuccessful completion for the configuration write is returned upon receiving the SMI_Ack message response. ***Note:*** SW must write a 1 to this bit to clear it, which will also deassert the Sync-SMI (IOSF-SB Deassert_SSMI message is generated). ***Note:*** The Sync-SMI sets the PMC SMI_STS.TCO_STS register.
7	0h RW/L	**BIOS Interface Lock-Down (BILD):** When set, prevents BC.TS and BC.BBS from being changed. This bit can only be written from 0 to 1 once. ***BIOS Note:*** This bit is not backed up in the RTC well. This bit should also be set in the BUC register in the RTC device to record the last state of this value following a cold reset. **Locked by:** ESPI_BC.BILD
6	0h RW/V/L	**Boot BIOS Strap (BBS):** This field determines the destination of accesses to the BIOS memory range. Bits Description; 0 SPI 1 Reserved When SPI is selected, the range that is decoded is further qualified by other configuration bits described in the respective sections. The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down is not set. **Locked by:** ESPI_BC.BILD
5	1h RW/L	**Enable InSMM.STS (EISS):** When this bit is set, the BIOS region is not writable until SMM sets the InSMM.STS bit. Today BIOS Flash is writable if WPD is a 1. If this bit (5) is set, then WPD must be a 1 and InSMM.STS (0xFED3_0880(0)) must be 1 also. If this bit (5) is clear, then BIOS is write-able based only on WPD = 1 and the InSMM.STS is a don't care. **Locked by:** ESPI_BC.LE

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO/V	**Top Swap (TS):** When set, PCH will invert either A16, A17, or A18 for cycles going to the BIOS space (but not the Feature space) in the FWH. When cleared, PCH will not invert A16. If booting from LPC (FWH) or eSPI, then the Boot Block Size is fixed at 64KB and A16 is inverted if Top Swap is enabled. If booting from SPI, then the BOOT_BLOCK_SIZE soft strap determines if A16, A17, or A18 should be inverted if Top Swap is enabled. ***Note:*** If the Top-Swap strap is asserted, then this bit cannot be cleared by software. The strap jumper should be removed and the system rebooted. ***BIOS Note:*** This bit provides a read-only path to view the state of the Top Swap strap. It is backed up and driven from the RTC well. BIOS will need to program the corresponding register in the RTC well, which will be reflected in this register.
3	0h RO	**Reserved**
2	0h RO/V	**eSPI Enable Pin Strap (ESPI):** eSPI Enable Pin Strap (ESPI): This field determines the destination of accesses to the D31:F0 and related Fixed and Variable IO and Memory decode ranges, including BIOS memory range. 1'b0: LPC is the D31:F0 target. 1'b1: eSPI is the D31:F0 target. ***Note:*** This field, along with the PCBC.BBS strap setting, determines PCH configuration. ***Note:*** This field cannot be overwritten by software (unlike the PCBC.BBS field). ***Note:*** This bit is also reflected in the LPC (D31:F0) and SPI Flash (D31:F5) PCI Configuration register Offset DCh.
1	0h RW/L	**Lock Enable (LE):** When set, setting the WP bit will cause SMI. When cleared, setting the WP bit will not cause SMI. Once set, this bit can only be cleared by a PLTRST#. When this bit is set, EISS - bit (5) of this register is locked down. **Locked by:** ESPI_BC.LE
0	0h RW	**Write Protect Disable (WPD):** When set, access to the BIOS space is enabled for both read and write cycles to BIOS. When cleared, only read cycles are permitted to the FWH or SPI flash. When this bit is written from a 0 to a 1 and the LE bit is also set, an SMI# is generated. This ensures that only SMM code can update BIOS.

2.1.26 PCI Clock Control (PCCTL) - Offset E0h

PCI Clock Control.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**Clock Run Enable (CLKRUN_EN):** Enables the CLKRUN# logic to stop the PCI clocks. If the SLP_EN bit is set, then the Intel PCH will drive CLKRUN# low. This will keep the PCI and LPC clocks running on the way to the sleeping state. This is required to meet an LPC specification. This does not necessarily mean that the CLKRUN_EN bit is forced low when SLP_EN is set. Even though the CLKRUN# signal will be low when SLP_EN is set, the state of the CLKRUN_EN bit is ignored when SLP_EN bit is set. This gives flexibility in the implementation.

2.1.27 Unsupported Request Error Status (URES) - Offset F0h

This register denotes the status for the unsupported request on IOSF Primary I/F.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + F0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/C	**Unsupported Request Detected (URD):** Set to 1 by hardware upon detecting an Unsupported Request on IOSF Primary interface that is not considered Advisory Non-Fatal. Cleared to 0 by SW. URD bit is only set based on IOSF primary bus interface activity. It is not set based on IOSF sideband bus interface activity.

2.1.28 Unsupported Request Error Control (UREC) - Offset F4h

This register denotes the status for the unsupported request on IOSF Primary I/F.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + F4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**Unsupported Request Reporting Enable (URRE):** If set to 1 by software, it allows reporting of an Unsupported Request as a system error.

2.1.29 Manufacturer's ID (ESPI_MANID) - Offset F8h

This register is assigned during the boot flow using the SetID message based on values found in the fuse block. All fields except MID will be reset by hardware to zero and set only by the SetID message.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:0] + F8h	00000F00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000F00h RO/P	**Manufacturers ID Field (MANID):** Manufacturer ID: Default value comes from straps

2.2 eSPI PCR Registers Summary

Table 2-1. Summary of eSPI PCR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4000h	4	eSPI PCR Register And Link Control (SLV_CFG_REG_CTL)	00000000h
4004h	4	eSPI PCR Register Data (SLV_CFG_REG_DATA)	00000000h
4020h	4	Peripheral Channel Error for Slave 0 (PCERR_SLV0)	00000080h
4024h	4	Peripheral Channel Error for Slave 1 (PCERR_SLV1)	00000000h
4030h	4	Virtual Wire Channel Error for Slave 0 (VWERR_SLV0)	00000000h
4034h	4	Virtual Wire Channel Error for Slave 1 (VWERR_SLV1)	00000000h
4040h	4	Flash Access Channel Error for Slave 0 (FCERR_SLV0)	00040080h
4050h	4	Link Error for Slave 0 (LNKERR_SLV0)	0000FF00h
4054h	4	Link Error for Slave 1 (LNKERR_SLV1)	0000FF00h

2.2.1 eSPI PCR Register And Link Control (SLV_CFG_REG_CTL) - Offset 4000h

Along with SLV_CFG_REG_DATA, this register controls Rd/Wr access to Slave Configuration registers using eSPI Get/Set_Configuration, Get_Status and In-Band Reset cycles. It allows Tunneled Access to Slave Configuration (TASC) registers from Host/CSME software/firmware.

Type	Size	Offset	Default
MMIO	32 bit	FD720000h + 4000h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Slave Configuration Register Access Enable (SCRE):** Writing a 1 to this field triggers an access (SCRT) to a Slave Config Register ('Go'). **Note:** Hardware clears this bit to 0 (& sets the SCRS field) when the transaction has completed on the eSPI bus. In the case of a configuration/status register read, the data is valid only after this bit has been cleared by HW. **Note:** The SCRE is effective only if SCRS is clear.
30:28	0h RW/1C/V	**Slave Configuration Register Access Status (SCRS):** This field is set by upon the completion of a configuration register access (SCRE). Software must clear this field by writing all 1s before initiating another Slave configuration register access (SCRE). 3'h0: Status not valid 3'h1: Slave No_Response 3'h2: Slave Response CRC Error 3'h3: Slave Response Fatal Error 3'h4: Slave Response Non-Fatal Error 3'h5 3'h6: Reserved 3'h7: No errors (transaction completed successfully)
27	0h RW/1S	**IOSF-SB eSPI Link Configuration Lock (SBLCL):** When set, eSPI-MC prevents writes (i.e., SET_CONFIGURATION) from this IOSF-SB TASC mechanism to any eSPI Specification defined Slave Capabilities and Configuration registers in the reserved register address range (0h 7FFh). Access to Slave implementation specific configuration registers outside this range are not impacted by this lock bit and are always available access protections to such registers are Slave implementation dependent. **Note:** This bit cannot be written to 0 once it has been set to 1. It can only be cleared by PLTRST# assertion. The lock is automatically disabled if and while the LNKERR_SLV0.SLCRR register bit is asserted (upon an eSPI link Fatal Error condition) to allow BIOS (or another SW agent) to attempt to recover the link. **Note:** This bit has no effect (i.e., IOSF-SB TASC is always enabled) when PLTRST# is asserted. **BIOS Note:** BIOS must ensure that this bit is set to 1 after initial eSPI link configuration is over to prevent any further (unintentional or malicious) changes to the eSPI link configuration via IOSF-SB (per AR from eSPI SAFE S1 review).
26:21	0h RO	**Reserved**
20:19	0h RW	**Slave ID (SID):** eSPI Slave ID (CS#) to which the Slave Configuration Register Access (SCRT) is directed. 2'b00: eSPI Slave 0 (EC/BMC) 2'b01: eSPI Slave 1 (Note: *Only* supported when a when a second eSPI Slave device is present) 2'b10: eSPI Slave 2 (Note: *Only* supported when a when a third eSPI Slave device is present) 2'b11: eSPI Slave 3 (Note: *Only* supported when a when a fourth eSPI Slave device is present)
18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Slave Configuration Register Access Type (SCRT):** Rd/Wr/Status 2'b00: Slave Configuration register read from address SCRA[11:0] (GET_CONFIG) 2'b01: Slave Configuration register write to address SCRA[11:0] (SET_CONFIG) 2'b10: Slave Status register read (GET_STATUS) 2'b11: In-Band Reset **Note:** Writes to Slave Configuration registers in the reserved address range (0h 7FFh) are gated by the SBLCL bit. **Note:** Setting this field to 2'b10 triggers a Get_Status command to the Slave. In this case, the SCRA field is ignored and only the lower 16-bits of the returned data (SLV_CFG_REG_DATA[15:0]) are valid. **Note:** Setting this field to 2'b11 triggers an In-Band Reset command to the Slave. In this case, the SCRA field is ignored and no data is returned. This command resets the link for the targeted Slave to a default configuration. Software is responsible for reinitializing the link to optimized (higher performance) settings using these registers.
15:12	0h RO	**Reserved**
11:0	000h RW	**Slave Configuration Register Address (SCRA):** Per eSPI Spec. / eSPI Compatibility Spec.

2.2.2 eSPI PCR Register Data (SLV_CFG_REG_DATA) - Offset 4004h

Along with SLV_CFG_REG_CTL, this register controls Rd/Wr access to Slave Configuration registers using eSPI Get/Set_Configuration cycles. It allows access to Slave configuration registers from Host/CSME software/firmware.

For writes (SCRT = 2'b01) to Slave Configuration registers, this register should be written to first with the required data before writing to the CTL register. The eSPI-MC processes the write to the Slave using an eSPI Set_Configuration command.

If a write is to a supported register in the reserved register address range (0h 7FFh), the eSPI-MC updates its local copy of the Slave configuration registers after the write has been successfully sent to the Slave.

Note: eSPI-MC does no checking of the register values (even for supported Slave Capabilities / Configuration Registers) the SW assumes full responsibility for programming legal values supported by both the eSPI-MC and the Slave.

For reads (SCRT = 2'b00 or 2b10) to Slave Configuration registers, the hardware writes the data read back from the Slave into this register. The read data is valid after hardware has cleared the SCRE bit in the CTL register and the SCRS field indicates a successful transaction.

Type	Size	Offset	Default
MMIO	32 bit	FD720000h + 4004h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Slave Configuration Register for Read and Write data (SCRD):** Configuration register Write data from software or read data from the Slave. For writes, this register must be programmed before the CTL register. For reads, data in this register is valid after the CTL.SCRE bit has been cleared by HW and the CTL.SCRS field indicates a successful transaction.

2.2.3 Peripheral Channel Error for Slave 0 (PCERR_SLV0) - Offset 4020h

Peripheral Channel Error for Slave 0

Type	Size	Offset	Default
MMIO	32 bit	FD720000h + 4020h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Slave Host Reset Ack Override (SLV_HOST_RST_ACK_OVRD):** A 1 in this bit will cause the eSPI-MC to not wait for the Slave HOST_RESET_ACK Virtual Wire before (immediately) asserting the ResetPrepAck (Host space, GenPrep). The Host_Reset_Warn VW will be transmitted to the Slave independent of the setting for this bit.
27:26	0h RW	**Peripheral Channel Received Master or Target Abort Reporting Enable (PCRMTARE):** 2'b00: Disable RMA or RTA Reporting 2'b01: Reserved 2'b10: Enable RMA or RTA Reporting as SERR (IOSF-SB Do_SErr message) 2'b11: Enable RMA or RTA Reporting as SMI (IOSF-SB Assert_SMI message) **Note:** SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. **Note:** SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted.
25	0h RW	**Peripheral Channel Unsupported Request Reporting Enable (PCURRE):** If set to 1 by software, it allows reporting of an Unsupported Request (UR) as a System Error (SERR). If eSPI-MC decodes a Posted transaction on IOSF-P Host Root Space that is not supported, it sets the PCURD bit. If PCCMD.SEE (SERR enable) is also set to 1, then eSPI-MC sets the PCSTS.SSE (Signaled System Error) bit and sends a Do_SErr message on its IOSF-SB interface. Note: If the transaction was a Non-Posted request, then the agent handles the transaction as an Advisory Non-Fatal error, and no error logging or signaling is done. The Completion with UR Completion Status serves the purpose of error reporting.
24	0h RW/1C/V	**Peripheral Channel Unsupported Request Detected (PCURD):** Set to 1 by hardware upon detecting an Unspported Request (UR) that is not considered an Advisory Non-Fatal error and PCERR.PCURRE is set. Cleared to 0 when software writes a 1 to this register.
23:15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RW	**Peripheral Channel Non-Fatal Error Reporting Enable (PCNFEE):** 2'b00: Disable Non-Fatal Error Reporting 2'b01: Reserved 2'b10: Enable Non-Fatal Error Reporting as SERR (IOSF-SB Do_SErr message) 2'b11: Enable Non-Fatal Error Reporting as SMI (IOSF-SB Assert_SMI message) **Note:** SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. **Note:** SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. **Note:** SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
12	0h RW/1C/V	**Peripheral Channel Non-Fatal Status (PCNFES):** This field is set by hardware if a Non-Fatal Error condition is detected on the Peripheral Channel. Software must clear this bit. 1'b0: No Non-Fatal Error detected 1'b1: Non-Fatal Error detected (PCNFEC has a non-zero value) **Note:** Clearing this unlocks the PCNFEC field and triggers an IOSF-SB Deassert_SMI message if PCNFEE is set to SMI. **Note:** Setting of this bit is independent of the enable to generate a SMI/SERR (PCNFEE).
11:8	0h RO/V	**Peripheral Channel Non-Fatal Cause (PCNFEC):** 4'h0: No error 4'h1: Slave Response Code: NONFATAL_ERROR 4'h2: Slave Response Code: Unsuccessful Completion 4'h3: Unexpected completion received from Slave (i.e. completion without non-posted request or completion with invalid tag or completion with invalid length) 4'h4: Unsupported Cycle Type (w.r.t. Command) 4'h5: Unsupported Message Code 4'h6: Unsupported Address/Length alignment (upstream only): Memory: Address + Length > 64 B (aligned) [for both Posted and Non-Posted transactions] 4'h7: Unsupported Address/Length alignment (upstream only): Memory: 64-bit Address with Addr[63:32] = 0h [for both Posted and Non-Posted transactions] 4'h8 - 4'hF: Reserved **Note:** This field is updated after a Peripheral channel transaction is completed if the PCNFES bit is not set.
7	1h RW	**PLCC Misaligned Memory Access (PMMA):** Applies to only posted and non-posted memory transactions directed towards D31:f0 to be sent over the eSPI Peripheral Channel to an eSPI Slave. 1'b0: Requests with a length of 3 bytes or requests with a length of 1/2/4 bytes whose Address+Length is not DWord aligned will be rejected. 1'b1: Requests with a length of 3 bytes or requests with a lenght of 1/2/4 butes whose Address+Length is not DWord aligned will be sent to the slave using the memory write/read format.

Bit Range	Default & Access	Field Name (ID): Description
6:5	0h RW	**Peripheral Channel Fatal Error Reporting (PCFEE):** 2'b00: Disable Fatal Error Reporting 2'b01: Reserved 2'b10: Enable Fatal Error Reporting as SERR (IOSF-SB Do_SErr message) 2'b11: Enable Fatal Error Reporting as SMI (IOSF-SB Assert_SMI message) **Note:** SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. **Note:** SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. **Note:** SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
4	0h RW/1C/V	**Peripheral Channel Fatal Error Reporting (PCFES):** This field is set by hardware if a Fatal Error condition is detected on the Peripheral Channel. Software must clear this bit by writing a 1 to it. 1'b0: No Fatal Error detected 1'b1: Fatal Error Type 2 detected (PCFEC has a non-zero value) **Note:** Clearing this unlocks the PCFEC field and triggers an IOSF-SB Deassert_SMI message if PCFEE is set to SMI. **Note:** Setting of this bit is independent of the enable to generate a SMI/SERR (PCFEE).
3:0	0h RO/V	**Peripheral Channel Fatal Error Cause (PCFEC):** 4'h0: No error 4'h1 4'h7: Reserved 4'h8: Malformed Slave Response Payload: Payload length > Max Payload Size (aligned) [Type 2] 4'h9: Malformed Slave Response Payload: Read request size > Max Read Request Size (aligned) [Type 2] 4'hA: Malformed Slave Response Payload: Address + Length > 4KB (aligned) [Type 2] 4'hB 4'hF: Reserved **Note:** This field is updated after a Peripheral channel transaction is completed if the PCFES bit is not set.

2.2.4 Peripheral Channel Error for Slave 1 (PCERR_SLV1) - Offset 4024h

This register is used to control error reporting for the eSPI Peripheral Channel for the second eSPI Slave device.

Note: Accesses to this register must respond with a U/R when a second eSPI Slave device is not present (i.e., in a single Slave configuration).

The register definition is identical to that of PCERR_SLV0, with the following exception:

SLV_HOST_RST_ACK_OVRD (bit [28]): This bit has no impact since the Host_Reset_Ack VW from CS1# is not supported by eSPI-MC (Host partition reset flow is gated only for CS0#).

Type	Size	Offset	Default
MMIO	32 bit	FD720000h + 4024h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Slave Host Reset Ack Override (SLV_HOST_RST_ACK_OVRD):** This bit has no impact since the Host_Reset_Ack VW from CS1# is not supported by eSPI-MC (Host partition reset flow is gated only for CS0#).
27:26	0h RW	**Peripheral Channel Received Master or Target Abort Reporting Enable (PCRMTARE):** Not used by the design. The field in the Slave 0 register is used.
25	0h RW	**Peripheral Channel Unsupported Request Reporting Enable (PCURRE):** See PCERR_SLV0.PCURRE.
24	0h RW/1C/V	**Peripheral Channel Unsupported Request Detected (PCURD):** See PCERR_SLV0.PCURD
23:15	0h RO	**Reserved**
14:13	0h RW	**Peripheral Channel Non-Fatal Error Reporting Enable (PCNFEE):** See PCERR_SLV0.PCNFEE.
12	0h RW/1C/V	**Peripheral Channel Non-Fatal Status (PCNFES):** See PCERR_SLV0.PCNFES.
11:8	0h RO/V	**Peripheral Channel Non-Fatal Cause (PCNFEC):** See PCERR_SLV0.PCNFEC.
7	0h RO	**Reserved**
6:5	0h RW	**Peripheral Channel Fatal Error Reporting (PCFEE):** See PCERR_SLV0.PCFEE.
4	0h RW/1C/V	**Peripheral Channel Fatal Error Reporting (PCFES):** See PCERR_SLV0.PCFES.
3:0	0h RO/V	**Peripheral Channel Fatal Error Cause (PCFEC):** See PCERR_SLV0.PCFEC.

2.2.5 Virtual Wire Channel Error for Slave 0 (VWERR_SLV0) - Offset 4030h

This register is used to control error reporting for the eSPI Virtual Wire Channel

Type	Size	Offset	Default
MMIO	32 bit	FD720000h + 4030h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW/L	**Master HOST_C10, NMIOUT# and SMIOUT# (Virtual Wires) to Slave Enable Lock (VWNSMIEL):** 1'b0: VWHC10OE(if present), VMNMIOE, VWSMIOEi, and VWNSMIEL fields are not locked (writeable by SW) 1'b1: VWHC10OE(if present), VMNMIOE, VWSMIOE, and VWNSMIEL fields are locked **Note:** This bit can be cleared only upon assertion of eSPI_Reset#. **Note:** This field is supported for server platforms only. **Locked by:** VWERR_SLV0.VWNSMIEL
27	0h RW/L	**Master NMIOUT (Virtual Wire) to Slave Enable (VWNMIOE):** 1'b0: Disable NMIOUT# reporting (NMI#_Sent indication from ITSS is ignored) 1'b1: Enable NMIOUT# reporting to Slave via eSPI Virtual Wire (upon receiving a NMI#_Sent indication from ITSS) **Note:** This field is supported for server platforms only. **Note:** This bit is locked when VWNSMIEL = 1. **Locked by:** VWERR_SLV0.VWNSMIEL
26	0h RW/L	**Master SMIOUT (Virtual Wire) to Slave Enable (VWSMIOE):** 1'b0: Disable SMIOUT# reporting (SMI#_Sent indication from PMC is ignored) 1'b1: Enable SMIOUT# reporting to Slave via eSPI Virtual Wire (upon receiving a SMI#_Sent indication from PMC) **Note:** This field is supported for server platforms only. **Note:** This bit is locked when VWNSMIEL = 1. **Locked by:** VWERR_SLV0.VWNSMIEL
25	0h RW/L	**Master HOST_C10 (Virtual Wire) to Slave Enable (VWHC10OE):** 1'b0: Disable HOST_C10 reporting (HOST_C10 indication from PMC is ignored) 1'b1: Enable HOST_C10 reporting to Slave via eSPI Virtual Wire (upon receiving a HOST_C10 indication from PMC) **Note:** This field is supported for server platforms only. **Note:** This bit is locked when VWNSMIEL = 1. **Locked by:** VWERR_SLV0.VWNSMIEL
24:15	0h RO	**Reserved**
14:13	0h RW	**Virtual Wire Channel Non-Fatal Error Reporting Enable (VWNFEE):** 2'b00: Disable Non-Fatal Error Reporting 2'b01: Reserved 2'b10: Enable Non-Fatal Error Reporting as SERR (IOSF-SB Do_SErr message) 2'b11: Enable Non-Fatal Error Reporting as SMI (IOSF-SB Assert_SMI message) **Note:** SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. **Note:** SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. **Note:** SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
12	0h RW/1C/V	**Virtual Wire Channel Non-Fatal Error Status (VWNFES):** This field is set by hardware if a Non-Fatal Error condition is detected on the Virtual Wire Channel. Software must clear this bit. 1'b0: No Non-Fatal Error detected 1'b1: Non-Fatal Error detected (VWNFEC has a non-zero value) **Note:** Clearing this unlocks the VWNFEC field and triggers an IOSF-SB Deassert_SMI message if VWNFEE is set to SMI. **Note:** Setting of this bit is independent of the enable to generate a SMI/SERR (VWNFEE).

Bit Range	Default & Access	Field Name (ID): Description
11:8	0h RO/V	**Virtual Wire Channel Non-Fatal Error Cause (VWNFEC):** 4'h0: No error 4'h1: Slave Response Code: NONFATAL_ERROR 4'h2 4'h5: Reserved 4'h6 4'hD: Reserved 4'hE: Slave Virtual Wire: NON_FATAL_ERROR: 0->1 transition (1->0 transition on this VW is ignored) 4'hF: Reserved **Note:** This field is updated after a Virtual Wire Channel transaction is completed if the VWNFES bit is not set.
7	0h RO	**Reserved**
6:5	0h RW	**Virtual Wire Channel Fatal Error Reporting Enable (VWFEE):** 2'b00: Disable Fatal Error Reporting 2'b01: Reserved 2'b10: Enable Fatal Error Reporting as SERR (IOSF-SB Do_SErr message) 2'b11: Enable Fatal Error Reporting as SMI (IOSF-SB Assert_SMI message) **Note:** SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. **Note:** SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. **Note:** SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
4	0h RW/1C/V	**Virtual Wire Channel Fatal Error Status (VWFES):** This field is set by hardware if a Fatal Error condition is detected on the Virtual Wire Channel. Software must clear this bit by writing all 1s to it. 1'b0: No Fatal Error detected 1'b1: Fatal Error Type 2 detected (VWFEC has a non-zero value) **Note:** Clearing this unlocks the VWFEC field and triggers an IOSF-SB Deassert_SMI message if VWFEE is set to SMI. **Note:** Setting of this bit is independent of the enable to generate a SMI/SERR (VWFEE).
3:0	0h RO/V	**Virtual Wire Channel Fatal Error Cause (VWFEC):** 4'h0: No error 4'h1 4'h7: Reserved 4'h8: Malformed Slave Response Payload: VW Count > Max. VW Count [Type 2] 4'h9 4'hD: Reserved 4'hE: Slave Virtual Wire: FATAL_ERROR 0->1 transition (1->0 transition on this VW is ignored) [Type 2] 4'hF: Reserved **Note:** This field is updated after a Virtual Wire Channel transaction is completed if the VWFES bit is not set.

2.2.6 Virtual Wire Channel Error for Slave 1 (VWERR_SLV1) - Offset 4034h

This register is used to control error reporting for the eSPI Virtual Wire Channel for the second eSPI Slave device.

Note: Accesses to this register must respond with a U/R when a second eSPI Slave device is not present (i.e., in a single Slave configuration).

The register definition is identical to that of VWERR_SLV0, with the following exception:

VWNSMIEL, VWNMIOE, VWSMIOE (bits [28:26]): These bits are not supported. The correspomding bits for Slave0 in VWERR_SLV0 register cover NMI# and SMI# transmission to both Slaves.

Type	Size	Offset	Default
MMIO	32 bit	FD720000h + 4034h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RO	**Master NMIOUT# and SMIOUT# (Virtual Wires) to Slave Enable Lock (VWNSMIEL):** These bits are not supported. The corresponding bits for Slave0 in VWERR_SLV0 register cover NMI# and SMI# transmission to both Slaves.
27	0h RO	**Master NMIOUT (Virtual Wire) to Slave Enable (VWNMIOE):** These bits are not supported. The corresponding bits for Slave0 in VWERR_SLV0 register cover NMI# and SMI# transmission to both Slaves.
26	0h RO	**Master SMIOUT (Virtual Wire) to Slave Enable (VWSMIOE):** These bits are not supported. The corresponding bits for Slave0 in VWERR_SLV0 register cover NMI# and SMI# transmission to both Slaves.
25:15	0h RO	**Reserved**
14:13	0h RW	**Virtual Wire Channel Non-Fatal Error Reporting Enable (VWNFEE):** See VWERR_SLV0.VWNFEE.
12	0h RW/1C/V	**Virtual Wire Channel Non-Fatal Error Status (VWNFES):** See VWERR_SLV0.VWNFES.
11:8	0h RO/V	**Virtual Wire Channel Non-Fatal Error Cause (VWNFEC):** See VWERR_SLV0.VWNFEC.
7	0h RO	**Reserved**
6:5	0h RW	**Virtual Wire Channel Fatal Error Reporting Enable (VWFEE):** See VWERR_SLV0.VWFEE.
4	0h RW/1C/V	**Virtual Wire Channel Fatal Error Status (VWFES):** See VWERR_SLV0.VWFES.
3:0	0h RO/V	**Virtual Wire Channel Fatal Error Cause (VWFEC):** See VWERR_SLV0.VWFEC.

2.2.7 Flash Access Channel Error for Slave 0 (FCERR_SLV0) - Offset 4040h

This register is used to determine how to log and report errors on the Flash Access channel, for both Master and Slave Attached Flash configurations.

Type	Size	Offset	Default
MMIO	32 bit	FD720000h + 4040h	00040080h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	1h RO/V	**SAF CAM Empty (SAFCAMEMPTY):** Only valid in slave-attached flash mode. Will always read 1 otherwise. 0: SAF CAM is not empty - there are outstanding NP flash transactions to the eSPI slave. 1: SAF CAM is empty - there are no outstanding NP flash transactions to the eSPI slave.
17	0h RW/1C/V	**SAF Blocked (SAFBLK):** Only valid in slave-attached flash mode. Will never be set to 1 by hardware otherwise. Set to 1 by hardware, when SAF NF Error Blocking Enable is set, when a NON_FATAL_ERROR response is received in response to a GET_FLASH_C. When this bit is set, the eSPI master will not issue any additional transactions on the flash channel. Software must write a 1 to clear this bit.
16	0h RW	**SAF NF Error Blocking Enable (SAFNFEBLKEN):** Only valid in slave-attached flash mode. Has no impact otherwise. 1: the flash channel will be blocked when a NON_FATAL_ERROR response is received in response to a GET_FLASH_C. 0: the flash channel will NOT be blocked when a NON_FATAL_ERROR response is received in response to a GET_FLASH_C.
15	0h RO	**Reserved**
14:13	0h RW	**Flash Access Channel Non-Fatal Error Reporting Enable (FCNFEE):** 2'b00: Disable Non-Fatal Error Reporting 2'b01: Reserved 2'b10: Enable Non-Fatal Error Reporting as SERR (IOSF-SB Do_SErr message) 2'b11: Enable Non-Fatal Error Reporting as SMI (IOSF-SB Assert_SMI message) **Note:** SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. **Note:** SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. **Note:** SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
12	0h RW/1C/V	**Flash Access Channel Non-Fatal Error Status (FCNFES):** This field is set by hardware if a Non-Fatal Error condition is detected on the Flash Access Channel. Software must clear this bit. 1'b0: No Non-Fatal Error detected 1'b1: Non-Fatal Error detected (FCNFEC has a non-zero value) **Note:** Clearing this unlocks the FCNFEC field and triggers an IOSF-SB Deassert_SMI message if FCNFEE is set to SMI. **Note:** Setting of this bit is independent of the enable to generate a SMI/SERR (FCNFEE).

Bit Range	Default & Access	Field Name (ID): Description
11:8	0h RO/V	**Flash Access Channel Non-Fatal Error Cause (FCNFEC):** 4'h0: No error 4'h1: Slave Response Code: NONFATAL_ERROR received in response to GET_FLASH_NP, PUT_FLASH_C [for Master-Attached Flash accesses only] or GET_FLASH_C [for Slave-Attached Flash accesses only]. 4'h2: Slave Response Code: Unsuccessful Completion [for Slave-Attached Flash accesses only] 4'h3: Unexpected completion received from Slave (i.e. completion without non-posted request or completion with invalid tag or completion with invalid length) [for Slave-Attached Flash accesses only] 4'h4: Unsupported Cycle Type (w.r.t. Command) [for SPT-LP Master Attached Flash this should only be unsupported Erase Block Size] 4'h5: Slave Response Code: NONFATAL_ERROR received in response to PUT_FLASH_NP [for Slave-Attached Flash accesses only]. 4'h6: Unsupported Address (i.e., address > Flash linear address range) [for Master-Attached Flash accesses only] set to Flash Access Error 4'h7: Reserved 4'h8-4'hF: Reserved **Note:** This field is updated after a Flash Access Channel transaction is completed if the FCNFES bit is not set
7	1h RW	**Master Attached Flash Request Priority (MAFRP):** 1'b0: MAF Completion Requests are highest priority 1'b1: MAF Non-posted Requests are highest priority
6:5	0h RW	**Flash Access Channel Fatal Error Reporting Enable (FCFEE):** 2'b00: Disable Fatal Error Reporting 2'b01: Reserved 2'b10: Enable Fatal Error Reporting as SERR (IOSF-SB Do_SErr message) 2'b11: Enable Fatal Error Reporting as SMI (IOSF-SB Assert_SMI message) **Note:** SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. **Note:** SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. **Note:** SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
4	0h RW/1C/V	**Flash Access Channel Fatal Error Status (FCFES):** This field is set by hardware if a Fatal Error condition is detected on the Flash Access Channel. Software must clear this bit by writing a 1 to it. 1'b0: No Fatal Error detected 1'b1: Fatal Error Type 2 detected (FCFEC has a non-zero value) **Note:** Clearing this unlocks the FCFEC field and triggers an IOSF-SB Deassert_SMI message if FCFEE is set to SMI. **Note:** Setting of this bit is independent of the enable to generate a SMI/SERR (FCFEE).
3:0	0h RO/V	**Flash Access Channel Fatal Error Cause (FCFEC):** 4'h0: No error 4'h1-4'h7: Reserved 4'h8: Malformed Slave Response Payload: Payload length > Max Payload Size [Type 2] 4'h9: Malformed Slave Response Payload: Read request size > Max Read Request Size [for Master-Attached Flash accesses only] [Type 2] 4'hA-4'hF: Reserved **Note:** This field is updated after a Flash Access Channel transaction is completed if the FCFES bit is not set.

2.2.8 Link Error for Slave 0 (LNKERR_SLV0) - Offset 4050h

This register is used to control link error reporting for the eSPI Slave 0.

Type	Size	Offset	Default
MMIO	32 bit	FD720000h + 4050h	0000FF00h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**eSPI Link and Slave Channel Recovery Required (SLCRR):** HW sets this bit when it has detected a Type 1 Fatal Error condition, for any channel (LFET1C is non-zero). Setting of this bit will trigger an error handling sequence by the eSPI-MC. SW must clear this bit (by writing a 1 to it) after it has taken all necessary actions to recover the link. This indicates the eSPI-MC to resume HW initiated transactions with the Slave.
30:23	0h RO	**Reserved**
22:21	0h RW	**Fatal Error Type 1 Reporting Enable (LFET1E):** 2'b00: Disable Fatal Error Type 1 Reporting 2'b01: Reserved 2'b10: Enable Fatal Error Type 1 Reporting as SERR (IOSF-SB Do_SErr message) 2'b11: Enable Fatal Error Type 1 Reporting as SMI (IOSF-SB Assert_SMI message) **Note:** SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. **Note:** SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. **Note:** SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted). **Note:** When this error is reported, SW must also inspect and handle the SLCRR field.
20	0h RW/1C/V	**Fatal Error Type 1 Reporting Status (LFET1S):** This field is set by hardware if a Link Fatal Error Type 1 condition is detected on the eSPI link (any transaction). Software must clear this bit by writing a 1 to it. 1'b0: No Link Fatal Error Type 1 detected 1'b1: Fatal Error Type 1 detected (LFET1C has a non-zero value) **Note:** Clearing this unlocks the LFET1C field and triggers an IOSF-SB Deassert_SMI message if LFET1E is set to SMI. **Note:** Setting of this bit is independent of the enable to generate a SMI/SERR (LFET1E).
19:16	0h RO/V	**Link Fatal Type 1 cause (LFET1C):** 4'h0: No error 4'h1: Slave Response Code: NO_RESPONSE [Type 1] 4'h2: Slave Response Code: FATAL_ERROR [Type 1] or length in header >= 512 Bytes 4'h3: Slave Response Code: CRC_ERROR [Type 1] 4'h4: Invalid Slave Response Code (w.r.t. to Command) [Type 1] 4'h5: Invalid Slave Cycle Type (w.r.t. to Command) [Type 1] 4'h6 4'hF: Reserved **Note:** This field is updated after a transaction (any channel) is completed if the LFET1S bit is clear. **Note:** A non-zero value in this field also causes the SLCRR bit to be set.
15:8	FFh RO/V	**Link Fatal Error Type 1 Cycle Type (LFET1CTYP):** When LFET1C is set, this field reflects the Cycle Type for the transaction that encountered the Fatal Error Type 1. If no valid Cycle Type exists w.r.t. the Command (LFET1CMD), this field is set to 8hFF to indicate that it should be ignored. **Note:** This field is updated after a transaction (any channel) is completed if the LFET1S bit is clear.
7:0	00h RO/V	**Link Fatal Error Type 1 Command (LFET1CMD):** When LFET1C is set, this field reflects the Command for the transaction that encountered the Fatal Error Type 1. **Note:** This field is updated after a transaction (any channel) is completed if the LFET1S bit is clear.

2.2.9 Link Error for Slave 1 (LNKERR_SLV1) - Offset 4054h

This register is used to log and control link error reporting for the second eSPI Slave device.

Note: Accesses to this register must respond with a U/R when a second eSPI Slave device is not present (i.e., in a single Slave configuration).

The register definition is identical to that of LNKERR_SLV0.

Type	Size	Offset	Default
MMIO	32 bit	FD720000h + 4054h	0000FF00h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**eSPI Link and Slave Channel Recovery Required (SLCRR):** See LNKERR_SLV0.SLCRR.
30:23	0h RO	**Reserved**
22:21	0h RW	**Fatal Error Type 1 Reporting Enable (LFET1E):** See LNKERR_SLV0.LFET1E.
20	0h RW/1C/V	**Fatal Error Type 1 Reporting Status (LFET1S):** See LNKERR_SLV0.LFET1S.
19:16	0h RO/V	**Link Fatal Type 1 cause (LFET1C):** See LNKERR_SLV0.LFET1C.
15:8	FFh RO/V	**Link Fatal Error Type 1 Cycle Type (LFET1CTYP):** See LNKERR_SLV0.LFET1CTYP.
7:0	00h RO/V	**Link Fatal Error Type 1 Command (LFET1CMD):** See LNKERR_SLV0.LFET1CMD.

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3 Primary to Sideband Bridge (P2SB)

3.1 P2SB Configuration Registers Summary

This chapter documents the registers in Bus: 0, Device 31, Function 1.

Table 3-1. Summary of Bus: 0, Device: 31, Function: 1 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	PCI Identifier (PCIID)	4B208086h
4h	2	PCI Command (PCICMD)	0004h
Eh	1	PCI Header Type (PCIHTYPE)	00h
10h	4	Sideband Register Access BAR (SBREG_BAR)	00000004h
14h	4	Sideband Register BAR High DWORD (SBREG_BARH)	00000000h
2Ch	4	PCI Subsystem Identifiers (PCIHSS)	00000000h
50h	2	VLW Bus:Device:Function (VBDF)	00F8h
52h	2	ERROR Bus:Device:Function (EBDF)	00F8h
54h	4	Routing Configuration (RCFG)	0000C700h
60h	1	High Performance Event Timer Configuration (HPTC)	00h
64h	2	IOxAPIC Configuration (IOAC)	0000h
6Ch	2	IOxAPIC Bus:Device:Function (IBDF)	00F8h
70h	2	HPET Bus:Device:Function (HBDF)	00F8h
C0h	4	Display Bus:Device:Function (DISPBDF)	00060010h
C4h	2	ICC Register Offsets (ICCOS)	0000h
D0h	4	SBI Address (SBIADDR)	00000000h
D4h	4	SBI Data (SBIDATA)	00000000h
D8h	2	SBI Status (SBISTAT)	0000h
DAh	2	SBI Routing Identification (SBIRID)	0000h
DCh	4	SBI Extended Address (SBIEXTADDR)	00000000h
E0h	4	P2SB Control (P2SBC)	00000007h
E4h	1	Power Control Enable (PCE)	09h
200h	4	Sideband Register Posted 0 (SBREGPOSTED0)	00000000h
204h	4	Sideband Register Posted 1 (SBREGPOSTED1)	00000000h
208h	4	Sideband Register Posted 2 (SBREGPOSTED2)	00000000h
20Ch	4	Sideband Register Posted 3 (SBREGPOSTED3)	00000000h
210h	4	Sideband Register Posted 4 (SBREGPOSTED4)	00000000h
214h	4	Sideband Register Posted 5 (SBREGPOSTED5)	00000000h
218h	4	Sideband Register Posted 6 (SBREGPOSTED6)	00000000h
21Ch	4	Sideband Register Posted 7 (SBREGPOSTED7)	00000000h
220h	4	Endpoint Mask 0 (EPMASK0)	00000000h
224h	4	Endpoint Mask 1 (EPMASK1)	00000000h
228h	4	Endpoint Mask 2 (EPMASK2)	00000000h
22Ch	4	Endpoint Mask 3 (EPMASK3)	00000000h
230h	4	Endpoint Mask 4 (EPMASK4)	00000000h
234h	4	Endpoint Mask 5 (EPMASK5)	00000000h
238h	4	Endpoint Mask 6 (EPMASK6)	00000000h
23Ch	4	Endpoint Mask 7 (EPMASK7)	00000000h

3.1.1 PCI Identifier (PCIID) - Offset 0h

PCI header registers.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + 0h	4B208086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4B20h RO/V	**Device Identification (DID):** The upper 8-bits of this field can be overridden by the SetID IOSF-SB Message.
15:0	8086h RO	**Vendor Identification (VID):** Indicates Intel

3.1.2 PCI Command (PCICMD) - Offset 4h

PCI header registers.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:31, F:1] + 4h	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved**
10	0h RO	**Interrupt Disable (INTD):** P2SB does not issue any interrupts on its own behalf.
9	0h RO	**Fast Back to Back Enable (FB2BE):** Not applicable.
8	0h RW	**SERR# Enable (SEE):** This will enable parity error reporting to IEH.
7	0h RO	**Reserved**
6	0h RW	**Parity Error Response Enable (PEE):** This bit controls the device's response to parity error.
5	0h RO	**VGA Palette Snoop (VGA):** Not applicable.
4	0h RO	**Memory Write & Invalidate Enable (MWIE):** Not applicable.
3	0h RO	**Special Cycle Enable (SCE):** Not applicable.

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO	**Bus Master Enable (BME):** Bus mastering cannot be disabled as this device acts as a proxy for non-PCI devices.
1	0h RW	**Memory Space Enable (MSE):** Will control the P2SB acceptance of PCI MMIO BARs only. Other legacy regions are unaffected by this bit.
0	0h RW	**I/O Space Enable (IOSE):** Legacy regions are unaffected by this bit.

3.1.3 PCI Header Type (PCIHTYPE) - Offset Eh

PCI header registers.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:31, F:1] + Eh	00h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Multi-Function Device (MFD):** Indicates that this is part of a multi-function device.
6:0	0h RO	**Header Type (HTYPE):** Indicates a generic device header.

3.1.4 Sideband Register Access BAR (SBREG_BAR) - Offset 10h

PCI header registers.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + 10h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Register Base Address (RBA):** Lower DWORD of the base address for the sideband register access BAR.
23:4	0h RO	**Hardwired to 0 to request a BAR of 16MB (HW202RB16MB):** Hardwired to 0 to request a BAR of 16MB
3	0h RO	**PREF:** Indicates this is not pre-fetch-able.
2:1	2h RO	**Address Type (ATYPE):** Indicates that this can be placed anywhere in 64b space.
0	0h RO	**Space Type (STYPE):** Indicates memory space

3.1.5 Sideband Register BAR High DWORD (SBREG_BARH) - Offset 14h

PCI header registers.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Register Base Address (RBAH):** Upper DWORD of the base address for the sideband register access BAR.

3.1.6 PCI Subsystem Identifiers (PCIHSS) - Offset 2Ch

PCI header registers.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SSID):** Written by BIOS. Not used by hardware.
15:0	0h RW/O	**Subsystem Vendor ID (SSVID):** Written by BIOS. Not used by hardware.

3.1.7 VLW Bus:Device:Function (VBDF) - Offset 50h

This register specifies the Bus:Device:Function ID that the VLW VDM will use for its Requester ID.

This field is default to Bus 0: Device 31: Function 0 after reset. BIOS shall program this field accordingly if unique bus:device:function number is required for the VLW message.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:31, F:1] + 50h	00F8h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Bus Number (BUS):** VLW Bus Number
7:3	1Fh RW	**Device Number (DEV):** VLW Device Number
2:0	0h RW	**Function Number (FUNC):** VLW Function Number

3.1.8 ERROR Bus:Device:Function (EBDF) - Offset 52h

This register specifies the Bus:Device:Function ID that the Error Signaling messages VDM will use for its Requester ID.

This field is default to Bus 0: Device 31: Function 0 after reset. BIOS shall program this field accordingly if unique bus:device:function number is required for the VLW message.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:31, F:1] + 52h	00F8h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Bus Number (BUS):** ERROR Bus Number
7:3	1Fh RW	**Device Number (DEV):** ERROR Device Number
2:0	0h RW	**Function Number (FUNC):** ERROR Function Number

3.1.9 Routing Configuration (RCFG) - Offset 54h

This register contains information used for routing transactions between primary and sideband interfaces.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + 54h	0000C700h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	C7h RW	**Reserved Page Register Destination ID (RPRID):** Specifies the IOSF-SB destination ID for sending Reserved Page Register cycles (e.g. Port 80h). By default this will load to the ID of the eSPI device depending on which has been strapped active in the system.
7:1	0h RO	**Reserved**
0	0h RW	**RTC Shadow Enable (RSE):** When set, all IO writes to the RTC will be also sent to the PMC. This allows cases where the battery backed storage is in an external PMIC.

3.1.10 High Performance Event Timer Configuration (HPTC) - Offset 60h

HPET configuration register.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:31, F:1] + 60h	00h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Address Enable (AE):** When set, the P2SB will decode the High Performance Timer memory address range selected by bits 1:0 below.
6:2	0h RO	**Reserved**
1:0	0h RW	**Address Select (AS):** This 2-bit field selects 1 of 4 possible memory address ranges for the High Performance Timer functionality. The encodings are: 00: FED0_0000h - FED0_03FFFh 01: FED0_1000h - FED0_13FFFh 10: FED0_2000h - FED0_23FFFh 11: FED0_3000h - FED0_33FFFh

3.1.11 IOxAPIC Configuration (IOAC) - Offset 64h

IOAPIC configuration register.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:31, F:1] + 64h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	**Reserved**
8	0h RW	**Address Enable (AE):** When set, the P2SB will decode the IOxAPIC memory address range selected by bits 7:0 below.
7:0	0h RW	**APIC Range Select (ASEL):** These bits define address bits 19:12 for the IOxAPIC range. The default value of 00h enables compatibility with prior products as an initial value. This value must not be changed unless the IOxAPIC Enable bit is cleared.

3.1.12 IOxAPIC Bus:Device:Function (IBDF) - Offset 6Ch

This register specifies the Bus:Device:Function ID that the IOxAPIC will use in the following:

As the Requester ID when initiating Interrupt Messages to the CPU.

As the Completer ID when responding to the reads targeting the IOxAPICs Memory-Mapped I/O registers.

This field is default to Bus 0: Device 31: Function 0 after reset. BIOS shall program this field accordingly if unique Bus:Device:Function number is required for the internal IOxAPIC.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:31, F:1] + 6Ch	00F8h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Bus Number (BUS):** IOxAPIC Bus Number
7:3	1Fh RW	**Device Number (DEV):** IOxAPIC Device Number
2:0	0h RW	**Function Number (FUNC):** IOxAPIC Function Number

3.1.13 HPET Bus:Device:Function (HBDF) - Offset 70h

This register specifies the Bus:Device:Function ID that the HPET device will use in the following:

As the Requester ID when initiating Interrupt Messages to the CPU.

As the Completer ID when responding to the reads targeting the corresponding HPETs Memory-Mapped I/O registers.

This field is default to Bus 0: Device 31: Function 0 after reset. BIOS shall program this field accordingly if unique Bus:Device:Function number is required for the corresponding HPET.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:31, F:1] + 70h	00F8h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Bus Number (BUS):** HPET Bus Number
7:3	1Fh RW	**Device Number (DEV):** HPET Device Number
2:0	0h RW	**Function Number (FUNC):** HPET Function Number

3.1.14 Display Bus:Device:Function (DISPBDF) - Offset C0h

This register specifies the Bus:Device:Function ID that the Display initiated upstream RAVDMs will use for its Requester ID. This will also be used for the claiming these Route-by-ID RAVDMs downstreams.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + C0h	00060010h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18:16	6h RW	**Display Target Block (DTBLK):** This register contains the Target BLK field that will be used when sending RAVDM messages to the CPU Complex North Display.
15:8	0h RW	**Bus Number (BUS):** The bus number of the Display in the CPU Complex.
7:3	2h RW	**Device Number (DEV):** The bus number of the Display in the CPU Complex.
2:0	0h RW	**Function Number (FUNC):** The function number of the Display in the CPU Complex

3.1.15 ICC Register Offsets (ICCOS) - Offset C4h

This register contains the offsets to be used when sending RAVDMs to the Integrated Clock Controller. Each of the two spaces decoded for the ICC has a separate base address that will be used when sending those transactions on IOSF-SB to the ICC.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:31, F:1] + C4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Modulator Control Address Offset (MODBASE):** This specifies the upper 8b for the 16b address that will be used for sending RAVDM access that target the Modulator Control range of the ICC (FFF00h - FFFFFh).
7:0	0h RW	**Buffer Address Offset (BUFBASE):** This specifies the upper 8b for the 16b address that will be used for sending RAVDM access that target the Buffer range of the ICC (FFE00h - FFEFFh).

3.1.16 SBI Address (SBIADDR) - Offset D0h

Provides mechanism to send message on IOSFSB; the SAI check is only required on RS field but due to tool limitation, the SAI check is applied in RDL on whole register.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Destination Port ID (DESTID):** The content of this register field is sent in the IOSF Sideband Message Register Access dest field.
23:20	0h RO	**Reserved**
19:16	0h RW	**Root Space (RS):** Destination IOSF-SB Root Space. ***Note:*** This register may only be written during manufacturing test. P2SB will only accept writes to this register from transactions with a SAI equal to the SBI_RS_ACCESS_SAI parameter. This should be assigned to the SAI used by the functional test module (typically TAM) that will perform this register write on IOSF-P.
15:0	0h RW	**Address Offset (OFFSET):** Register address offsets. The content of this register field is sent in the IOSF Sideband Message Register Access address(15:0) field.

3.1.17 SBI Data (SBIDATA) - Offset D4h

Provides mechanism to send message on IOSFSB.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**DATA:** The content of this register field is sent on the IOSF sideband Message Register Access data(31:0) field.

3.1.18 SBI Status (SBISTAT) - Offset D8h

Provides mechanism to send message on IOSFSB.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:31, F:1] + D8h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**OPCODE:** This is the Opcode sent in the IOSF sideband message.
7	0h RW	**POSTED:** When set to 1, the message will be sent as a posted message instead of non-posted. This should only be used if the receiver is known to support posted operations for the specified operation.
6:3	0h RO	**Reserved**
2:1	0h RW/V	**Response Status (RESPONSE):** 00 - Successful 01 - Unsuccessful / Not Supported 10 - Powered Down 11 - Multi-cast Mixed This register reflects the response status for the previously completed transaction. The value of this register is only meaningful if SBISTAT.INITRDY is zero.
0	0h RW/1S	**Initiate/ Ready# (INITRDY):** 0: The IOSF sideband interface is ready for a new transaction 1: The IOSF sideband interface is busy with the previous transaction. A write to set this register bit to 1 will trigger an IOSF sideband message on the private IOSF sideband interface. The message will be formed based on the values programmed in the Sideband Message Interface Register Access registers. Software needs to ensure that the interface is not busy (SBISTAT.INITRDY is clear) before writing to this register.

3.1.19 SBI Routing Identification (SBIRID) - Offset DAh

Provides mechanism to send message on IOSFSB.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:31, F:1] + DAh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW	**First Byte Enable (FBE):** The content of this field is sent in the IOSF Sideband Register Access FBE field.
11	0h RO	**Reserved**
10:8	0h RW	**Base Address Register (BAR):** The contents of this field are sent in the IOSF Sideband Register Access BAR field. This should be zero performing a Memory Mapped operation to a PCI compliant device.
7:0	0h RW	**Function ID (FID):** The contents of this field are sent in the IOSF Sideband Register access FID field. This field should generally remain at zero unless specifically required by a particular application.

3.1.20 SBI Extended Address (SBIEXTADDR) - Offset DCh

Provides mechanism to send message on IOSFSB.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Extended Address (ADDR):** The content of this register field is sent on the IOSF sideband Message Register Access address(48:32) field. This must be set to all 0 if 16b addressing is desired.

3.1.21 P2SB Control (P2SBC) - Offset E0h

P2SB general configuration register.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + E0h	00000007h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/O	**SBI register Lock (SBILOCK):** Once written, it will not be writeable until module reset. Write once (1 or 0) to lock the Lock Bit. SBISTAT.INITRDY Register bit only lock if SBILOCK Bit = 1
30:28	0h RO	**Reserved**
27	0h RW	**VLW Wire Mode Enable (VWME):** When 1, VLW Wire Mode is enabled, where the VLW events from ITSS are received via the sideband wire handshake and this handshake is handled in P2SB as if a Posted Message is received from ITSS to the VLW VDM logic in Legacy Service agent. When 0, VLW Wire Mode is disabled, where the VLW events from ITSS are received via the IOSF Sideband using Non-Posted message. This policy is default to '0' which is the old behavior since Sunrise point. ***BIOS Note***: BIOS is expected to set this to '1' for Server Platform to mitigate in-out dependency risk.
26	0h RW	**Data Parity Error Enable (DPEE):** IOSFP data parity error handling (EP bit) enabling bit
25	0h RW	**Command Parity Error Enable (CPEE):** IOSFP command parity error handling enabling bit
24	0h RW	**Data Phase Parity Error Enable (DPPEE):** IOSFP data phase parity error handling enabling bit
23:18	0h RO	**Reserved**
17	0h RW/O	**Endpoint Mask Lock (MASKLOCK):** Locks the value of the EPMASK[0-7] registers. Once this value is written to a one it may only be cleared by a reset.
16	0h RW	**PGCB Clock Gating Enable (PGCBCGE):** When asserted the P2SB can de-assert the clock request to disable the PGCB clock dynamically when it reaches the power down idle state.
15:9	0h RO	**Reserved**
8	0h RW	**Hide Device (HIDE):** When this bit is set, the P2SB will return 1s on any PCI Configuration Read on IOSF-P. All other transactions including PCI Configuration Writes are unaffected by this. This does not affect reads performed on the IOSF-SB interface.
7:5	0h RO	**Reserved**
4	0h RW	**RAVDM Completion Status Policy Enable (RCSPE):** When this bit is SET, P2SB performs the following. 1) Return '000' (Successful Completion) for upstream Reg_rsp RAVDM on IOSF-P. 2) Return '001' (Unsupported Request) for upstream Reg_rsp. When clear P2SB always return '000' (Successful Completion) for Upstream Reg_rsp RAVDM
3	0h RO	**Reserved**
2:0	7h RW	**Max Writes Pending (MAXW):** This controls the max number of outstanding writes on IOSF-SB initiated by MMIO writes to the SBREG_BAR. Once the number of SBREG_BAR writes issued but not completed on IOSF-SB is equal to this value no new requests will be forwarded until completions are received. A value of zero will have the same behavior as the value of one (single write outstanding).

3.1.22 Power Control Enable (PCE) - Offset E4h

Power Control Enable register.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:31, F:1] + E4h	09h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RW	**Hardware Autonomous Enable (HAE):** When set, the P2SB will automatically engage power gating when it has reached its idle condition.
4	0h RO	**Reserved**
3	1h RO	**Sleep Enable (SE):** tied to 1
2	0h RO	**D3-Hot Enable (D3HE):** No support for D3 Hot power gating.
1	0h RO	**I3 Enable (I3E):** No support for S0i3 power gating.
0	1h RW	**PMC Power Gating Enable (PMCPG_EN):** When set to 1, the P2SB will engage power gating if it is idle and the pmc_p2sb_sw_pg_req_b signal is asserted.

3.1.23 Sideband Register Posted 0 (SBREGPOSTED0) - Offset 200h

Provides a mechanism to send MMIO writes as posted writes on the IOSFSB space.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + 200h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 0 (SBREGPOSTED0):** One hot masks for setting SBREG to posted for IOSF-SB endpoint IDs 31-0.

3.1.24 Sideband Register Posted 1 (SBREGPOSTED1) - Offset 204h

Provides a mechanism to send MMIO writes as posted writes on the IOSFSB space.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + 204h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 1 (SBREGPOSTED1):** One hot masks for setting SBREG to posted for IOSF-SB endpoint IDs 63-32.

3.1.25 Sideband Register Posted 2 (SBREGPOSTED2) - Offset 208h

Provides a mechanism to send MMIO writes as posted writes on the IOSFSB space.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + 208h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 0 (SBREGPOSTED2):** One hot masks for setting SBREG to posted for IOSF-SB endpoint IDs 95-64.

3.1.26 Sideband Register Posted 3 (SBREGPOSTED3) - Offset 20Ch

Provides a mechanism to send MMIO writes as posted writes on the IOSFSB space.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + 20Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 3 (SBREGPOSTED3):** One hot masks for setting SBREG to posted for IOSF-SB endpoint IDs 127-96.

3.1.27 Sideband Register Posted 4 (SBREGPOSTED4) - Offset 210h

Provides a mechanism to send MMIO writes as posted writes on the IOSFSB space.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + 210h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 4 (SBREGPOSTED4):** One hot masks for setting SBREG to posted for IOSF-SB endpoint IDs 159-128.

3.1.28 Sideband Register Posted 5 (SBREGPOSTED5) - Offset 214h

Provides a mechanism to send MMIO writes as posted writes on the IOSFSB space.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + 214h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 5 (SBREGPOSTED5):** One hot masks for setting SBREG to posted for IOSF-SB endpoint IDs 191-160.

3.1.29 Sideband Register Posted 6 (SBREGPOSTED6) - Offset 218h

Provides a mechanism to send MMIO writes as posted writes on the IOSFSB space.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + 218h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 6 (SBREGPOSTED6):** One hot masks for setting SBREG to posted for IOSF-SB endpoint IDs 223-192.

3.1.30 Sideband Register Posted 7 (SBREGPOSTED7) - Offset 21Ch

Provides a mechanism to send MMIO writes as posted writes on the IOSFSB space.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + 21Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 7 (SBREGPOSTED7):** One hot masks for setting SBREG to posted for IOSF-SB endpoint IDs 255-224.

3.1.31 Endpoint Mask 0 (EPMASK0) - Offset 220h

Provide a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + 220h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 0 (EPMASK0):** One hot masks for disabling IOSF-SB endpoint IDs 31-0 **Locked by:** P2SBC.MASKLOCK

3.1.32 Endpoint Mask 1 (EPMASK1) - Offset 224h

Provide a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + 224h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 1 (EPMASK1):** One hot masks for disabling IOSF-SB endpoint IDs 63-32 **Locked by:** P2SBC.MASKLOCK

3.1.33 Endpoint Mask 2 (EPMASK2) - Offset 228h

Provide a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + 228h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 2 (EPMASK2):** One hot masks for disabling IOSF-SB endpoint IDs 95-64 **Locked by:** P2SBC.MASKLOCK

3.1.34 Endpoint Mask 3 (EPMASK3) - Offset 22Ch

Provide a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + 22Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 3 (EPMASK3):** One hot masks for disabling IOSF-SB endpoint IDs 127-96 **Locked by:** P2SBC.MASKLOCK

3.1.35 Endpoint Mask 4 (EPMASK4) - Offset 230h

Provide a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + 230h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 4 (EPMASK4):** One hot masks for disabling IOSF-SB endpoint IDs 128-159 **Locked by:** P2SBC.MASKLOCK

3.1.36 Endpoint Mask 5 (EPMASK5) - Offset 234h

Provide a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + 234h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 5 (EPMASK5):** One hot masks for disabling IOSF-SB endpoint IDs 191-160 **Locked by:** P2SBC.MASKLOCK

3.1.37 Endpoint Mask 6 (EPMASK6) - Offset 238h

Provide a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + 238h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 6 (EPMASK6):** One hot masks for disabling IOSF-SB endpoint IDs 223-192 **Locked by:** P2SBC.MASKLOCK

3.1.38 Endpoint Mask 7 (EPMASK7) - Offset 23Ch

Provide a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:31, F:1] + 23Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 7 (EPMASK7):** One hot masks for disabling IOSF-SB endpoint IDs 255-224 **Locked by:** P2SBC.MASKLOCK

4 Power Management Controller (PMC)

4.1 PMC Configuration Registers Summary

This chapter documents the registers in Bus: 0, Device 31, Function 2.

Table 4-1. Summary of Bus: 0, Device: 31, Function: 2 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device Vendor ID (DEVVENDID)	4B218086h
4h	4	STATUSCOMMAND Status and Command (STATUSCOMMAND)	00100000h
8h	4	Revision Class Codes (REVCLASSCODE)	00000000h
Ch	4	CLLATHEADERBIST Cache Line Latency Header And BIST (CLLATHEADERBIST)	00000000h
10h	4	32-bit Base Address Register (BAR)	00000004h
14h	4	BAR HIGH (BAR_HIGH)	00000000h
18h	4	32-bit Base Address Register1 (BAR1)	00000004h
1Ch	4	BAR1 HIGH (BAR1_HIGH)	00000000h
20h	4	Bar 2 (BAR2)	00000001h
2Ch	4	Subsystem Identifiers (SUBSYSTEMID)	00000000h
30h	4	EXPANSION ROM BASEADDR (EXPANSION_ROM_BASEADDR)	00000000h
34h	4	CAPABILITY PTR (CAPABILITYPTR)	00000080h
3Ch	4	INTERRUPT REG Interrupt Register (INTERRUPTREG)	00000000h
80h	4	POWER CAP ID PowerManagement Capability ID (POWERCAPID)	48030001h
84h	4	PME CTRL STATUS (PMECTRLSTATUS)	00000008h
90h	4	PCIDEVIDLE CAP RECORD (PCIDEVIDLE_CAP_RECORD)	F0140009h
94h	4	DEVID VEND SPECIFIC REG (DEVID_VEND_SPECIFIC_REG)	01400010h
98h	4	D0I3 CONTROL SW LTR MMIO REG (D0I3_CONTROL_SW_LTR_MMIO_REG)	00000000h
9Ch	4	DEVICE IDLE POINTER REG (DEVICE_IDLE_POINTER_REG)	00000000h
A0h	4	D0I3 MAX POW LAT PG CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG)	00000800h
B0h	4	GEN REGRW1 (GEN_REGRW1)	00000000h
B4h	4	GEN REGRW2 (GEN_REGRW2)	00000000h
B8h	4	GEN REGRW3 (GEN_REGRW3)	00000000h
BCh	4	GEN REGRW4 (GEN_REGRW4)	00000000h
C0h	4	GEN INPUT REG (GEN_INPUT_REG)	00000000h
F8h	4	Manufacturer's ID (MANID)	00000000h

4.1.1 Device Vendor ID (DEVVENDID) - Offset 0h

Device Vendor ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 0h	00008086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4B21h RO	**Device Identification (DEVICEID):** These bits are controlled as follows: Bits [15:7]: SETID msg Bits [6:0]: strap_deviceid[6:0] (00 to 1F - variable).
15:0	8086h RO	**Vendor Identification (VENDORID):** Indicates Intel

4.1.2 STATUSCOMMAND Status and Command (STATUSCOMMAND) - Offset 4h

Status and Command

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW/1C	**RMA:** Received Master Abort
28	0h RW/1C	**RTA:** Received Target Abort
27:21	0h RO	**Reserved**
20	1h RO	**CAPLIST:** Capabilities List
19	0h RO	**INTR_STATUS:** Interrupt Status
18:11	0h RO	**Reserved**
10	0h RW	**INTR_DISABLE:** Interrupt Disable
9	0h RO	**Reserved**
8	0h RW	**SERR_ENABLE:** System Error Enable
7:3	0h RO	**Reserved**
2	0h RW	**BME:** Bus Master Enable
1	0h RW	**MSE:** Memory Space Enable
0	0h RO	**Reserved**

4.1.3 Revision Class Codes (REVCLASSCODE) - Offset 8h

Revision Class Codes

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**CLASS_CODES:** Class Codes
7:0	00h RO	**RID:** Revision ID

4.1.4 CLLATHEADERBIST Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch

Cache Line Latency Header And BIST

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**MULFNDEV:** Multi Function Device
22:16	00h RO	**HEADERTYPE:** Header Type
15:8	00h RO	**LATTIMER:** Latency Timer
7:0	00h RW	**CACHELINE_SIZE:** Cacheline Size

4.1.5 32-bit Base Address Register (BAR) - Offset 10h

Base Address Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 10h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:13	00000h RW	**BASEADDR:** Software programs this register with the base address of the device's memory region
12:4	000h RO	**Size Indicator (SIZEINDICATOR):** Hardwired to 0 to indicate 8KB of memory space
3	0h RO	**PREFETCHABLE:** A device can mark a range as pre-fetch-able if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables. Hardwired to 0 to indicate the device's memory space as not pre-fetch-able.
2:1	2h RO	**TYPE:** Hardwired to 10 to indicate that Base register is 64 bits wide and mapping can be done anywhere in the 64-bit Memory Space.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** Hardwired to 0 to identify a Memory BAR.

4.1.6 BAR HIGH (BAR_HIGH) - Offset 14h

BAR -Base Address Register High

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address HIGH (BASEADDR_HIGH):** Base Address

4.1.7 32-bit Base Address Register1 (BAR1) - Offset 18h

Base Address Register1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 18h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**BASEADDR1:** Software programs this register with the base address of the device's memory region
11:4	00h RO	**Size Indicator (SIZEINDICATOR1):** Hardwired to 0 to indicate 4KB of memory space

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**PREFETCHABLE1:** A device can mark a range as pre-fetch-able if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables. Hardwired to 0 to indicate the device's memory space as not pre-fetch-able.
2:1	2h RO	**TYPE1:** Hardwired to 10 to indicate that Base register is 64 bits wide and mapping can be done anywhere in the 64-bit Memory Space.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** Hardwired to 0 to identify a Memory BAR.

4.1.8 BAR1 HIGH (BAR1_HIGH) - Offset 1Ch

BAR1 - Base Address Register High

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address HIGH (BASEADDR1_HIGH):** Base Address HIGH

4.1.9 Bar 2 (BAR2) - Offset 20h

BAR - Base Address Register2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 20h	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**Base Address (BASEADDR):** Base Address
6:1	0h RO	**Reserved**
0	1h RO	**Message Space (MESSAGE_SPACE):** Hardwired to 1 to identify an IO BAR.

4.1.10 Subsystem Identifiers (SUBSYSTEMID) - Offset 2Ch

Subsystem Identifiers

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** Written by BIOS. Not used by hardware.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** Written by BIOS.Not used by hardware.

4.1.11 EXPANSION ROM BASEADDR (EXPANSION_ROM_BASEADDR) - Offset 30h

EXPANSION ROM base address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Expansion ROM Base

4.1.12 CAPABILITY PTR (CAPABILITYPTR) - Offset 34h

CAPABILITYPTR - Capabilities Pointer

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**CAPPTR_POWER:** Capabilities Pointer

4.1.13 INTERRUPT REG Interrupt Register (INTERRUPTREG) - Offset 3Ch

Interrupt Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**MAX_LAT:** Maximum Latency
23:16	00h RO	**MIN_GNT:** Minimum GNT
15:12	0h RO	**Reserved**
11:8	0h RO	**INTPIN:** Interrupt Pin
7:0	00h RW	**INTLINE:** Interrupt Line

4.1.14 POWER CAP ID Power Management Capability ID (POWERCAPID) - Offset 80h

Power Management Capability ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 80h	48030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	09h RO	**PMESUPPORT:** PME Support
26:19	0h RO	**Reserved**
18:16	3h RO	**VERSION:** Version
15:8	00h RO	**NXTCAP:** Next Capability
7:0	01h RO	**POWER_CAP:** Power Management Capability

4.1.15 PME CTRL STATUS (PMECTRLSTATUS) - Offset 84h

Power Management Control and Status Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C	**PMESTATUS:** PME Status
14:9	0h RO	**Reserved**
8	0h RW	**PMEENABLE:** PME Enable
7:4	0h RO	**Reserved**
3	1h RO	**NO_SOFT_RESET:** NO SOFT RESET
2	0h RO	**Reserved**
1:0	0h RW	**POWERSTATE:** Power State

4.1.16 PCIDEVIDLE CAP RECORD (PCIDEVIDLE_CAP_RECORD) - Offset 90h

PCI DEVICE IDLE CAPABILITY RECORD

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 90h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP:** Vendor Specific Capability ID
27:24	0h RO	**REVID:** Vendor Specific Capability Revision
23:16	14h RO	**CAP_LENGTH:** Vendor Specific Capability Length
15:8	00h RO	**NEXT_CAP:** NEXT Capability
7:0	09h RO	**CAPID:** Capability ID

4.1.17 DEVID VEND SPECIFIC REG (DEVID_VEND_SPECIFIC_REG) - Offset 94h

DEVID VENDOR SPECIFIC REG

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**VSEC_LENGTH:** Vendor Specific Extended Capability Length
19:16	0h RO	**VSEC_REV:** Vendor Specific Extended Capability Revision
15:0	0010h RO	**VSECID:** Vendor Specific Extended Capability ID

4.1.18 D0I3 CONTROL SW LTR MMIO REG (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h

SW LTR Update MMIO Location Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**SW_LAT_DWORD_OFFSET:** SW LTR Update MMIO Offset Location
3:1	0h RO	**SW_LAT_BAR_NUM:** SW LTR Bar Num
0	0h RO	**SW_LAT_VALID:** SW LTR Valid Strap

4.1.19 DEVICE IDLE POINTER REG (DEVICE_IDLE_POINTER_REG) - Offset 9Ch

Device IDLE Pointer Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**DWORD_OFFSET:** Device MMIO Offset Location
3:1	0h RO	**BAR_NUM:** D0i3 MMIO Location
0	0h RO	**VALID:** D0i3 Valid Strap

4.1.20 D0I3 MAX POW LAT PG CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h

DEVICE PG CONFIG

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + A0h	00000800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW	**HAE:** Hardware Autonomous Enable
20	0h RO	**Reserved**
19	0h RW	**SLEEP_EN:** Sleep Enable
18	0h RW	**PGE:** Power Gate Enable
17	0h RW	**I3_ENABLE:** I3 Enable
16	0h RW	**PMCRE:** PMC Request Enable
15:13	0h RO	**Reserved**
12:10	2h RW/O	**POW_LAT_SCALE:** Power On Latency Scale
9:0	000h RW/O	**POW_LAT_VALUE:** Power On Latency Value

4.1.21 GEN REGRW1 (GEN_REGRW1) - Offset B0h

General Purpose Read Write Register1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW1:** General Purpose PCI Register

4.1.22 GEN REGRW2 (GEN_REGRW2) - Offset B4h

General Purpose Read Write Register2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW2:** General Purpose PCI Register

4.1.23 GEN REGRW3 (GEN_REGRW3) - Offset B8h

General Purpose Read Write Register3

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW3:** General Purpose PCI Register

4.1.24 GEN REGRW4 (GEN_REGRW4) - Offset BCh

General Purpose Read Write Register4

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW4:** General Purpose PCI Register

4.1.25 GEN INPUT REG (GEN_INPUT_REG) - Offset C0h

General Purpose Input Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN REG INPUT_RW (GEN_REG_INPUT_RW):** General Purpose Input Register

4.1.26 Manufacturer's ID (MANID) - Offset F8h

Manufacturer ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + F8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Manufacturers ID (MANID):** Manufacturer ID

4.2 PMC Memory Mapped Registers Summary

Table 4-2. Summary of PMC Memory Mapped (MMIO) Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1020h	4	General PM Configuration A (GEN_PMCON_A)	20014000h
1024h	4	General PM Configuration B (GEN_PMCON_B)	00000004h
1030h	4	Configured Revision ID (CRID)	00000000h
1048h	4	Extended Test Mode Register 3 (ETR3)	00000000h
104Ch	4	SET STRAP MSG LOCK (SSML)	00000000h
1050h	4	SET STRAP MSG CONTROL (SSMC)	00000000h
1054h	4	SET STRAP MSG DATA (SSMD)	00000000h
10B0h	4	Configured Revision ID (CRID_UIP)	00000000h
10B4h	4	SLP S0 DEBUG REG0 (SLP_S0_DBG_0)	00000000h
10B8h	4	SLP S0 DEBUG REG1 (SLP_S0_DBG_1)	00000000h
10BCh	4	SLP S0 DEBUG REG2 (SLP_S0_DBG_2)	00000000h
10C0h	4	ModPHY Power Management Configuration Reg 1 (MODPHY_PM_CFG1)	00000000h
10C4h	4	ModPHY Power Management Configuration Reg 2 (MODPHY_PM_CFG2)	00000FFFh
10C8h	4	ModPHY Power Management Configuration Reg 3 (MODPHY_PM_CFG3)	00000000h
10CCh	4	ModPHY Power Management Configuration Reg 4 (MODPHY_PM_CFG4)	00000000h
10D0h	4	ModPHY Power Management Configuration Reg 5 (MODPHY_PM_CFG5)	00000000h
10D4h	4	ModPHY Power Management Configuration Reg 6 (MODPHY_PM_CFG6)	00000000h
11B8h	4	External Rail Config (EXT_RAIL_CONFIG)	00000000h
11C0h	4	External Rail Config (EXT_V1P05_VR_CONFIG)	00000000h
11C4h	4	External Rail Config (EXT_VNN_VR_CONFIG0)	00000000h
11C8h	4	VNN V1p05 Control Hold Off (VNN_V1P05_CTRL_HOLD_OFF)	00000101h
11CCh	4	EXT FET RAMP CFG (EXT_FET_RAMP_CFG)	00040004h
11D0h	4	VCCIN AUX CONFIG Register1 (VCCIN_AUX_CFG1)	00000000h
11D4h	4	VCCIN AUX CONFIG Register2 (VCCIN_AUX_CFG2)	00000000h
1200h	4	Always Running Timer Value 31:0 (ARTV_31_0)	00000000h
1204h	4	Always Running Timer Value 31:0 (ARTV_63_32)	00000000h
1210h	4	Timed GPIO Control 0 (TGPIOCTL0)	00000000h
1220h	4	Timed GPIO 0 Comparator Value 31:0 (TGPIOCOMPV0_31_0)	00000000h
1224h	4	Timed GPIO Comparator Value 63:32 (TGPIOCOMPV0_63_32)	00000000h
1228h	4	Timed GPIO0 Periodic Interval Value 31_0 (TGPIOPIV0_31_0)	00000000h
122Ch	4	Timed GPIO 0 Periodic Interval Value 63_32 (TGPIOPIV0_63_32)	00000000h
1230h	4	Timed GPIO Time Capture Register 31_0 (TGPIOTCV0_31_0)	00000000h
1234h	4	Timed GPIO0 Time Capture Register 63_32 (TGPIOTCV0_63_32)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1238h	4	Timed GPIO0 Event Counter Capture Register 31_0 (TGPIOECCV0_31_0)	00000000h
123Ch	4	Timed GPIO0 Event Counter Capture Register 63_32 (TGPIOECCV0_63_32)	00000000h
1240h	4	Timed GPIO0 Event Counter Register 31_0 (TGPIOEC0_31_0)	00000000h
1244h	4	Timed GPIO0 Event Counter Register 63_32 (TGPIOEC0_63_32)	00000000h
1310h	4	Timed GPIO Control 1 (TGPIOCTL1)	00000000h
1320h	4	Timed GPIO 1 Comparator Value 31:0 (TGPIOCOMPV1_31_0)	00000000h
1324h	4	Timed GPIO Comparator Value 63:32 (TGPIOCOMPV1_63_32)	00000000h
1328h	4	Timed GPIO1 Periodic Interval Value 31_0 (TGPIOPIV1_31_0)	00000000h
132Ch	4	Timed GPIO 1 Periodic Interval Value 63_32 (TGPIOPIV1_63_32)	00000000h
1330h	4	Timed GPIO Time Capture Register 31_0 (TGPIOTCV1_31_0)	00000000h
1334h	4	Timed GPIO Time Capture Register 63_32 (TGPIOTCV1_63_32)	00000000h
1338h	4	Timed GPIO0 Event Counter Capture Register 31_0 (TGPIOECCV1_31_0)	00000000h
133Ch	4	Timed GPIO0 Event Counter Capture Register 63_32 (TGPIOECCV1_63_32)	00000000h
1340h	4	Timed GPIO1 Event Counter Register 31_0 (TGPIOEC1_31_0)	00000000h
1344h	4	Timed GPIO Event Counter Register 63_32 (TGPIOEC1_63_32)	00000000h
150Ch	4	Catastrophic Trip Point Enable (CTEN)	00000001h
1510h	4	EC Thermal Sensor Reporting Enable (ECRPTEN)	00000000h
1520h	4	Throttle Level (TL)	0FF3FCFFh
1528h	4	Throttle Levels Enable (TLEN)	00000000h
1530h	4	Thermal Sensor Alert High Value (TSAHV)	000000FFh
1534h	4	Thermal Sensor Alert Low Value (TSALV)	00000000h
1538h	4	Thermal Alert Trip Status (TAS)	00000000h
1540h	4	PCH Hot Level Control (PHLC)	00000000h
1560h	4	Temperature Sensor Control and Status (TSS0)	00000000h
1800h	4	Wake Alarm Device Timer: AC (WADT_AC)	FFFFFFFFh
1804h	4	Wake Alarm Device Timer: DC (WADT_DC)	FFFFFFFFh
1808h	4	Wake Alarm Device Expired Timer: AC (WADT_EXP_AC)	FFFFFFFFh
180Ch	4	Wake Alarm Device Expired Timer: DC (WADT_EXP_DC)	FFFFFFFFh
1810h	4	Power and Reset Status (PRSTS)	00000000h
1818h	4	Power Management Configuration Reg 1 (PM_CFG)	00000020h
1828h	4	S3 Power Gating Policies (S3_PWRGATE_POL)	00000000h
182Ch	4	S4 Power Gating Policies (S4_PWRGATE_POL)	00000000h
1830h	4	S5 Power Gating Policies (S5_PWRGATE_POL)	00000000h
1834h	4	DeepSx Configuration (DSX_CFG)	00000000h
183Ch	4	Power Management Configuration Reg 2 (PM_CFG2)	08000000h
18C8h	4	PM_SYNC Miscellaneous Configuration (PM_SYNC_MISC_CFG)	00000000h
18E0h	4	Power Management Configuration Reg 3 (PM_CFG3)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
18E8h	4	Power Management Configuration Reg 4 (PM_CFG4)	00000000h
18ECh	4	CPU Early Power-on Configuration (CPU_EPOC)	00000000h
18FCh	4	ACPI Timer Control (ACPI_TMR_CTL)	00000000h
1910h	4	Last TSC Alarm Value[31:0] (TSC_ALARM_LO)	00000000h
1914h	4	Last TSC Alarm Value[63:32] (TSC_ALARM_HI)	00000000h
1920h	4	GPIO Configuration (GPIO_CFG)	00000432h
1930h	4	Latency Limit Residency 0 (LAT_LIM_RES_0)	00000000h
1934h	4	Latency Limit Residency 1 (LAT_LIM_RES_1)	00000000h
1938h	4	Latency Limit Residency 2 (LAT_LIM_RES_2)	00000000h
193Ch	4	SLP_S0 Residency (SLP_S0_RESIDENCY)	00000000h
1940h	4	Latency Limit Control (LATENCY_LIMIT_CONTROL)	00000000h
1A78h	4	DBG SLP S0 WAKE1 (DBG_SLP_S0_WAKE1)	00000000h
1A7Ch	4	DBG SLP S0 WAKE2 (DBG_SLP_S0_WAKE2)	00000000h
1BD4h	4	CWB MDID Status Register (CWBMDIDSTATUS)	00000000h
1BD8h	4	ACPI Control (ACTL)	00000000h
1BECh	4	Clock Source Shutdown Control Reg 2 (CS_SD_CTL2)	00000000h
1D80h	4	PGD PG_ACK Status Register 0 (PPASR0)	00000000h
1D84h	4	PGD PG_ACK Status Register 1 (PPASR1)	00000000h
1D90h	4	PGD PFET Enable Ack Status Register 0 (PPFEAR0)	00000000h
1D94h	4	PGD PFET Enable Ack Status Register 1 (PPFEAR1)	00000000h
1E20h	4	Static PG Related Function Disable Register 1 (ST_PG_FDIS_PMC_1)	00000000h
1E24h	4	Static Function Disable Control 2 Register (ST_PG_FDIS_PMC_2)	00000000h
1E28h	4	Non-Static PG Related Function Disable Register 1 (NST_PG_FDIS_1)	00000000h
1E40h	4	Non-Static PG Fuse Disable Read 1 Register (N_STPG_FUSE_SS_DIS_RD_1)	00000000h
1E44h	4	Static PG Fuse and Soft Strap Disable Read Register 2 (STPG_FUSE_SS_DIS_RD_2)	00000000h
1E4Ch	4	CPPMVRIC3 CPPM VR Idle Control 3 (CPPMVRIC3)	00000001h

4.2.1 General PM Configuration A (GEN_PMCON_A) — Offset 1020h

Usage ACPI, Legacy. Available Desktop, Mobile.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1020h	20014000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RW	**DC PHY Power Disable (DC_PP_DIS):** This bit determines the Host software contribution to whether the LAN PHY remains powered in Sx/MOFF or DeepSx while on battery. See the SLP_LAN# sub-section later in the chapter for more information.
29	1h RW	**Deep-Sx PHY Power Disable (DSX_PP_DIS):** This bit determines the Host software contribution to whether the LAN PHY remains powered in DeepSx. See the SLP_LAN# sub-section later in the chapter for more information. If this bit is cleared, for the PHY to be powered in deep-Sx state, SX_PP_EN must be set to 1.
28	0h RW	**After G3 PHY Power Enable (AG3_PP_EN):** This bit determines the Host software contribution to whether the LAN PHY is powered up after exiting G3 (to either Sx/MOFF or DeepSx). See the SLP_LAN# sub-section later in the chapter for more information.
27	0h RW	**Sx PHY Power Enable (SX_PP_EN):** This bit determines the Host software contribution to whether the LAN PHY remains powered in an Sx/MOFF state that was entered from S0 (rather than from G3). See the SLP_LAN# sub-section later in the chapter for more information.
26:25	0h RO	**Reserved**
24	0h RW/1C/V	**Global Reset Status (GBL_RST_STS):** This bit is set after a global reset (not G3 or DeepSx) occurs. See the GEN_PMCON_B.HOST_RST_STS bit for potential usage models.
23	0h RW	**DRAM Initialization Scratchpad Bit (DISB):** This bit does not effect hardware functionality in any way. It is provided as a scratchpad bit that is maintained through main power well resets and CF9h-initiated resets. BIOS is expected to set this bit prior to starting the DRAM initialization sequence and to clear this bit after completing the DRAM initialization sequence. BIOS can detect that a DRAM initialization sequence was interrupted by a reset by reading this bit during the boot sequence. If the bit is 1, then the DRAM initialization was interrupted. This bit is reset by the assertion of the RSMRST# pin.
22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO/V	**Memory Placed in Self-Refresh (MEM_SR):** This bit will be set to 1 if DRAM should have remained powered and held in Self-Refresh through the last power state transition (i.e. the last time the system left S0). The scenarios where this should be the case are: - successful S3 entry & exit - successful Host partition reset without power cycle These scenarios both involve a handshake between the PCH and the CPU/MCH. The acknowledge from the CPU/MCH back to the PCH is assumed to imply that memory was successfully placed into Self-Refresh (the PCH has no way to verify whether that actually occurred). This bit will be cleared whenever the PCH begins a transition out of S0. Note: This bit should not be consulted upon wake from S1, as that state does not involve the same type of handshake or placing memory into Self-Refresh. It is assumed that software is already aware that memory context is not impacted by S1 and therefore does not need to check this bit.
20:19	0h RO	**Reserved**
18	0h RW/1C/V	**Minimum SLP_S4# Assertion Width Violation Status (MS4V):** Hardware sets this bit when the SLP_S4# assertion width is less than the time programmed in the SLP_S4# Minimum Assertion Width field (D31.F0.A4h.5:4). The PCH begins the timer when SLP_S4# pin (including ME override logic) is asserted during S4/S5 entry, or when the pri_pwrgood_rst_b input is deasserted during SUS well power-up. The status bit is cleared by software writing a 1 to the bit. Note that this bit is functional regardless of the value in the SLP_S4# Assertion Stretch Enable and the Disable SLP_X Stretching After SUS Power Failurebits. This bit is reset by the assertion of the pri_pwrgood_rst_b pin, but can be set in some cases before the default value is readable.
17	0h RO	**Reserved**
16	1h RW/1C	**SUS Well Power Failure (SUS_PWR_FLR):** This bit is set to '1' whenever SUS well power is lost, as indicated by RSMRST# assertion. Software writes a 1 to this bit to clear it.
15	0h RW	**PME B0 S5 Disable (PME_B0_S5_DIS):** When set to '1', this bit blocks wake events from PME_B0_STS in S5, regardless of the state of PME_B0_EN. When cleared (default), wake events from PME_B0_STS are allowed in S5 if PME_B0_EN = '1'. Wakes from power states other than S5 are not affected by this policy bit. The net effect of setting PME_B0_S5_DIS = '1' is described by the truth table below: Y = Wake N = Don't wake B0 = PME_B0_EN OV = WOL Enable Override B0/OV | S1/S3/S4 | S5 00 | N | N 01 | N | Y (LAN only) 11 | Y (all PME B0 sources) | Y (LAN only) 10 | Y (all PME B0 sources) | N This bit is cleared by the rtc_pwrgood_rst_b pin.
14	1h RW/1C	**PF:** 1 = Indicates that the trickle current (from the main battery or trickle supply) was removed or failed. 0 = Indicates that the trickle current has not failed since the last time the bit was cleared. Software writes a 1 to this bit to clear it. This bit is in the DSW well, and defaults to '1' based on dsw_pwrgood_rst_b deassertion (not cleared by any type of reset). Implementation Note: dsw_pwrgood_rst_b is an asynchronous set term to this bit.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**Reserved**
12	0h RW/L	**Disable SLP_X Stretching After SUS Well Power Up (DIS_SLP_X_STRCH_SUS_UP):** When this bit is set to 1, all SLP_* pin stretching is disabled when powering up after a SUS well power loss. When this bit is left at 0, SLP_* stretching will be performed after SUS power failure as enabled in various other fields. Note that if this bit is a 0, SLP_* stretch timers start on SUS well power up (the PCH has no ability to count stretch time while the SUS well is powered down). Setting this bit can therefore prevent long delays after SUS power loss which may be common in mobile platforms and in manufacturing flow testing, while still allowing for the full power cycling during S3, S4 and S5 states. If the platform guarantees minimum SUS power down residence in other ways, an additional PCH-induced delay is not needed or wanted. Note: This policy bit has a different effect on SLP_SUS# stretching than on the other SLP_* pins, since SLP_SUS# is the control signal for one of the scenarios where SUS well power is lost (DeepSx). The effect of setting this bit to '1' on: - SLP_S3#, SLP_S4#, SLP_A# and SLP_LAN# stretching: disabled after any SUS power loss - SLP_SUS# stretching: disabled after G3, but no impact on DeepSx This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. This bit is cleared by the rtc_pwrgood_rst_b pin. **Locked by:** GEN_PMCON_B.SLPSX_STR_POL_LOCK
11:10	0h RW/L	**SLP_S3# Minimum Assertion Width (SLP_S3_MIN_ASST_WDTH):** This 2-bit value indicates the minimum assertion width of the SLP_S3# signal to guarantee that the Main power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power failure detection circuits, etc. Settings are: 00: 60 usec 01: 1 ms 10: 50 ms 11: 2 sec This field is not writable when the SLP_Sx# Stretching Policy Lock- Down bit is set. This bit is cleared by the pri_pwrgood_rst_b pin. **Locked by:** GEN_PMCON_B.SLPSX_STR_POL_LOCK
9	0h RW/1C/V	**Host Reset Status (HOST_RST_STS):** This bit is set by hardware when a host partition reset (not a global reset, DeepSx, or G3) occurs. This bit is an optional tool to help BIOS determine when a host partition reset might have collided with a wake from a valid sleep state. A possible usage model would be to consult and then write a '1' to clear this bit during the boot flow before determining what action to take based on reading PM1_STS.WAK_STS = '1'. If HOST_RST_STS = '1' and/or GEN_PMCON_A.GBL_RST_STS = '1', the cold reset boot path could be followed rather than the resume path, regardless of the setting of WAK_STS. This bit does not affect PCH operation in any way, and can therefore be left set if BIOS chooses not to use it.
8	0h RW/L	**ESPI SMI Lock (ESPI_SMI_LOCK):** When this bit is set, writes to the ESPI_SMI_EN bit will have no effect. Once the ESPI_SMI_LOCK bit is set, writes of 0 to ESPI_SMI_LOCK bit will have no effect (i.e. once set, this bit can only be cleared by host_prim_rst_b). **Locked by:** GEN_PMCON_A.ESPI_SMI_LOCK

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RW	**SWSMI Rate Select (SWSMI_RATESEL):** This 2-bit value indicates when the SWSMI timer will time out. Valid values are: 00 1.5ms +/- 0.6ms 01 16ms +/- 4ms 10 32ms +/- 4ms 11 64ms +/- 4ms These bits are not cleared by any type of reset except rtc_pwrgood_rst_b.
5:4	0h RW/L	**SLP_S4# Minimum Assertion Width (S4MAW):** This 2-bit value indicates the minimum assertion width of the SLP_S4# signal to guarantee that the DRAMs have been safely power-cycled. This value may be modified per platform depending on DRAM types, power supply capacitance, etc. Valid values are: 11: 1 second 10: 2 seconds 01: 3 seconds 00: 4 seconds This value is used in two ways: 1. If the SLP_S4# assertion width is ever shorter than this time, a status bit (D31.F0.A2h.2) is set for BIOS to read when S0 is entered 2. If enabled by bit 3 in this register, the hardware will prevent the SLP_S4# signal from deasserting within this minimum time period after asserting. Note that the logic that measures this time is in the suspend power well. Therefore, when leaving a G3 or DeepSx state, the minimum time is measured from the deassertion of the internal suspend well reset (unless the Disable SLP_X Stretching After SUS Power Failurebit is set). This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. rtc_pwrgood_rst_b forces this field to the conservative default state (00b). **Locked by:** GEN_PMCON_B.SLPSX_STR_POL_LOCK
3	0h RW/L	**SLP_S4# Assertion Stretch Enable (S4ASE):** When set to 1, the SLP_S4# pin (which includes the ME override logic) will minimally assert for the time specified in bits 5:4 of this register. When 0, the minimum assertion time for SLP_S4# is the same as the timing defined in the timing tables in Default 16.6.3. This bit is provided so that all DIMMs in the system can deterministically detect a power-cycle event for proper initialization. Note that there are behavioral changes that may be noticeable to the end-user when this bit is set. Resume times from S4 and S5 and power-up times from G3 or DeepSx may be delayed by several seconds. Cases in which this feature may not be desirable and therefore keeping the bit cleared are: A customer decides the user confusion due to the hardware delay is a bigger issue than the potential DRAM issue A customer decides the software status bit solution is adequate A different DRAM type is used or the platform provides an external solution to solve the power-cycling issue Validation regressions are impacted by the delay (especially after pri_pwrgood_rst_b deassertion) Avoid potential resume time WHQL violations This bit is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. This bit is cleared by rtc_pwrgood_rst_b. **Locked by:** GEN_PMCON_B.SLPSX_STR_POL_LOCK
2:1	0h RW	**Period SMI Select (PER_SMI_SEL):** Software sets these bits to control the rate at which the periodic SMI# is generated: 00 = 64 seconds (default), 01 = 32 seconds, 10 = 16 seconds, 11 = 8 seconds Tolerance for the timer is +/- 1 second.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**AG3E:** Determines what state to go to when power is reapplied after a power failure (G3 state). 0 = System will return to an S0 state (boot) after power is re-applied. 1 = System will return to the S5 state (except if it was in S4, in which case it will return to S4-like state). In the S5 state, the only enabled wake-up event is the Power Button or any enabled wake event that was preserved through the power failure. This bit is in the RTC well and is only cleared by rtc_pwrgood_rst_b assertion.

4.2.2 General PM Configuration B (GEN_PMCON_B) — Offset 1024h

General PM configuration B

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1024h	00000004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW/L	**SLP_Sx# Stretching Policy Lock-Down (SLPSX_STR_POL_LOCK):** When set to 1, this bit locks down the following fields: - GEN_PMCON_3.DIS_SLP_X_STRCH_SUSPF - GEN_PMCON_3.SLP_S3_MIN_ASST_WDTH - GEN_PMCON_3.S4MAW - GEN_PMCON_3.S4ASE - PM_CFG.SLP_A_MIN_ASST_WDTH - PM_CFG.SLP_LAN_MIN_ASST_WDTH - PM_CFG.PWR_CYC_DUR Those bits become read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a platform reset. This lockdown bit is available in both desktop and mobile. **Locked by:** GEN_PMCON_B.SLPSX_STR_POL_LOCK
17:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**WOL Enable Override (WOL_EN_OVRD):** When this bit is set to 1, the integrated LAN is enabled to wake the system from S5 regardless of the value in the PME_B0_EN bit in the GPE0_EN register. This allows the system BIOS to enable Wake-On-LAN regardless of the policies selected through the operating system. This bit is maintained in the RTC power well, therefore permitting WOL following a surprise power failure even in cases in which the system may have been running in S0 without the PME Enables set. (Note that the LAN NVRAM configuration must support WOL after SUS power loss.) When this bit is cleared to 0, the wake-on-LAN policies are determined by OS-visible bits. This bit has no effect on wakes from S1, S3, or S4. This bit is cleared by the rtc_pwrgood_rst_b pin
12:11	0h RO	**Reserved**
10	0h RW	**BIOS PCI Express Enable (BIOS_PCI_EXP_EN):** This bit acts as a global enable for the SCI associated with the PCI express ports. If this bit is not set, then the various PCI Express ports and MCH cannot cause the PCI_EXP_STS bit to go active.
9	0h RO/V	**Power Button Level (PWRBTN_LVL):** This read-only bit indicates the current state of the PWRBTN# signal. 1= High, 0 = Low. The value reflected in this bit is dependent upon PM_CFG1.PB_DB_MODE. The PB_DB_MODE bit's value causes the following behavior: - '0': PWRBTN_LVL is taken from the debounced PWRBTN# pin value that is seen at the output of a 16ms debouncer. - '1': PWRBTN_LVL is taken from the raw PWRBTN# pin (before the debouncer).
8	0h RW	**T32a Bypass Enable (T32A_BYPASS_EN):** When set to '1', the full t32a timing will only be counted on the first boot after an RTC power-loss. When '0', t32a will be will be counted on every boot after a G3. Note: If the t32a_bypass pin-strap is set, t32a is never counted and this bit has no effect.
7:5	0h RO	**Reserved**
4	0h RW/L	**SMI Lock (SMI_LOCK):** When this bit is set, writes to the GLB_SMI_EN bit will have no effect. Once the SMI_LOCK bit is set, writes of 0 to SMI_LOCK bit will have no effect (i.e. once set, this bit can only be cleared by host_prim_rst_b). **Locked by:** GEN_PMCON_B.SMI_LOCK
3	0h RO	**Reserved**
2	1h RW	**RPS:** Intel PCH will set this bit to 1 when rtc_pwrgood_rst_b indicates a weak or missing battery. The bit will remain set until the software clears it by writing a 0 back to this bit position. This bit is not cleared by any type of reset.
1:0	0h RO	**Reserved**

4.2.3 Configured Revision ID (CRID) — Offset 1030h

Configured revision ID Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1030h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**CRID Lock (CRID_LK):** BIOS writes to this bit to lock this register (a specific lock bit is preferable over a write-based self-lock for the RID_SEL field). When this bit is written to 1, the entire register becomes RO (writes have no effect, reads return actual value) until the next assertion of host_prim_rst_b. **Locked by:** CRID.CRID_LK
30:2	0h RO	**Reserved**
1:0	0h RW/L	**RID Select(RID_SEL) (RID_SEL):** Software writes this field to select the fuse sets reflected in PCI config space Revision ID. The decoding is: 00 - Revision ID 01 - CRID 0 10 - CRID 1 11 - CRID 2 Once written, this field can only be cleared by a reset. reset_type = host_prim_rst_bDeepRst-BIOS wr all boots, (HOST_RST/platform reset when arch available.) (setid multicast sends this out) . **Locked by:** CRID.CRID_LK

4.2.4 Extended Test Mode Register 3 (ETR3) — Offset 1048h

This register resides in the primary well. All bits except bit[23:16] are reset by host_deep_rst_b. Bit[23:16] are reset by pri_pwrgood_rst_b only.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V/L	**CF9h Lockdown (CF9LOCK):** When set, this will lock the CF9h Global Resetbit. When set, this register locks itself. This register is reset by a CF9h reset. **Locked by:** ETR3.CF9LOCK
30	0h RW/V	**Reserved**
29	0h RW	**Reserved**
28	0h WO	**Reserved**
27:21	0h RO	**Reserved**
20	0h RW/L	**CF9h Global Reset (CF9GR):** When this bit is set, a CF9h write of 6h or Eh will cause a Global Reset of both the Host and the ME partitions. If this bit is cleared, a CF9h write of 6h or Eh will only reset the Host partition. It is recommended that BIOS should set this bit early on in the boot sequence, and then clear it and set the CF9LOCK bit prior to loading the OS in both an ME Enabled and a ME Disabled system. When this bit is set, the hardware assumes that bit 18 (CF9h Without Resume Well Reset Enable) is cleared. This register is locked by the CF9 Lockdown (CF9LOCK) bit. This register is not reset by a CF9h reset. **Locked by:** ETR3.CF9LOCK
19:0	0h RO	**Reserved**

4.2.5 SET STRAP MSG LOCK (SSML) — Offset 104Ch

SET STRAP MSG LOCK

Type	Size	Offset	Default
MMIO	32 bit	BAR + 104Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/L	**Set_Strap Lock (SSL):** When set to 1, all of SSML, SSMC and SSMD is locked, including this Lock bit. Note that this bit is reset on host partition reset **Locked by:** SSML.SSL

4.2.6 SET STRAP MSG CONTROL (SSMC) — Offset 1050h

SET STRAP Message Control

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/L	**Set_Strap Mux Select (SSMS):** When set to 1, the Set strap message bits [47:32] come from the Set_Strap Msg Data register. This bit is reset by the RSMRST# pin only. When 0, the Set-Strap data continues to come from the soft straps themselves.This register field is locked by the Set Strap Lock (SSML.SSL) bit. **Locked by:** SSML.SSL

4.2.7 SET STRAP MSG DATA (SSMD) — Offset 1054h

This register is used to provide a BIOS programmable sticky register which contains data that will be used in the Set-Strap type 1 msg on subsequent resets. The bits in the message control certain CPU features, for which see the CPU spec. These bits are in the resume well, so only reset on G3. The usage model is that on each reset BIOS will check the state of the CPU. If the state is correct, then BIOS continues. If not, then BIOS writes the SSMD and SSMC registers and does a CF9 reset. On the reset the value of what was written to SSMD takes effect. Note that some mobile platforms force G3 on

S5 requests. For those platforms, if the user/BIOS wants to have these bits set, there will be 2 resets on every power-on. If the platform accepts the default of 0 for these controls, then there is only one reset. The bits are in DSW and not RTC well because this allows a user upgrade, assuming the user unplugged the system before doing the upgrade, to revert to a setting of 0. This should reduce any interoperability concerns regarding user upgrades. The DSW bits are all cleared dsw_pok, and must not be cleared by CF9h resets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/L	**Set_Strap DATA (SSD):** When SSMS is 1, then this data is sent in the Set-Strap msg Type 1 upon reset. This data is sent i//n the 2nd DW of data, bits 15:0. This register field is locked by the Set Strap Lock SSML.SSL bit. **Locked by:** SSML.SSL

4.2.8 Configured Revision ID (CRID_UIP) — Offset 10B0h

Configured revision ID Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/V	**CRID Update in Progress (CRID_UIP):** PMC HW sets this bit to indicate that SetID broadcast flow has been requested by BIOS. This bit is cleared by PMC FW only when the completion/s for the multicast non-posted SetIDVal message is received by PMC. BIOS is required to read this bit as cleared before writing to the CRID register (to request a CRID update). BIOS is also required to poll on reads to this bit until it sees the bit as cleared after BIOS has written to the CRID register. 0 Any previously requested CRID Update is complete. 1 the most recently requested CRID update is still in progress.

4.2.9 SLP S0 DEBUG REG0 (SLP_S0_DBG_0) — Offset 10B4h

This register captures the state of low power events involved in SLP_S0# entry to assist with debug. The status is captured as part of C10 entry (once CPU has entered package C10) or it can be captured by writing a 1 to LATCH_SLPS0_EVENTS bit in this register.Note that static or function disable status of the IP is incorporated in the individual status register bits though overrides / masks in CPPMVRIC* registers does not impact the value reflects in this register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Latch SLP_S0#events (LATCH_SLPS0_EVENTS):** When this bit is written to 1, the current state of SLP_S0# events is latched and captured in SLP_S0_DEBUG_REGx registers. A write of 0 has no effect though it is necessary to clear this register before writing a 1 to latch events the next time. Note that writes to this register will bring CPU out of C10 and wake PLLs in the PCH so its usage is limited to looking at certain low power entry events that are not affected by writes to this register.
30:9	0h RO	**Reserved**
8	0h RO/V	**EMMC_D3_STS:** This bit when 1 indicates that eMMC controller is in D3 state (taking static/function disables into account as well)
7	0h RO/V	**Reserved**
6	0h RO/V	**Reserved**
5	0h RO/V	**SATA_D3_STS:** This bit when 1 indicates that SATA controller is in D3 state (taking static/function disables into account as well)

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO/V	**SDX_D3_STS:** This bit when 1 indicates that SDX controller is in D3 state (taking static/function disables into account as well)
3	0h RO/V	**LPIO_D3_STS:** This bit when 1 indicates that LPIO controller is in D3 state (taking static/function disables into account as well)
2	0h RO/V	**XHCI_D3_STS:** This bit when 1 indicates that XHCI controller is in D3 state (taking static/function disables into account as well)
1	0h RO/V	**OTG_D3_STS:** This bit when 1 indicates that OTG controller is in D3 state (taking static/function disables into account as well)
0	0h RO/V	**AUDIO_D3_STS:** This bit when 1 indicates that Audio DSP controller is in D3 state (taking static/function disables into account as well)

4.2.10 SLP S0 DEBUG REG1 (SLP_S0_DBG_1) — Offset 10B8h

This register captures the state of low power events involved in SLP_S0# entry to assist with debug. The status is captured as part of C10 entry (once CPU has entered package C10) or it can be captured by writing a 1 to LATCH_SLPS0_EVENTS bit in SLP_S0_DEBUG_REG0 register.Note that static or function disable status of the IP is incorporated in the individual status register bits though overrides / masks in CPPMVRIC* registers does not impact the value reflects in this register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RO/V	**IOTG PLL OFF Status (IOTG_PLL_OFF_STS):** This bit when 1 indicates that IOTG PLL is off
12	0h RO/V	**CLKACK_STS:** This bit when 1 indicates that all CLKACKs have deasserted following graceful_park request from PMC
11	0h RO/V	**AON2 Ring Oscillator clock gated status (AON2_ROSC_GATED_STS):** This bit when 1 indicates that AON2 partition ring oscillator clocks are gated.
10	0h RO/V	**PMC ROSC SWITCH status (PMC_ROSC_SWITCH_STS):** This bit when 1 indicates that PMC has switched from fast to slow ring oscillator clock
9	0h RO/V	**HPET XOSC CLKREQ status (HPET_XOSC_CLKREQ_STS):** This bit when 1 indicates that HPETs crystal CLKREQ is requesting clock.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO/V	**AUDIO RING OSC status (AUDIO_ROSC_OFF_STS):** This bit when 1 indicates that the audio ring oscillator is off.
7	0h RO/V	**PCIe external CLKREQs deasserted (PCIE_CLKREQS_OFF_STS):** This bit when 1 indicates that all external PCIe clock request pins are inactive
6	0h RO/V	**LPC output clocks gated status (LPC_CLKS_GATED_STS):** This bit when 1 indicates that external LPC clocks are gated.
5	0h RO/V	**Crystal OFF Status (XOSC_OFF_STS):** This bit when 1 indicates that crystal oscillator has shut down.
4	0h RO/V	**ISCLK Main PLL OFF Status (MAIN_PLL_OFF_STS):** This bit when 1 indicates that main PLL is off
3	0h RO/V	**ISCLK OCPLL OFF Status (OC_PLL_OFF_STS):** This bit when 1 indicates that OC PLL is off
2	0h RO/V	**Audio PLL OFF Status (AUDIO_PLL_OFF_STS):** This bit when 1 indicates that Audio PLL is off
1	0h RO/V	**USB2 PLL OFF Status (USB2_PLL_OFF_STS):** This bit when 1 indicates that USB2 PLL is off
0	0h RO/V	**SDIO PLL OFF Status (SDIO_PLL_OFF_STS):** This bit when 1 indicates that SDIO PLL is off

4.2.11 SLP S0 DEBUG REG2 (SLP_S0_DBG_2) — Offset 10BCh

This register captures the state of low power events involved in SLP_S0# entry to assist with debug. The status is captured as part of C10 entry (once CPU has entered package C10) or it can be captured by writing a 1 to LATCH_SLPS0_EVENTS bit in SLP_S0_DEBUG_REG0 register.Note that static or function disable status of the IP is incorporated in the individual status register bits though overrides / masks in CPPMVRIC* registers does not impact the value reflects in this register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10BCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14	0h RO/V	**PMC ARC PG Ready IDLE (PMC_ARC_IDLE_STS):** This bit when 1 indicates that the PMCs ARC microcontroller is ready for power gating
13	0h RO/V	**Platform ASLT greater than threshold Status (ASLT_GT_THRES_STS):** This bit when 1 indicates that the platform ASLT is greater than threshold
12	0h RO/V	**PM_SYNC States Inactive (PMSYNC_STATE_IDLE_STS):** This bit when 1 indicates that PMSYNC requests are not active.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO/V	**Reserved**
10	0h RO/V	**CNV VNN REQ Status (CNV_VNN_REQ_STS):** This bit when 1 indicates that CNV VNN Req is active.
9	0h RO/V	**CNV VNN AON REQ Status (CNV_VNNAON_REQ_STS):** This bit when 1 indicates that CNV VNNAON Req is active.
8	0h RO/V	**ISH VNN REQ Status (ISH_VNN_REQ_STS):** This bit when 1 indicates that ISH Vnn Req is active.
7	0h RO/V	**ISH VNN AON REQ Status (ISH_VNNAON_REQ_STS):** This bit when 1 indicates that ISH VnnAON Req is active.
6	0h RO/V	**PCIe Low Power Status (PCIE_LP_STS):** This bit when 1 indicates that all PCIe root port controllers are in their low power state.
5	0h RO/V	**Thermal Sensor Disabled Status (TS_DIS_STS):** This bit when 1 indicates that the thermal sensor is disabled
4	0h RO/V	**GBE No Link Status (GBE_NO_LINK_STS):** This bit when 1 indicates that the GBE interface is disconnected.
3	0h RO/V	**Dynamic Flex IO Status (DYNAMIC_FLEX_IO_STS):** This bit when 1 indicates that Dynamic FLEX IO change is not in progress.
2	0h RO/V	**USB2 SUS Power Gated Status (USB2_SUS_PG_STS):** This bit when 1 indicates that USB2 PHY SUS power domain is off.
1	0h RO/V	**CSME Power Gated Status (CSME_PG_STS):** This bit when 1 indicates that all power gated domains in CSME are turned off.
0	0h RO/V	**MHPY CORE Power Gated Status (MPHY_CORE_PG_STS):** This bit when 1 indicates that mphy core and data lanes are off.

4.2.12 ModPHY Power Management Configuration Reg 1 (MODPHY_PM_CFG1) — Offset 10C0h

This register contains misc. fields used to configure the PCH's power management behavior with respect to the modPHY

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
11:0	000h RW	**ModPHY Lane S0 SUS Well Power Gating Policy [11:0] (MLS0SWPGP):** This is a bit per lane that controls SUS Well Power Gating for a ModPHY lane to be used for S0 and S0ix use models. Bit 0: Corresponds to ModPHY Lane 0 Bit 1: Corresponds to ModPHY Lane 1 Bit 2: Corresponds to ModPHY Lane 2 : : Bit 11: Corresponds to ModPHY Lane 11 For each lane: 0: Lane power gating not permitted in S0. 1: Lane power gating is permitted in S0. Note that strap information/PCIe Lane reversal information will be factored by BIOS when programming these bits in the configuration registers. Note that it is illegal SW programming to have a bit location to be 1 in this field and the corresponding bit position to be 0 in MLSXSWPGP

4.2.13 ModPHY Power Management Configuration Reg 2 (MODPHY_PM_CFG2) — Offset 10C4h

This register contains misc. fields used to configure the PCH's power management behavior with respect to the modPHY

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10C4h	00000FFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
11:0	FFFh RW	**ModPHY Lane Sx SUS Well Power Gating Policy [11:0] (MLSXSWPGP):** This is a bit per lane that controls SUS Well Power Gating for a ModPHY lane when system is in Sx. Bit 0: Corresponds to ModPHY Lane 0 Bit 1: Corresponds to ModPHY Lane 1 Bit 2: Corresponds to ModPHY Lane 2 : : Bit 11: Corresponds to ModPHY Lane 11 For each lane: 0: Lane power gating not permitted in Sx. 1: Lane power gating is permitted in Sx. Note that strap information/PCIe Lane reversal information will be factored by BIOS when programming these bits in the configuration registers. For ease of PMC implementation, this field will be used to manage Sx policies even in S0. In other words, the earlier restriction that BIOS does not have to program this field if MLSPDDGE is 1 does not apply any more. BIOS shall set this field appropriately for all cases.

4.2.14 ModPHY Power Management Configuration Reg 3 (MODPHY_PM_CFG3) — Offset 10C8h

This register contains misc. fields used to configure the PCH's power management behavior with respect to the modPHY.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RW	**ModPHY Lane SUS Power Domain Dynamic Gating Enable (MLSPDDGE):** When this bit is set to 1, ModPHY Lane SUS Well Dynamic Gating is enabled. When this bit is 0, ModPHY Lane SUS Well Gating can still be done at a more coarse level using MLSXSWPGP and MLS0SWPGP fields.
29:2	0h RO	**Reserved**
1	0h RW	**ModPHY Per-Lane SUS Power Domain Dynamic Gating Enable (MPLSPDDGE):** When this bit is set to 1, ModPHY Per-Lane SUS Well Dynamic Gating is enabled. When this bit is 0, if modPHY lane SUS power domain dynamic gating is enabled, all lanes are gated/ungated together. This bit has no impact if modPHY lane SUS power domain dynamic gating is disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**C10 Qualifier for MPHY Power Gating (C10_QUAL_MPHYPG):** C10 qualification for MPHY power gating, 1: C10 is not required for mPHY Sus power gating 0: C10 is required for mPHY Sus power gating

4.2.15 ModPHY Power Management Configuration Reg 4 (MODPHY_PM_CFG4) — Offset 10CCh

This register contains misc. fields used to configure the PCH's power management behavior with respect to the modPHY

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**ASL Over-rides [26:0] (ASLOR):** This field provides ASL code to take over SPD power gating control. If ASL code sets a bit corresponding to a controller, it implies that PMC shall ignore any other inputs from that controller and assume that the controller is ready for SPD power gating. 0 in a bit position: Use HW interfaces for the controller to manage SPD gating/wake-up. 1 in a bit position: Ignore HW interfaces for the controller, rely only on MSPDRTReq field thats managed by ASL code. Bit 0: Corresponds to PCIe Controller A, Function 0 Bit 1: Corresponds to PCIe Controller A, Function 1 Bit 2: Corresponds to PCIe Controller A, Function 2 Bit 3: Corresponds to PCIe Controller A, Function 3 Bit 4: Corresponds to PCIe Controller B, Function 0 Bit 5: Corresponds to PCIe Controller B, Function 1 Bit 6: Corresponds to PCIe Controller B, Function 2 Bit 7: Corresponds to PCIe Controller B, Function 3 Bit 8: Corresponds to PCIe Controller C, Function 0 Bit 9: Corresponds to PCIe Controller C, Function 1 Bit 10: Corresponds to PCIe Controller C, Function 2 Bit 11: Corresponds to PCIe Controller C, Function 3 Bit 12: Corresponds to SATA Controller Bit 13: Corresponds to Gbe Controller Bit 14: Corresponds to xHCI Controller Bit 15: Corresponds to xDCI Controller Bit 16: Reserved Bit 17: Corresponds to PCIe Controller D, Function 0 Bit 18: Corresponds to PCIe Controller D, Function 1 Bit 19: Corresponds to PCIe Controller D, Function 2 Bit 20: Corresponds to PCIe Controller D, Function 3 Bit 21: Corresponds to PCIe Controller E, Function 0 Bit 22: Corresponds to PCIe Controller E, Function 1 Bit 23: Corresponds to PCIe Controller E, Function 2 Bit 24: Corresponds to PCIe Controller E, Function 3 Bit 25: Corresponds to DMI Controller Bit 26: Reserved Bit 27: Corresponds to PCIe Controller F, Function 0 Bit 28: Corresponds to PCIe Controller F, Function 1 Bit 29: Corresponds to PCIe Controller F, Function 2 Bit 30: Corresponds to PCIe Controller F, Function 3 Bit 31: Corresponds to GBETSN Controller This field is going to be used in conjunction with MSPDRTReq and MSPDRTRAck fields above. If ASL code intends to over-ride HW decisions, it will set the corresponding bit for a controller/function to 1 in ASLOR and use MSPDRTReq bits to power-up/power-down SPD.

4.2.16 ModPHY Power Management Configuration Reg 5 (MODPHY_PM_CFG5) — Offset 10D0h

This register contains misc fields used to configure the PCH's power management behavior with respect to the modPHY.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Controller SPD RTD3 Request [26:0] (MSPDRTREQ):** This field represents ASL code trigger request for ModPHY SPD gating. If this bit is set (to 1) for a controller, it implies that ASL code provides consent for SPD to be gated for the corresponding controllers lanes. Note that this bit could also be more statically used by BIOS to set this to 1 for a controller where SPD will only be managed through other interfaces implying ASL code does not exist for a controller. The controllers that are not enabled (Function Disabled), this field will be statically set by BIOS to activate ASL component in SPD gating equations. Bit 0: Corresponds to PCIe Controller A, Function 0 Bit 1: Corresponds to PCIe Controller A, Function 1 Bit 2: Corresponds to PCIe Controller A, Function 2 Bit 3: Corresponds to PCIe Controller A, Function 3 Bit 4: Corresponds to PCIe Controller B, Function 0 Bit 5: Corresponds to PCIe Controller B, Function 1 Bit 6: Corresponds to PCIe Controller B, Function 2 Bit 7: Corresponds to PCIe Controller B, Function 3 Bit 8: Corresponds to PCIe Controller C, Function 0 Bit 9: Corresponds to PCIe Controller C, Function 1 Bit 10: Corresponds to PCIe Controller C, Function 2 Bit 11: Corresponds to PCIe Controller C, Function 3 Bit 12: Corresponds to SATA Controller Bit 13: Corresponds to Gbe Controller Bit 14: Corresponds to xHCI Controller Bit 15: Corresponds to xDCI Controller Bit 16: Reserved Bit 17: Corresponds to PCIe Controller D, Function 0 Bit 18: Corresponds to PCIe Controller D, Function 1 Bit 19: Corresponds to PCIe Controller D, Function 2 Bit 20: Corresponds to PCIe Controller D, Function 3 Bit 21: Corresponds to PCIe Controller E, Function 0 Bit 22: Corresponds to PCIe Controller E, Function 1 Bit 23: Corresponds to PCIe Controller E, Function 2 Bit 24: Corresponds to PCIe Controller E, Function 3 Bit 25: Corresponds to DMI Controller Bit 26: Reserved Bit 27: Corresponds to PCIe Controller F, Function 0 Bit 28: Corresponds to PCIe Controller F, Function 1 Bit 29: Corresponds to PCIe Controller F, Function 2 Bit 30: Corresponds to PCIe Controller F, Function 3 Bit 31: Corresponds to GBETSN Controller

4.2.17 ModPHY Power Management Configuration Reg 6 (MODPHY_PM_CFG6) — Offset 10D4h

This register contains misc. fields used to configure the PCH's power management behavior with respect to the modPHY.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Controller SPD RTD3 Request Acknowledge [19:0] (MSPDRTRACK):** This field represents the acknowledge for ASL code trigger request for ModPHY SPD gating. PMC sets a bit in this field to 1 to acknowledge that it has registered the corresponding MSPDRTREQ. Note that the action of setting this bit to 1 is immediate no other gating conditions are involved in this. Actual SPD shutdown may happen later once other power gating conditions have been satisfied as well. PMC clears a bit to 0 in this field once the corresponding MSPTDRTREQ is cleared by the ASL code and SPD state has been fully restored. Bit 0: Corresponds to PCIe Controller A, Function 0 Bit 1: Corresponds to PCIe Controller A, Function 1 Bit 2: Corresponds to PCIe Controller A, Function 2 Bit 3: Corresponds to PCIe Controller A, Function 3 Bit 4: Corresponds to PCIe Controller B, Function 0 Bit 5: Corresponds to PCIe Controller B, Function 1 Bit 6: Corresponds to PCIe Controller B, Function 2 Bit 7: Corresponds to PCIe Controller B, Function 3 Bit 8: Corresponds to PCIe Controller C, Function 0 Bit 9: Corresponds to PCIe Controller C, Function 1 Bit 10: Corresponds to PCIe Controller C, Function 2 Bit 11: Corresponds to PCIe Controller C, Function 3 Bit 12: Corresponds to SATA Controller Bit 13: Corresponds to Gbe Controller Bit 14: Corresponds to xHCI Controller Bit 15: Corresponds to xDCI Controller Bit 16: Reserved Bit 17: Corresponds to PCIe Controller D, Function 0 Bit 18: Corresponds to PCIe Controller D, Function 1 Bit 19: Corresponds to PCIe Controller D, Function 2 Bit 20: Corresponds to PCIe Controller D, Function 3 Bit 21: Corresponds to PCIe Controller E, Function 0 Bit 22: Corresponds to PCIe Controller E, Function 1 Bit 23: Corresponds to PCIe Controller E, Function 2 Bit 24: Corresponds to PCIe Controller E, Function 3 Bit 25: Corresponds to DMI Controller Bit 26: Reserved Bit 27: Corresponds to PCIe Controller F, Function 0 Bit 28: Corresponds to PCIe Controller F, Function 1 Bit 29: Corresponds to PCIe Controller F, Function 2 Bit 30: Corresponds to PCIe Controller F, Function 3 Bit 31: Corresponds to GBETSN Controller

4.2.18 External Rail Config (EXT_RAIL_CONFIG) — Offset 11B8h

External Rail Configuration

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**VNN_MIN_RET_VOLT_SUPPORTED:** This bit indicates whether minimum retention voltage (0.7V) is supported for VNN rail **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
30	0h RW/L	**VNN_MIN_ACTIVE_VOLT_SUPPORTED:** This bit indicates whether minimum active voltage (0.75V) is supported for VNN rail **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
29	0h RW/L	**VNN_NORM_ACTIVE_VOLT_SUPPORTED:** This bit indicates whether normal active voltage (1.05V) is supported **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
28	0h RW/L	**VNN_RET_ACTIVE_SWITCH_SUPPORTED:** This bit indicates whether or not GPIO controls what voltage the voltage rail supports (Bit 31 and Bit 30) **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
27	0h RW/L	**V1P05_MIN_RET_VOLT_SUPPORTED:** This bit indicates whether minimum retention voltage is supported for V1P05 rail (0.95) **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
26	0h RW/L	**V1P05_MIN_ACTIVE_VOLT_SUPPORTED:** This bit is not used and only kept for consistency with Vnn and possible future use **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
25	0h RW/L	**V1P05_NORM_ACTIVE_VOLT_SUPPORTED:** This bit indicates whether normal active voltage (1.05V) is supported **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
24	0h RW/L	**V1P05_RET_ACTIVE_SWITCH_SUPPORTED:** This bit indicates whether or not GPIO controls what voltage the voltage rail supports (Bit 26 and Bit 27) **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
23:13	0h RO	**Reserved**
12	0h RW/L	**Enable External V1P05 Rail in S5 (ENABLE_EXT_V1P05_RAIL_S5):** Enable External V1P05 Rail in S5 **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
11	0h RW/L	**Enable External V1P05 Rail in S4 (ENABLE_EXT_V1P05_RAIL_S4):** Enable External V1P05 Rail in S4 **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/L	**Enable External V1P05 Rail in S3 (ENABLE_EXT_V1P05_RAIL_S3):** Enable External V1P05 Rail in S3 **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
9	0h RW/L	**Enable External V1P05 Rail in S0i3 (ENABLE_EXT_V1P05_RAIL_S0I3):** Enable External V1P05 Rail in S0i3 **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
8	0h RW/L	**Enable External V1P05 Rail in S0i1/S0i2 (ENABLE_EXT_V1P05_RAIL_S0I1_I2):** Enable External V1P05 Rail in S0i1/S0i2 **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
7:5	0h RO	**Reserved**
4	0h RW/L	**Enable External VNN Rail in S5 (ENABLE_EXT_VNN_RAIL_S5):** Enable External Vnn Rail in S5 **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
3	0h RW/L	**Enable External VNN Rail in S4 (ENABLE_EXT_VNN_RAIL_S4):** Enable External Vnn Rail in S4 **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
2	0h RW/L	**Enable External VNN Rail in S3 (ENABLE_EXT_VNN_RAIL_S3):** Enable External Vnn Rail in S3 **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
1	0h RW/L	**Enable External VNN Rail in S0i3 (ENABLE_EXT_VNN_RAIL_S0I3):** Enable External Vnn Rail in S0i3 **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
0	0h RW/L	**Enable External VNN Rail in S0i1/S0i2 (ENABLE_EXT_VNN_RAIL_S0I1_I2):** Enable External Rail in S0i1/S0i2 **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK

4.2.19 External Rail Config (EXT_V1P05_VR_CONFIG) — Offset 11C0h

External Rail Configuration

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
26:24	0h RW/L	**External V1P05 Voltage Value - Upper (EXT_V1P05_VOLTAGE1):** This register houses the voltage for the external V1p05 rail that will be used in S0i2/S0i3 states. Expectation is that SW will update this based on if there are in S0i2 or S0i3. This value is given in 2.5mV increments. PMC will need to write this value to the WORKPOINT FIVR sleep entrance register. When this register is updated, the value in this field gets translated into a write to the SSBFEXITWP1 register in the associated FIVR, in the format expected in SSBEXITWP1. OEM cannot change the value of the PMIC voltage during idle windows in which this supply is being used. **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
23:16	00h RW/L	**External V1P05 Voltage Value - Lower (EXT_V1P05_VOLTAGE0):** This register houses the voltage for the external V1p05 rail that will be used in S0i2/S0i3 states. Expectation is that SW will update this based on if there are in S0i2 or S0i3. This value is given in 2.5mV increments. PMC will need to write this value to the WORKPOINT FIVR sleep entrance register. When this register is updated, the value in this field gets translated into a write to the SSBFEXITWP1 register in the associated FIVR, in the format expected in SSBEXITWP1. OEM cannot change the value of the PMIC voltage during idle windows in which this supply is being used. **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
15:8	00h RW/L	**External V1P05 Icc Max Value - Upper (EXT_V1P05_ICC_MAX_VAL1):** This register houses the Icc max for the external V1p05 rail in granularity of ma in U2.14 format. **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
7:0	00h RW/L	**External V1P05 Icc Max Value - Lower (EXT_V1P05_ICC_MAX_VAL0):** This register houses the Icc max for the external V1p05 rail in granularity of ma in U2.14 format. **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK

4.2.20 External Rail Config (EXT_VNN_VR_CONFIG0) — Offset 11C4h

External Rail Configuration

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
26:24	0h RW/L	**External VNN Voltage Value - Upper (EXT_VNN_VOLTAGE1):** This register houses the voltage for the external VNN rail that will be used in S0i2/S0i3 states. Expectation is that SW will update this based on if there are in S0i2 or S0i3. This value is given in 2.5mV increments. PMC will need to write this value to the WORKPOINT FIVR sleep entrance register. When this register is updated, the value in this field gets translated into a write to the SSBFEXITWP1 register in the associated FIVR, in the format expected in SSBEXITWP1. OEM cannot change the value of the PMIC voltage during idle windows in which this supply is being used. **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
23:16	00h RW/L	**External VNN Voltage Value - Lower (EXT_VNN_VOLTAGE0):** This register houses the voltage for the external VNN rail that will be used in S0i2/S0i3 states. Expectation is that SW will update this based on if there are i S0i2 or S0i3. This value is given in 2.5mV increments. PMC will need to write this value to the WORKPOINT FIVR sleep entrance register. When this register is updated, the value in this field gets translated into a write to the SSBFEXITWP1 register in the associated FIVR, in the format expected in SSBEXITWP1. OEM cannot change the value of the PMIC voltage during idle windows in which this supply is being used. **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
15:8	00h RW/L	**External VNN Icc Max Value - Upper (EXT_VNN_ICC_MAX_VAL1):** This register houses the Icc max for the external VNN rail in granularity of ma in U2.14 format. **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
7:0	00h RW/L	**External VNN Icc Max Value - Lower (EXT_VNN_ICC_MAX_VAL0):** This register houses the Icc max for the external VNN rail in granularity of ma in U2.14 format. **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK

4.2.21 VNN V1p05 Control Hold Off (VNN_V1P05_CTRL_HOLD_OFF) — Offset 11C8h

Hold Off Control for V1p05

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11C8h	00000101h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15:8	01h RW/L	**V1p05 Control Ramp Timer (V1P05_CTRL_RAMP_TMR):** This register holds the V1P05 control hold off values to be used when changing the v1p05_ctrl for external bypass value in us **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
7:0	01h RW/L	**VNN Control Ramp Timer (VNN_CTRL_RAMP_TMR):** This register holds the VNN control hold off values to be used when changing the vnn_ctrl for external bypass value in us **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK

4.2.22 EXT FET RAMP CFG (EXT_FET_RAMP_CFG) — Offset 11CCh

External FET Ramp Time Configuration

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11CCh	00040004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**V1p05-IS FET Ramp Time Lock (V1P05_IS_FRT_LOCK):** The bit is used to lock V1P05_IS_FET_RAMP_TIME. This bit is self-locking (i.e. once written to '1', it can only be cleared by host_prim_rst_b). **Locked by:** EXT_FET_RAMP_CFG.V1P05_IS_FRT_LOCK
30:24	0h RO	**Reserved**
23:16	04h RW/L	**V1p05-IS FET Ramp Time (V1P05_IS_FET_RAMP_TIME):** This field defines the ramp time of the external V1p05-IS FET. Each increment is 10us (ie. 0x4=40us). This field is locked by V1P05_IS_FRT_LOCK. **Locked by:** EXT_FET_RAMP_CFG.V1P05_IS_FRT_LOCK
15	0h RW/L	**V1P05-PHY FET Ramp Time Lock (V1P05_PHY_FRT_LOCK):** The bit is used to lock V1P05_PHY_FET_RAMP_TIME. This bit is self-locking (i.e. once written to '1', it can only be cleared by host_prim_rst_b). **Locked by:** EXT_FET_RAMP_CFG.V1P05_PHY_FRT_LOCK
14:8	0h RO	**Reserved**
7:0	04h RW/L	**V1p05-PHY FET Ramp Time (V1P05_PHY_FET_RAMP_TIME):** This field defines the ramp time of the external V1p05-PHY FET. Each increment is 31us (ie. 0x4=124us). This field is locked by V1P05_PHY_FRT_LOCK. **Locked by:** EXT_FET_RAMP_CFG.V1P05_PHY_FRT_LOCK

4.2.23 VCCIN AUX CONFIG Register1 (VCCIN_AUX_CFG1) — Offset 11D0h

This register defines the characteristics of the VCCIN_AUX voltage

rail

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW/L	**Low Current Mode Voltage to High Current Mode Voltage Transition Time (LCM_HCM_VOLT_TRANS_TIME):** Voltage transition time required by motherboard voltage regulator when PCH changes the VCCIN_AUX regulator set point from the low current mode voltage and high current mode voltage. This field has 1us resolution. 8'h00 = Transition from low current mode voltage retention mode VID disabled. (default) 8'h01 = 1us 8'h02 = 2us . . . 8'hFF = 255us Note: When [23:16]=8'h00 PCH will not transition VCCIN_AUX to low current mode voltage. **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK
15:8	00h RW/L	**Retention Mode Voltage to High Current Mode Voltage Transition Mode (RMV_HCM_VOLT_TRANS_TIME):** Voltage transition time required by motherboard voltage regulator when PCH changes the VCCIN_AUX regulator set point from the retention mode voltage and low current mode voltage. This field has 1us resolution. when PCH changes the VCCIN_AUX regulator set point from the retention mode voltage and high current mode voltage. This field has 1us resolution. 8'h00 = Transition from retention mode voltage to high current mode voltage is disabled (default) 8'h01 = 1us 8'h02 = 2us . . . 8'hFF = 255us Note: When [7:0]=8'h00 and [15:8]=8'h00 PCH will not transition VCCIN_AUX to retention voltage. **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/L	**Retention Mode Voltage to Low Current Mode Voltage Transition Mode (RMV_LCM_VOLT_TRANS_TIME):** Voltage transition time required by motherboard voltage regulator when PCH changes the VCCIN_AUX regulator set point from the retention mode voltage and low current mode voltage. This field has 1us resolution. 8'h00 = Transition from retention mode voltage to low current mode voltage is disabled (default) 8'h01 = 1us 8'h02 = 2us . . . 8'hFF = 255us Note: When [7:0]=8'h00 and [15:8]=8'h00 PCH will not transition VCCIN_AUX to retention voltage. **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK

4.2.24 VCCIN AUX CONFIG Register2 (VCCIN_AUX_CFG2) — Offset 11D4h

This register defines the characteristics of the VCCIN_AUX voltage

rail

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10:8	0h RW/L	**Retention Mode Voltage to Low Current Mode Voltage Transition Mode (OFF_HCM_VOLT_TRANS_TIME_10_8):** Voltage transition time required by motherboard voltage regulator when PCH changes the VCCIN_AUX regulator set point from 0V to the high current mode voltage. 11'h000 = Transition to 0V in S0 & Sx states is disabled (default) 11'h001 = 1us 11'h002 = 2us . . . 11'hFFF = 2048us Note: Setting this field to 11'h000 sets VCCIN_AUX as a fixed rail that stays on in all S0 & Sx power states after initial start up on G3 exit **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/L	**Retention Mode Voltage to Low Current Mode Voltage Transition Mode (OFF_HCM_VOLT_TRANS_TIME_7_0):** Voltage transition time required by motherboard voltage regulator when PCH changes the VCCIN_AUX regulator set point from 0V to the high current mode voltage. 11'h000 = Transition to 0V in S0 & Sx states is disabled (default) 11'h001 = 1us 11'h002 = 2us . . . 11'hFFF = 2048us Note: Setting this field to 11'h000 sets VCCIN_AUX as a fixed rail that stays on in all S0 & Sx power states after initial start up on G3 exit **Locked by:** GEN_PMCON_B.VR_CONFIG_LOCK

4.2.25 Always Running Timer Value 31:0 (ARTV_31_0) — Offset 1200h

Always Running Timer Value

Note: This register is intended for debug purposes only. to obtain the most accurate timer reading, customers are recommended to read the PCH ART through the CPU TSC (Time Stamp Counter) register and apply CPUID conversion.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1200h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**ART Value (ARTV):** Reads return current value of the ART timer [31:0]. Writes to this register has no effect Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

4.2.26 Always Running Timer Value 31:0 (ARTV_63_32) — Offset 1204h

Always Running Timer Value

Note: This register is intended for debug purposes only. to obtain the most accurate timer reading, customers are recommended to read the PCH ART through the CPU TSC (Time Stamp Counter) register and apply CPUID conversion.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1204h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**ART Value (ARTV):** Reads return current value of the ART timer [63:32]. Writes to this register has no effect Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

4.2.27 Timed GPIO Control 0 (TGPIOCTL0) — Offset 1210h

Timed GPIO Control 0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1210h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RW	**Periodic Mode (PM):** 0:Periodic mode is disabled 1:periodic mode is enabled This bit is only applicable when Timed GPIO is configured as an output
3:2	0h RW	**Event Polarity (EP):** 00:Rising Edge 01:Falling Edge 10:Toggle Edge 11:Reserved
1	0h RW	**DIR:** 0: Output 1: Input

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**EN:** 0: Timed GPIO is disabled 1: Timed GPIO is enabled Note: a. When Enabled, xtal clock turnoff is disabled. This may also disable SLP_S0 assertion b. All other Timed GPIO configuration bits must be programmed before enable bit is set and must not change while the enable is 1

4.2.28 Timed GPIO 0 Comparator Value 31:0 (TGPIOCOMPV0_31_0) — Offset 1220h

Timed GPIO 0 comparator Value 31:0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1220h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Comparator Value (COMPV):** This register is only applicable when Timed GPIO is configured as an output. If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. For example, in periodic mode if the value written to this register is 00000100h, and Periodic Interval register has the value of 200h. 1. A Timed GPIO event will be generated when ART reaches 00000100h. 2. The value in this register will then be adjusted by the hardware to 00000300h. 3. Another Timed GPIO event will be generated when the ART reaches 00000300h. 4. The value in this register will then be adjusted by the hardware to 00000500h As such when periodic Timed GPIO event occurs, the value in this register will increment. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

4.2.29 Timed GPIO Comparator Value 63:32 (TGPIOCOMPV0_63_32) — Offset 1224h

Timed GPIO Comparator Value

Note: **NOTE:** Bit definitions are the same as TGPIOCOMPV0_31_0, offset 1220h.

4.2.30 Timed GPIO0 Periodic Interval Value 31_0 (TGPIOPIV0_31_0) — Offset 1228h

Timed GPIO0 Periodic Interval Value 31_0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1228h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Periodic Interval Value [31:0] (PIV):** This register is only applicable when Timed GPIO is configured as an output, and Periodic Mode is enabled. The value in this register is written by SW to set the interval for the periodic Timed GPIO event

4.2.31 Timed GPIO 0 Periodic Interval Value 63_32 (TGPIOPIV0_63_32) — Offset 122Ch

Timed GPIO 0 Periodic Interval Value 63_32

Note: **NOTE:** Bit definitions are the same as TGPIOPIV0_31_0, offset 1228h.

4.2.32 Timed GPIO Time Capture Register 31_0 (TGPIOTCV0_31_0) — Offset 1230h

Timed GPIO Time Cpature Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1230h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Time Capture Value [31:0] (TCV):** When Timed GPIO event triggers, HW captures the current ART time into this register. This register is applicable to both when Timed GPIO is configured as an input or an output. When Timed GPIO is configured as an output, the Time Capture Value in this register is the Comparator Value (COMPV) when a match with ART time happens and a Timed GPIO output event generated. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

4.2.33 Timed GPIO0 Time Capture Register 63_32 (TGPIOTCV0_63_32) — Offset 1234h

Timed GPIO Time Capture Register 63_32

Note: **NOTE:** Bit definitions are the same as TGPIOTCV0_31_0, offset 1230h.

4.2.34 Timed GPIO0 Event Counter Capture Register 31_0 (TGPIOECCV0_31_0) — Offset 1238h

Timed GPIO0 Event Counter Capture Register 31_0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1238h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Event Counter Capture Value [31:0] (ECCV):** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register. A read to the Time Capture Value (TGPIOTCV0_31_0) register triggers HW to load the Event Counter value into this register. Note: The 'load' signal is the same register read signal that returns the Time Capture Value to the SW. SW must first perform a read to the Time Capture Value (TGPIOTCV0_31_0) register, followed by a read to this Event Counter Capture Value (ECCV) register such that these two values are associated with each others, despite they are obtained thru 2 separate register read operations one after another. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

4.2.35 Timed GPIO0 Event Counter Capture Register 63_32 (TGPIOECCV0_63_32) — Offset 123Ch

Timed GPIO0 Event Counter Capture Register 63_32

Type	Size	Offset	Default
MMIO	32 bit	BAR + 123Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Event Counter Capture Value [63:32] (ECCV):** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value (TGPIOTCV0_31_0) register. A read to the Time Capture Value (TGPIOTCV0_31_0) register triggers HW to load the Event Counter value into this register. Note: The 'load' signal is the same register read signal that returns the Time Capture Value to the SW. SW must first perform a read to the Time Capture Value (TCV_31_0) register, followed by a read to this Event Counter Capture Value (ECCV) register such that these two values are associated with each others, despite they are obtained thru 2 separate register read operations one after another. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

4.2.36 Timed GPIO0 Event Counter Register 31_0 (TGPIOEC0_31_0) — Offset 1240h

Timed GPIO0 Event Counter Register 31_0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1240h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Event Counter Register [31:0] (EC):** Event Counter (EC): After Timed GPIO is enabled, event counter operates as follow: ' When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. ' When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. Note: The signal to increment the count is the same signal that captures the ART time into the TCV register. For Timed GPIO configured as output with Periodic Mode enabled, it is also the same signal that updates the Comparator Value for the subsequent match. When Timed GPIO is disabled, event counter is reset to 0x0. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

4.2.37 Timed GPIO0 Event Counter Register 63_32 (TGPIOEC0_63_32) — Offset 1244h

Timed GPIO0 Event Counter Register 63_32

Note: **NOTE:** Bit definitions are the same as TGPIOEC0_31_0, offset 1240h.

4.2.38 Timed GPIO Control 1 (TGPIOCTL1) — Offset 1310h

Timed GPIO Control 1

Note: **NOTE:** Bit definitions are the same as TGPIOCTL0, offset 1210h.

4.2.39 Timed GPIO 1 Comparator Value 31:0 (TGPIOCOMPV1_31_0) — Offset 1320h

Timed GPIO 1 comparator Value 31:0

Note: **NOTE:** Bit definitions are the same as TGPIOCOMPV0_31_0, offset 1220h.

4.2.40 Timed GPIO Comparator Value 63:32 (TGPIOCOMPV1_63_32) — Offset 1324h

Timed GPIO Comparator Value 63:32

Note: **NOTE:** Bit definitions are the same as TGPIOCOMPV0_31_0, offset 1220h.

4.2.41 Timed GPIO1 Periodic Interval Value 31_0 (TGPIOPIV1_31_0) — Offset 1328h

Timed gPIO Periodic Interval Value 31_0

Note: **NOTE:** Bit definitions are the same as TGPIOPIV0_31_0, offset 1228h.

4.2.42 Timed GPIO 1 Periodic Interval Value 63_32 (TGPIOPIV1_63_32) — Offset 132Ch

Timed GPIO 1 Periodic Interval Value 63_32

Note: **NOTE:** Bit definitions are the same as TGPIOPIV0_31_0, offset 1228h.

4.2.43 Timed GPIO Time Capture Register 31_0 (TGPIOTCV1_31_0) — Offset 1330h

Timed GPIO Time Capture Register 31_0

Note: **NOTE:** Bit definitions are the same as TGPIOTCV0_31_0, offset 1230h.

4.2.44 Timed GPIO Time Capture Register 63_32 (TGPIOTCV1_63_32) — Offset 1334h

Timed GPIO Time Capture Register 63_32

Note: **NOTE:** Bit definitions are the same as TGPIOTCV0_31_0, offset 1230h.

4.2.45 Timed GPIO0 Event Counter Capture Register 31_0 (TGPIOECCV1_31_0) — Offset 1338h

Timed GPIO0 Event Counter Capture Register 31_0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1338h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Event Counter Capture Value [31:0] (ECCV):** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register. A read to the Time Capture Value (TCV1_31_0) register triggers HW to load the Event Counter value into this register. Note: The 'load' signal is the same register read signal that returns the Time Capture Value to the SW. SW must first perform a read to the Time Capture Value (TCV1_31_0) register, followed by a read to this Event Counter Capture Value (ECCV) register such that these two values are associated with each others, despite they are obtained thru 2 separate register read operations one after another. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

4.2.46 Timed GPIO0 Event Counter Capture Register 63_32 (TGPIOECCV1_63_32) — Offset 133Ch

Timed GPIO0 Event Counter Capture Register 63_32

Type	Size	Offset	Default
MMIO	32 bit	BAR + 133Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Event Counter Capture Value [63:32] (ECCV):** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value (TGPIOTCV0_31_0) register. A read to the Time Capture Value (TCV) register triggers HW to load the Event Counter value into this register. Note: The 'load' signal is the same register read signal that returns the Time Capture Value to the SW. SW must first perform a read to the Time Capture Value (TCV1_31_0) register, followed by a read to this Event Counter Capture Value (ECCV) register such that these two values are associated with each others, despite they are obtained thru 2 separate register read operations one after another. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

4.2.47 Timed GPIO1 Event Counter Register 31_0 (TGPIOEC1_31_0) — Offset 1340h

Timed GPIO1 Event Counter Register 31_0

Note: **NOTE:** Bit definitions are the same as TGPIOEC0_31_0, offset 1240h.

4.2.48 Timed GPIO Event Counter Register 63_32 (TGPIOEC1_63_32) — Offset 1344h

Timed GPIO Event Counter Register 63_32

Note: **NOTE:** Bit definitions are the same as TGPIOEC0_31_0, offset 1240h.

4.2.49 Catastrophic Trip Point Enable (CTEN) — Offset 150Ch

This register is used to enable Catastrophic Trip point assertion into S5 state on a Cattrip event. This bit should always be set in all functional cases.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 150Ch	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Policy Lock-Down Bit (CTENLOCK):** When written to 1, this bit prevents any more writes to this register. **Locked by:** CTEN.CTENLOCK
30:1	0h RO	**Reserved**
0	1h RW/L	**Catastrophic Power-Down Enable (CPDEN):** 0x1 (Default): When set, the power management logic (PMC) transitions to the S5 state when a catastrophic temperature is detected by any of the sensor. The transition to the S5 state must be unconditional (like the Power Button Override Function).0x0: Disable going into S5 state on a CatTrip detection. This bit should only be set to 0 for debug purposes. Note: Thermal sensor and response logic are in the core/main power well; therefore, detection of a catastrophic temperature is limited to times when this well is powered and out of reset. **Locked by:** CTEN.CTENLOCK

4.2.50 EC Thermal Sensor Reporting Enable (ECRPTEN) — Offset 1510h

This is a BIOS programmable register used to enable reporting of temperature by PMC to EC over eSPI. Setting bit 0 will cause a GCR interrupt to PMC FW through generic GCR mechanism. FW needs to enable the periodic reporting task accordingly. Bit 31 is uses as a lock bit to prevent any further writes to bit 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1510h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Lock-Down Bit (ECRPTENLOCK):** When written to 1, this bit prevents any more writes to this register. **Locked by:** ECRPTEN.ECRPTENLOCK
30:1	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/L	**Enable PMC to EC Temperature Reporting (EN_PMC_TO_EC_TEMP_RPT):** 0x1: Enables the reporting of the PCH temperature to the EC (via SMBUS or eSPI). Note that this must also be set if ME needs access to the PCH temperature. Once enabled this bit should not be cleared by SW. If it is cleared then the EC may get an undefined value. SW has no need to dynamically disable and then re-enable this bit.0x0 (Default): Disables temperature reporting (default) **Locked by:** ECRPTEN.ECRPTENLOCK

4.2.51 Throttle Level (TL) — Offset 1520h

Throttle Level.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1520h	0FF3FCFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**TLLOCK:** When set to 1, this entire register (TL) is locked and remains locked until the next platform reset **Locked by:** TL.TLLOCK
30	0h RW/L	**TT State 13 Enable (TT13EN):** When set to 1 and the programmed GPIO pin is a 1, then PMSync state 13 (now called GPIO_A) will force at least T2 state **Locked by:** TL.TLLOCK
29	0h RW/L	**TT Enable (TTEN):** This is the enable bit associated with the FW control of the throttle state. This bit needs to be set in order for the FW to be able to update the throttle state based on the comparison of the T2L/T1L/T0L with the temperature. At reset, BIOS must set bits 28:0 and then do a separate write to set bit 29 to enable throttling. SW may set bit 31 at the same time it sets bit 29 if it wishes to lock the register. If SW wishes to change the values of 28:0, it must first clear the TTEN bit, then change the values in 28:0; and then re-enable TTEN. It is legal to set bits 31, 30 and 29 with the same write This bit must not be set by SW until SW has already enabled atleast one of the thermal sensor(setting TSENx.ETS bits to 1) If TTEN is written to 0, after having been enabled, then the PCH may stay in the throttling state it was in at the moment TTEN is disabled. There is no intent that the sensor be enabled for a while and then disabled and left off. It may be disabled temporarily while changing the register values, but it should not be left in the disabled state **Locked by:** TL.TLLOCK
28:20	0FFh RW/L	**T2 Level (T2L):** Determines the temp level for T2 state. If TTEN = 1 AND TSEN = 1 AND T2L >= TEMP.MAXTEMP[8:0] > T1L, then the system is in T2 state. If TTEN = 1 AND TSE = 1 AND TEMP.MAXTEMP [8:0] > T2L, then the system is in T3 state.SW Note: When TTEN =1 condition to satisfy is T2L > T1L > T0L NOTE: the T3 condition overrides PMSync[13] and forces the system to T3 if both cases are true **Locked by:** TL.TLLOCK

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**Reserved**
18:10	0FFh RW/L	**T1 Level (T1L):** Determines the temp level for T1 state. If TTEN = 1 AND (|TSEN) = 1 AND T1L >= TEMP.MAXTEMP[8:0] > T0L, then the system is in T1 state. SW Note: When TTEN =1 condition to satisfy is T2L > T1L > T0L **Locked by:** TL.TLLOCK
9	0h RO	**Reserved**
8:0	0FFh RW/L	**T0 Level (T0L):** Determines the temp level for T0 state. If TEMP.MAXTEMP[8:0] <= T0L or TTEN = 0 OR (|TSEN) = 0, then the system is in T0 state SW Note: When TTEN =1 condition to satisfy is T2L> T1L > T0L **Locked by:** TL.TLLOCK

4.2.52 Throttle Levels Enable (TLEN) — Offset 1528h

Throttle Levels Enable

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1528h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**TLENLOCK:** When set to 1, this entire register (TLEN) is locked and remains locked until the next platform reset **Locked by:** TLEN.TLENLOCK
30:0	0h RO	**Reserved**

4.2.53 Thermal Sensor Alert High Value (TSAHV) — Offset 1530h

This register is used to set the Thermal Alert High Value for all Thermal Sensors on the chip. PMC HW should compare the aggregated MAXTEMP against these values to cause an SMI or SCI Interrupt

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1530h	000000FFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8:0	0FFh RW	**Alert High Value (AHV):** Sets the high value for the alert indication. See the later section for usage. Temperature programmed in S9.8.0 2s complement format This register is not lockable, so that SW can change the values during runtime. NOTE: it is illegal for SW to program TSAHV.AHV to a value lower than TSAL.ALV

4.2.54 Thermal Sensor Alert Low Value (TSALV) — Offset 1534h

This register is used to set the Thermal Alert Low Value for all Thermal Sensors on the chip. PMC HW should compare the aggregated MINTEMP against these values to cause an SMI or SCI Interrupt

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1534h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8:0	000h RW	**Alert Low Value (ALV):** Sets the low value for the alert indication. See the later section for usage. Temperature programmed in S9.8.0 2s complement format This register is not lockable, so that SW can change the values during runtime. NOTE: it is illegal for SW to program TSALV.ALV to a value higher than TSAH.AHV

4.2.55 Thermal Alert Trip Status (TAS) — Offset 1538h

SW uses this register to determine the Thermal Alert Trip event (Low-to-High or High-to-Low) along with the Thermal Sensor ID that caused this event.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1538h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/V	**TS Alert High-to-Low Event (AHLE):** 0x1: Indicates that an Thermal Sensor trip event occurred based on a higher to lower temperature transition thru the trip point 0x0: No trip for this event Software must write a 1 to clear this status bit Note: AHLE will not be set until there has been one occurrence of a Low to High event (ALHE must have been set once). This prevents the case where the system power up at a reasonably high temperature and starts to cool off while booting and causing an interrupt before there is SW loaded to handle it
14:12	0h RO	**Reserved**
11:8	0h RO/V	**High-to-Low trip TS (HLTTS):** 0xF 0x3: Reserved 0x2: TS2 0x1: TS1 0x0: TS0
7	0h RW/1C/V	**TS Alert Low-to-High Event (ALHE):** 0x1: Indicates that an Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point 0x0: No trip for this event Software must write a 1 to clear this status bit Note: AHLE will not be set until there has been one occurrence of a Low to High event (ALHE must have been set once). This prevents the case where the system power up at a reasonably high temperature and starts to cool off while booting and causing an interrupt before there is SW loaded to handle it
6:4	0h RO	**Reserved**
3:0	0h RO/V	**Low-to-High trip TS (LHTTS):** 0xF 0x3: Reserved 0x2: TS2 0x1: TS1 0x0: TS0

4.2.56 PCH Hot Level Control (PHLC) — Offset 1540h

PCH Hot Level Control

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1540h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**PHL Lock (PHLCLOCK):** When written to a 1, this entire register is locked and remains locked until next platform reset **Locked by:** PHLC.PHLCLOCK
30:16	0h RO	**Reserved**
15	0h RW/L	**PHL Enable (PHLE):** When set and the current temperature reading, MaxTSR is greater than PHLL, then the PCHHOT# pin will be asserted (active low) **Locked by:** PHLC.PHLCLOCK
14:9	0h RO	**Reserved**
8:0	000h RW/L	**PHL Level (PHLL):** Temperature value used for PCHHOT# pin assertion based on 2s complement format 0x001 positive 1oC 0x000 0oC 0x1FF negative 1oC 0x1D8 negative 40oC and so on **Locked by:** PHLC.PHLCLOCK

4.2.57 Temperature Sensor Control and Status (TSS0) — Offset 1560h

Register address 0x1560-0x157C are used to capture the raw 2s complement temperature received from the multiple Digital Thermal Sensor (DTS) on a die.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1560h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Policy Lock-Down Bit (TSS0LOCK):** When set to 1, this bit locks down the following fields: - TSS0.TSMASKEN The other bits in TSSx are anyway RO and hence do not need a lock bit set for them.Those bits become read-only . This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a global reset. **Locked by:** TSS0.TSS0LOCK
30:17	0h RO	**Reserved**
16	0h RW/L	**TS MASK for MAXTEMP calculation (TSMASKEN):** 0x0 (Default): Temperature reported from TS is used for temperature comparison with PMC. 0x1: Temperature reported from the TS is masked for TEMP comparison within PMC. This in turn will also enable/disable SMI/SCI assertions for alert thermal events from this TS. **Locked by:** TSS0.TSS0LOCK
15:10	0h RO	**Reserved**
9	0h RO/V	**TS Reading Valid (TSRV):** This bit indicates if the TS die temperature reported in valid or not.
8:0	000h RO/V	**TS Reading (TSR):** The TS die temperature with resolution of 1oC in S9.8.0 2s complement format 0x001 positive 1oC 0x000 0oC 0x1FF negative 1oC 0x1D8 negative 40oC and so on

4.2.58 Wake Alarm Device Timer: AC (WADT_AC) — Offset 1800h

Bits in this register only need to be valid for reading when the Main power well is up. However, since some of the events may initially be detected while the Main power well and SUS well are down, they are marked as DSW bits.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1800h	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/V	**Wake Alarm Device Timer Value for AC Mode (WADT_AC_VAL):** This field contains the 32-bit wake alarm device timer value (granularity 1s) for AC power. The timer begins decrementing when written to a value other than FFFFFFFFh (regardless of the power source when the write occurs). Upon counting down to 0: If on AC power, GPE0b_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0b_EN.WADT_EN is 1. If the power source is DC at this time, the status bit is not set. However, if AC power subsequently returns to the platform, the AC Expired Timer begins running. See the WADT_EXP_AC register for details. The timer returns to its default value of FFFFFFFFh.

4.2.59 Wake Alarm Device Timer: DC (WADT_DC) — Offset 1804h

Bits in this register only need to be valid for reading when the Main power well is up. However, since some of the events may initially be detected while the Main power well and SUS well are down, they are marked as DSW bits.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1804h	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/V	**Wake Alarm Device Timer Value for DC Mode (WADT_DC_VAL):** This field contains the 32-bit wake alarm device timer value (granularity 1s) for DC power. The timer begins decrementing when written to a value other than FFFFFFFFh (regardless of the power source when the write occurs). Upon counting down to 0: If on DC power, GPE0b_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0b_EN.WADT_EN is 1. If the power source is AC at this time, the status bit is not set. However, if DC power subsequently returns to the platform, the DC Expired Timer begins running. See the WADT_EXP_DC register for details. The timer returns to its default value of FFFFFFFFh.

4.2.60 Wake Alarm Device Expired Timer: AC (WADT_EXP_AC) — Offset 1808h

Bits in this register only need to be valid for reading when the Main power well is up. However, since some of the events may initially be detected while the Main power well and SUS well are down, they are marked as DSW bits.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1808h	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/V	**Wake Alarm Device Expired Timer Value for AC Mode (WADT_EXP_AC_VAL):** This field contains the 32-bit wake alarm device Expired Timervalue (granularity 1s) for AC power. The timer begins decrementing after switching from DC to AC power, in the case where the WADT_AC timer has already expired while the platform was on DC power. This timer only decrements while operating on AC power. So if the power source switches back to DC power, the timer will stop (but not reset). When AC power returns, the timer will again begin decrementing. Note: This timer will only begin decrementing under the conditions described above if this field has been configured for something other than its default value of FFFFFFFFh (i.e. FFFFFFFFh = disabled). Upon expiration of this timer: If on AC power, GPE0b_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0b_EN.WADT_EN is 1. BOTH the AC and DC Expired Timers return to their defaults value of FFFFFFFFh.

4.2.61 Wake Alarm Device Expired Timer: DC (WADT_EXP_DC) — Offset 180Ch

Bits in this register only need to be valid for reading when the Main power well is up. However, since some of the events may initially be detected while the Main power well and SUS well are down, they are marked as DSW bits.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 180Ch	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/V	**Wake Alarm Device Expired Timer Value for DC Mode (WADT_EXP_DC_VAL):** This field contains the 32-bit wake alarm device Expired Timervalue (granularity 1s) for DC power. The timer begins decrementing after switching from AC to DC power, in the case where the WADT_DC timer has already expired while the platform was on AC power. This timer only decrements while operating on DC power. So if the power source switches back to AC power, the timer will stop (but not reset). When DC power returns, the timer will again begin decrementing. Note: This timer will only begin decrementing under the conditions described above if this field has been configured for something other than its default value of FFFFFFFFh (i.e. FFFFFFFFh = disabled). Upon expiration of this timer: If on DC power, GPE0b_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0b_EN.WADT_EN is 1. BOTH the AC and DC Expired Timers return to their defaults value of FFFFFFFFh.

4.2.62 Power and Reset Status (PRSTS) — Offset 1810h

Bits in this register only need to be valid for reading when the Main power well is up. However, since some of the events may initially be detected while the Main power well is down, they are marked as suspend well bits. All suspend well bits in this register are reset by global_rst_b.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1810h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW/1C/V	**Wake On LAN Override Wake Status (WOL_OVR_WK_STS):** This bit gets set when integrated LAN Signals a Power Management Event AND the system is in S5. BIOS can read this status bit to determine this wake source. Software clears this bit by writing a 1 to it.
4	0h RW/1C/V	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
3:1	0h RO	**Reserved**
0	0h RW/1C/V	**ME_HOST_WAKE_STS:** This bit is set when the ME generates a non-maskable wake event and is not affected by any other enable bit. When this bit is set, the host power management logic wakes to S0.

4.2.63 Power Management Configuration Reg 1 (PM_CFG) — Offset 1818h

This register contains misc. fields used to configure the PCH's power management behavior.

This register is in multiple power wells and reset domains (see below).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1818h	00000020h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**SATA Interface Disable Indication (SATA_DIS_IND):** When set to 1, this bit indicates that the SATA interface on the PCH is completely disabled. Therefore, the mPhy lanes normally assigned to SATA will operate through the PCIe controller (or not be used at all). When cleared, it indicates that at least some of the SATA interface lanes may be used actively in the PCH by the SATA controller, so none of the four lanes assigned to SATA interface can operate through the PCIe controller.
30	0h RW	**Timing t591 (TIMING_T591):** This field configures t591 timing involved in the over-clocking flow (Wait times between writes from PMC to ICC registers when executing BCLK slow ramp flow) Note: Encodings are all min timings.
29	0h RW	**Allow 24MHz Crystal Oscillator Shutdown (ALLOW_24_OSC_SD):** When this bit is '0', the 24MHz crystal oscillator will always be running while in S0. When this bit is '1', the 24MHz crystal oscillator may be shut down in S0 (Cx only) if all other conditions allow.
28	0h RW	**Time Sync Maximum Attempts (TS_MAXTRY):** The value of this bit determines how many times the PMC will retry time synchronization before stopping and reporting failure to the initiator. Encoding: 0 Maximum of 5 attempts 1 Maximum of 10 attempts
27	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
26	0h RW	**Boot Media RTD3 Power Management Enable (BMRTD3PME):** 0: RTD3 is not enabled. Drive '1' to BOOTMPC pin 1: RTD3 is enabled. Drive the value of BMRTD3PP to BOOTMPC pin
25	0h RW	**Allow USB2 PHY Core Power Gating (ALLOW_USB2_CORE_PG):** When this bit is '0' (default), USB2 PHY power gating is disabled. When this bit is '1', USB2 PHY power gating can occur if all other required conditions are met.
24	0h RW/L	**Energy Reporting Lock (ER_LOCK):** When this bit is written to 1, it will remain 1 until the next host_prim_rst_b assertion. While this bit is 1, GEN_PMCON_A.ER_EN value cannot be changed. BIOS should write 1b1 to this bit only AFTER writing to GEN_PMCON_A.ER_EN. **Locked by:** PM_CFG.ER_LOCK
23:22	0h RO	**Reserved**
21	0h RW	**RTC Wake from DeepSx Disable (RTC_DSX_WAKE_DIS):** When set, this bit disables RTC wakes from waking the system from DeepSx.
20	0h RW	**Boot Media RTD3 Reset Management Enable (BMRTD3RME):** 0: Boot Media device not in D3. Drive '1' to reset pin 1: Boot Media device in D3. Drive the value of BMRTD3RP to reset pin
19:18	0h RW/L	**SLP_SUS# Minimum Assertion Width (SLP_SUS_MIN_ASST_WDTH):** This 2-bit value indicates the minimum assertion width of the SLP_SUS# signal to guarantee that the SUS well power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power failure detection circuits, etc. Settings are: 00 = 0 ms (i.e. stretching disabled - default) 01 = 500ms 10 = 1s 11 = 4s This field is not writable when the SLP_Sx# Stretching Policy Lock- Down bit is set. This field is ignored when exiting a G3 state if the Disable SLP_X Stretching After SUS Power Failurebit is set. Note that unlike with all other SLP_* pin stretching, this disable bit only impacts SLP_SUS# stretching during G3 exit rather than both G3 and DeepSx exit. SLP_SUS# stretching always applies to DeepSx regardless of the disable bit. Programming Note: For platforms that enable DeepSx, BIOS must program SLP_SUS# stretching to be greater than or equal to the largest stretching value on any other SLP_* pin (SLP_S3#, SLP_S4#, SLP_LAN#, or SLP_A#). This bit is cleared by the rtc_pwrgood_rst_b pin. **Locked by:** PCI_MMR.GEN_PMCON_B.SLPSX_STR_POL_LOCK
17:16	0h RW/L	**SLP_A# Minimum Assertion Width (SLP_A_MIN_ASST_WDTH):** This 2-bit value indicates the minimum assertion width of the SLP_A# signal to guarantee that the ASW power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power failure detection circuits, etc. Settings are: 00 = 0 ms (i.e. stretching disabled - default) 01 = 4 s 10 = 98 ms 11 = 2 s This field is not writable when the SLP_Sx# Stretching Policy Lock- Down bit is set. This field is ignored when exiting a G3 or DeepSx state if the Disable SLP_X Stretching After SUS Power Failurebit is set. This bit is cleared by the rtc_pwrgood_rst_b pin. **Locked by:** PCI_MMR.GEN_PMCON_B.SLPSX_STR_POL_LOCK

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RW/L	**SLP_LAN# Minimum Assertion Width (SLP_LAN_MIN_ASST_WDTH):** This 2-bit value indicates the minimum assertion width of the SLP_LAN# signal to guarantee that the power to the PHY has been fully power-cycled. This value may be modified per platform depending on power supply, capacitance, board capacitance, power failure detection circuits, etc. This field is not writable when the SLP_Sx# Stretching Policy Lock Down bit is set to 1.Encoding o0: 0ms, 01: 1ms, 10: 50ms, 11: 2s **Locked by:** PCI_MMR.GEN_PMCON_B.SLPSX_STR_POL_LOCK
13	0h RW	**After G3 Last State Enable (AG3_LS_EN):** When PM_CFG.AG3E is '0', AG3_LS_EN determines whether the PCH will consider the platform's previous state when determining whether to power-up after G3. Encodings: 0 (default): PCH power-up policies after G3 do not depend on the platform's state when the G3 occurred. 1: PCH power-up policies after G3 depend on the platform's state when the G3 occurred. - If the power failure occurred while the platform was in S0 or while in the process of going to S0, the platform will power-up to S0 upon exiting G3. - If the power failure occurred while the platform was in Sx or while in the process of going to Sx, the platform will stay in S4/S5 upon exiting G3. Note: This bit applies only when GEN_PMCON_3.AG3E is '0'. If AG3E is '1', the platform will always stay in S4/S5 after G3 regardless of the value of AG3_LS_EN.
12	0h RW	**After Type 8 Global Reset Last State Enable (A8GR_LS_EN):** AGR_LS_EN determines whether the PCH will consider the platform's previous state when determining whether to power-up after non-thermal and non-explicitly requested type 8 global resets. Encodings: 0 (default): PCH power-up policies after a global reset do not depend on the platform's state when the reset occurred. 1: PCH power-up policies after a global reset depend on the platform's state when the reset occurred. If the global reset occurred while the platform was in S0 or while in the process of going to S0, the platform will power-up to S0 after the reset. If the global reset occurred while the platform was in Sx or while in the process of going to Sx, the platform will stay in S5 upon exiting G3.
11	0h RW	**Global Reset Three Strike Counter Enable (GR_TSC_EN):** When set, GR_TSC_EN will cause the PMC to keep the platform in S5 after the third consecutive type 7 global reset occurs during the boot flow. The three strike counter is reset in the following situations: - The system reaches S0 - A type 8 global reset occurs, including after the three strike counter causes the system to stay in S5. - RSMRST# asserts (due to DeepSx entry or a G3 event occurring)
10	0h RW	**Power Button Debounce Mode (PB_DB_MODE):** This bit controls when interrupts (SMI#, SCI) are generated in response to assertion of the PWRBTN# pin. This bit's values cause the following behavior: - '0': The 16ms debounce period applies to all usages of the PWRBTN# pin (legacy behavior). - '1': When a falling edge occurs on the PWRBTN# pin, an interrupt is generated and the 16ms debounce timer starts. Subsequent interrupts are masked while the debounce timer is running. Note: Power button override logic always samples the post-debounce version of the pin.

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW/L	**Reset Power Cycle Duration (PWR_CYC_DUR):** The value in this register determines the minimum time a platform will stay in reset (SLP_S3#, SLP_S4#, SLP_S5# asserted and also SLP_A# and SLP_LAN# asserted if applicable) during a host partition reset with power cycle or a global reset. The duration programmed in this register takes precedence over the applicable SLP_# stretch timers in these reset scenarios. This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set.Encoding 00: 4-5sec, 01: 3-4sec, 10: 2-3 sec, 11: 1-2 sec Note that the duration programmed in this register should never be smaller than the stretch duration programmed in the following registers - - GEN_PMCON_3.SLP_S3_MIN_ASST_WDTH - GEN_PMCON_3.S4MAW - PM_CFG.SLP_A_MIN_ASST_WDTH - PM_CFG.SLP_LAN_MIN_ASST_WDTH **Locked by:** PCI_MMR.GEN_PMCON_B.SLPSX_STR_POL_LOCK
7:6	0h RW	**T37 Value (T37_VAL):** This field determines the delay from ungating the CPU RTC clock until the PMC considers the clock to be valid, allowing the boot flow to proceed. Encodings: 00 - 10ms 01 - 5ms 10 - 1ms 11 - 200us
5	1h RW/V	**CPU OC Strap (COCS):** SW programs this pin with the value that should be reflected to the GPIO8_OCS pin, when the pin is in native mode. Hardware also sets this bit when the over-clocking watchdog timer expires.
4:3	0h RO	**Reserved**
2	0h RW/L	**Energy Reporting Enable (ER_EN):** When this bit is 1, the PCH will periodically calculate and report its energy consumption to the CPU via PM_SYNC. When this bit is 0, the PCH will neither calculate nor report its energy consumption. **Locked by:** PM_CFG.ER_LOCK
1:0	0h RW/V	**Timing t581 (TIMING_T581):** This field configures the t581 timing involved in the power down flow (CPUPWRGD inactive to ICC_ICLK_INIT inactive). Encodings (all min timings): 00: 10 us (default) 01: 100 us 10: 1 ms 11: 10 ms reset_type=host_deep_rst_b

4.2.64 S3 Power Gating Policies (S3_PWRGATE_POL) — Offset 1828h

This register contains policy bits to configure various power gating options while the system is in S3. Note that setting any of these policies to enabledmay not directly result in power gating - in some cases other HW qualifications may be dynamically applied.

This register is in the RTC power well and is reset by rtc_pwrgood_rst_b.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1828h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**S3 Power Gate Enable in DC Mode: SUS Well (S3DC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S3 while operating on DC power (based on the AC_PRESENT pin value).
0	0h RW	**S3 Power Gate Enable in AC Mode: SUS Well (S3AC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S3 while operating on AC power (based on the AC_PRESENT pin value).

4.2.65 S4 Power Gating Policies (S4_PWRGATE_POL) — Offset 182Ch

This register contains policy bits to configure various power gating options while the system is in S4. Note that setting any of these policies to enabledmay not directly result in power gating - in some cases other HW qualifications may be dynamically applied.

This register is in the RTC power well and is reset by rtc_pwrgood_rst_b.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 182Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**S4 Power Gate Enable in DC Mode: SUS Well (S4DC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S4 while operating on DC power (based on the AC_PRESENT pin value).
0	0h RW	**S4 Power Gate Enable in AC Mode: SUS Well (S4AC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S4 while operating on AC power (based on the AC_PRESENT pin value).

4.2.66 S5 Power Gating Policies (S5_PWRGATE_POL) — Offset 1830h

This register contains policy bits to configure various power gating options while the system is in S5. Note that setting any of these policies to enabledmay not directly result in power gating - in some cases other HW qualifications may be dynamically applied.

This register is in the RTC power well and is reset by rtc_pwrgood_rst_b.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1830h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**S5 Power Gate Enable in DC Mode: SUS Well (S5DC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S5 while operating on DC power (based on the AC_PRESENT pin value).
14	0h RW	**S5 Power Gate Enable in AC Mode: SUS Well (S5AC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S5 while operating on AC power (based on the AC_PRESENT pin value).
13:0	0h RO	**Reserved**

4.2.67 DeepSx Configuration (DSX_CFG) — Offset 1834h

This register contains misc. fields used to configure the PCH's power management behavior.

This register is in the RTC power well.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1834h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RW	**Require CNV Wake Disabled for DeepSx Entry/SUSPWRDNACK (REQ_CNV_NOWAKE_DSX):** If this bit is 0, the state of connectivity wake enable is not considered when making DeepSx entry decisions. If this bit is 1, connectivity wake must be disabled to allow DeepSx entry or SUSPWRDNACK assertion, and even then all other conditions must be satisfied.
3	0h RW	**Require BATLOW# Assertion for DeepSx Entry/SUSPWRDNACK (REQ_BATLOW_DSX):** If this bit is 0, the state of the BATLOW# pin is not considered when making DeepSx entry and SUSPWRDNACK decisions. If this bit is 1, BATLOW# must be asserted to allow DeepSx entry or SUSPWRDNACK assertion, and even then all other entry conditions must be satisfied.
2	0h RW	**WAKE# Pin DeepSx Enable (WAKE_PIN_DSX_EN):** When this bit is 1, the PCI Express WAKE# pin is monitored while in DeepSx, supporting waking from DeepSx due to assertion of this pin. In this case, the platform must externally pull up the pin to the DSW (instead of pulling up to the SUS as has historically been the case). DeepSx disabled configurations must leave this bit at 0. When this bit is 0: DeepSx enabled configurations: The PCH internal pull-down on the WAKE# pin is enabled in deep-Sx and during G3 exit and the pin is not monitored during this time. DeepSx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled
1	0h RW	**AC_PRESENT Pin Pulldown in DeepSx Disable (ACPRES_PD_DSX_DIS):** When this bit is 1, the internal pull-down on the AC_PRESENT pin is disabled. However, the pulldown is not necessarily enabled if the bit '0. This bit must be left at 0 for DeepSx disabled configurations, and the pulldown is disabled for those configurations even though the bit is 0. To support ME wakes from DeepSx using MGPIO2, the pin is always monitored regardless of the value of this host policy bit. When this bit is 0: DeepSx enabled configurations: The PCH internal pull-down on AC_PRESENT is enabled in deep-Sx and during G3 exit. DeepSx disabled configurations: The PCH internal pull-down on AC_PRESENT is always disabled. Note: This bit has no impact on GPIO31 functionality (muxed with AC_PRESENT). GPIO31 is still only driven/monitored while the SUS well is up.
0	0h RW	**LANWAKE Pin DeepSx Enable (LANWAKE_PIN_DSX_EN):** When this bit is 1, the LANWAKE pin is monitored while in DeepSx, supporting waking from DeepSx due to assertion of this pin. In this case, the platform must drive the pin to the correct value while in DeepSx. DeepSx disabled configurations must leave this bit at 0. When this bit is 0: DeepSx enabled configurations: The PCH internal pull-down on LANWAKE pin is enabled in deep-Sx and during G3 exit and the pin is not monitored during this time. DeepSx disabled configurations: The PCH internal pull-down is never enabled

4.2.68 Power Management Configuration Reg 2 (PM_CFG2) — Offset 183Ch

This register contains misc. fields used to configure the PCH's power management behavior.

This register is in multiple power wells and reset domains (see below).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 183Ch	08000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Power Button Override Period (PBOP):** This field determines, while the power button remains asserted, how long the PMC will wait before initiating a global reset. <Enter text here> Encoding: 000b - 4 seconds 001b - 6 seconds 010b - 8 seconds 011b - 10 seconds 100b - 12 seconds 101b - 14 seconds Others - Reserved
28	0h RW/L	**Power Button Native Mode Disable (PB_DIS):** When this bit is '0' (default), the PMC's power button logic will act upon the input value from the GPIO unit, as normal. When this bit is set to '1', the PMC must force its internal version of the power button pin to '1'. This will result in the PMC logic constantly seeing the pin as de-asserted. This bit is not writable when ETR3.PB_DIS_LOCK bit is set. **Locked by:** PCI_MMR.ETR3.PB_DIS_LOCK
27	1h RW	**Reserved**
26	0h RW/V	**DRAM_RESET# Control (DRAM_RESET_CTL):** BIOS uses this bit to control the DRAM_RESET# pin from the PCH, which is routed to the reset pin on the DRAM. Encoding: 0 - DRAM_RESET# = '0' 1 - DRAM_RESET# output is tri-stated. Note: This bit is cleared to '0' by HW when SLP_S4# goes low.
25:0	0h RO	**Reserved**

4.2.69 PM_SYNC Miscellaneous Configuration (PM_SYNC_MISC_CFG) — Offset 18C8h

This register is used to configure miscellaneous aspects of the PM_SYNC pin.

This register is in the CORE power well and is reset by host_prim_rst_b.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 18C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW/L	**GPIO_D Pin Selection (GPIO_D_SEL):** There are two possible GPIOs that can be routed to the GPIO_D PM_SYNC state. This bit selects between them: 0: CPU_GP_3 (default) 1: CPU_GP_2 This field is not writeable when PM_SYNC_LOCK=1. **Locked by:** PM_SYNC_MISC_CFG.PM_SYNC_LOCK
10	0h RW/L	**GPIO_C Pin Selection (GPIO_C_SEL):** There are two possible GPIOs that can be routed to the GPIO_C PM_SYNC state. This bit selects between them: 0: CPU_GP_0 (default) 1: CPU_GP_1 This field is not writeable when PM_SYNC_LOCK=1. **Locked by:** PM_SYNC_MISC_CFG.PM_SYNC_LOCK
9	0h RW/L	**GPIO_B Pin Selection (GPIO_B_SEL):** There are two possible GPIOs that can be routed to the GPIO_B PM_SYNC state. This bit selects between them: 0: CPU_GP_2 (default) 1: CPU_GP_0 This field is not writeable when PM_SYNC_LOCK=1. **Locked by:** PM_SYNC_MISC_CFG.PM_SYNC_LOCK
8	0h RW/L	**GPIO_A Pin Selection (GPIO_A_SEL):** There are two possible GPIOs that can be routed to the GPIO_A PM_SYNC state. This bit selects between them: 0: CPU_GP_1 (default) 1: CPU_GP_3 This field is not writeable when PM_SYNC_LOCK=1. **Locked by:** PM_SYNC_MISC_CFG.PM_SYNC_LOCK
7:0	0h RO	**Reserved**

4.2.70 Power Management Configuration Reg 3 (PM_CFG3) — Offset 18E0h

This register contains misc. fields used to configure the PCH's power management behavior.

This register is in multiple power wells and reset domains (see below).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 18E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BIOS FIVR Dynamic Management Enable (BIOS_FIVR_DYN_EN):** This bit must be '1' to allow dynamic management of the FIVRs. This bit, the SMIP bit, and PMC internal policies must be also be enabled or FIVRs will not be dynamically managed
27:22	0h RO	**Reserved**
21:18	0h RW	**Reserved**
17	0h RW	**Host Wireless LAN Phy Power Enable (HOST_WLAN_PP_EN):** This policy bit is set by Host software when it desires the wireless LAN PHY to be powered in Sx power states for wakes over wireless LAN (WoWLAN). See the SLP_WLAN# sub-section later in this chapter for additional information.
16	0h RW	**Deep-Sx WLAN Phy Power Enable (DSX_WLAN_PP_EN):** When set to 1, PMC will keep SLP_WLAN# high in deep-Sx to enable WoWLAN. Note: (1) This policy bit will be applied for deep-Sx entry from S3, S4 and S5. (2) This bit does not affect SLP_WLAN# behaviour in Sx after G3 or after a global reset (3) HOST_WLAN_PP_EN must be set when this bit is set.
15:5	0h RO	**Reserved**
4	0h RW	**Halt Energy Reporting HW Counters with SLP_S0 Assertion (ER_HALT_SLPS0):** 0: When this register bit is cleared (or left in its default state), then all Energy Reporting HW counters are not halted from incrementing (free running).1: When this bit is set, then all Energy Reporting HW counters will stop incrementing when slp_s0# asserts regardless of the input signal state.
3:0	0h RW	**Reserved**

4.2.71 Power Management Configuration Reg 4 (PM_CFG4) — Offset 18E8h

This register contains misc. fields used to configure the PCH's power management behavior.

This register is in multiple power wells and reset domains (see below).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 18E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RW	**USB2 PHY SUS Well Power Gating Enable (U2_PHY_PG_EN):** If this bit is 1, dynamic power gating of the USB2 PHY SUS well is enabled. Note: This bit prevents HW from initiating power gating entry. However, the USB2 PHY SUS well is power gated by default while in Sx after global_rst_b assertion. So HW will not spontaneously exit power gating while in Sx just because this bit is 0.
29	0h RW	**CPU BCLK Config Override Enable (CPU_BCLK_CFG_OVR_EN):** When set to '1', the value of CPU_BCLK_CFG_OVR_VAL is sent to the CPU as part of EPOC2 instead of the value of the DEF_CPU_BCLK_CFG soft-strap.
28:27	0h RW	**CPU BCLK Config Override Value (CPU_BCLK_CFG_OVR_VAL):** See the definition of CPU_BCLK_CFG_OVR_EN
26:0	0h RO	**Reserved**

4.2.72 CPU Early Power-on Configuration (CPU_EPOC) — Offset 18ECh

CPU Early Power on Configuration

Type	Size	Offset	Default
MMIO	32 bit	BAR + 18ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:20	0h RO/V	**Crystal Frequency[2:1] (XTAL_FREQ_MSB):** Along with XTAL_FREQ_LSB the 3 bit field reflects the frequency of the crystal (aka NSSC) clock used by the CPU and PCH Encoding: 000b -24MHz 001b -19.Mhz 010b -38.4 Mhz Others - Reserved
19	0h RO/V	**EPOC Data[19] (EPOC_DATA_19):** DAM (Delayed Authentication Mode
18	0h RO/V	**EPOC Data[18] (EPOC_DATA_18):** Debug Consent
17	0h RO/V	**Crystal Frequency [0] (XTAL_FREQ_LSB):** See XTAL_FREQ_MSB
16	0h RO	**Reserved**
15:8	00h RO/V	**EPOC Data[15:8] (EPOC_DATA_15_8):** These bits come from PMC soft straps reserved for straps that must be available to the CPU prior to PLTRST# de-assertion. Note: Any straps that only need to be available after OPI is up should be sent as part of the strap set message from SPI instead of being reserved in the PMC straps, defined in EPOC, and sent by the PMC.
7:3	00h RW/L	**EPOC Data [7:3] (EPOC_DATA_7_3):** EPOC Data [7:3] **Locked by:** GEN_PMCON_B.CPU_EPOC_LOCK
2	0h RO	**Reserved**
1:0	0h RW/L	**EPOC Data [1:0] (EPOC_DATA_1_0):** EPOC Data [1:0] **Locked by:** GEN_PMCON_B.CPU_EPOC_LOCK

4.2.73 ACPI Timer Control (ACPI_TMR_CTL) — Offset 18FCh

This register allows software to disable the ACPI Timer, which could result in power savings for the PCH.

This register is in the CORE power well and is reset by host_prim_rst_b

Type	Size	Offset	Default
MMIO	32 bit	BAR + 18FCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**ACPI Timer Disable (ACPI_TIM_DIS):** This bit determines whether the ACPI Timer is enabled to run. Note that even when enabled, the timer only runs during S0. - 0: ACPI Timer is enabled (default) - 1: ACPI Timer is disabled (halted at the current value)
0	0h RW/1S/V	**ACPI Timer Clear (ACPI_TIM_CLR):** Writing a 1 to this bit will clear the ACPI Timer to all 0s. Hardware will automatically clear the bit back to '0' once the timer clear operation has completed. Writing a 0 to this bit has no effect. Implementation Note: The PCH must be capable of honoring this bit even while ACPI_TIM_DIS=1.

4.2.74 Last TSC Alarm Value[31:0] (TSC_ALARM_LO) — Offset 1910h

This register is in the CORE power well and is reset by host_prim_rst_b.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1910h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Last TSC Alarm Value [31:0] (TSC_ALARM_VAL_LO):** This field contains bits 31:0 of the last TSC alarm value received from the CPU.

4.2.75 Last TSC Alarm Value[63:32] (TSC_ALARM_HI) — Offset 1914h

This register is in the CORE power well and is reset by host_prim_rst_b.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1914h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Last TSC Alarm Value [63:32] (TSC_ALARM_VAL_HI):** This field contains bits 63:32 of the last TSC alarm value received from the CPU.

4.2.76 GPIO Configuration (GPIO_CFG) — Offset 1920h

This register is in the PRIMARY power well and is reset by global_rst_b.

reset_type=global_rst_b

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1920h	00000432h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:8	4h RW	**GPIO Group to GPE_DW2 assignment encoding (GPE0_DW2):** This register assigns a specific GPIO Group to the ACPI GPE0[96:64]. 0h = GPPC_G (GPI_GPE_STS/EN) 1h = GPPC_B 2h = GPPC_A 3h = GPP_R 4h = GPP_S 5h = GPD 6h = GPPC_H 7h = GPPC_D 8h = GPP_F 9h = vGPIO Ah = GPPC_C Bh = GPPC_E

Bit Range	Default & Access	Field Name (ID): Description
7:4	3h RW	**GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. 0h = GPPC_G (GPI_GPE_STS/EN) 1h = GPPC_B 2h = GPPC_A 3h = GPP_R 4h = GPP_S 5h = GPD 6h = GPPC_H 7h = GPPC_D 8h = GPP_F 9h = vGPIO Ah = GPPC_C Bh = GPPC_E
3:0	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. 0h = GPPC_G (GPI_GPE_STS/EN) 1h = GPPC_B 2h = GPPC_A 3h = GPP_R 4h = GPP_S 5h = GPD 6h = GPPC_H 7h = GPPC_D 8h = GPP_F 9h = vGPIO Ah = GPPC_C Bh = GPPC_E

4.2.77 Latency Limit Residency 0 (LAT_LIM_RES_0) — Offset 1930h

Latency Limit Residency 0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1930h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**LLR0:** This field contains the amount of time (in 100us granularity) for the corresponding 0/1/2 counter in the LATENCY_LIMIT_CONTROL register that the appropriate counter is limiting the memory LTR request to the CPU. Note that this counter can wrap and that should not be of any concern. This register will reset to 0 anytime the corresponding enable for the register transitions from a 0->1. Note that on a 1->0 transition, the counter should hold its previous value

4.2.78 Latency Limit Residency 1 (LAT_LIM_RES_1) — Offset 1934h

Latency Limit Residency 1

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1934h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**LLR1:** This field contains the amount of time (in 100us granularity) for the corresponding 0/1/2 counter in the LATENCY_LIMIT_CONTROL register that the appropriate counter is limiting the memory LTR request to the CPU. Note that this counter can wrap and that should not be of any concern. This register will reset to 0 anytime the corresponding enable for the register transitions from a 0->1. Note that on a 1->0 transition, the counter should hold its previous value

4.2.79 Latency Limit Residency 2 (LAT_LIM_RES_2) — Offset 1938h

Latency Limit Residency 2

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1938h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**LLR2:** This field contains the amount of time (in 100us granularity) for the corresponding 0/1/2 counter in the LATENCY_LIMIT_CONTROL register that the appropriate counter is limiting the memory LTR request to the CPU. Note that this counter can wrap and that should not be of any concern. This register will reset to 0 anytime the corresponding enable for the register transitions from a 0->1. Note that on a 1->0 transition, the counter should hold its previous value

4.2.80 SLP_S0 Residency (SLP_S0_RESIDENCY) — Offset 193Ch

SLP_S0 Residency

Type	Size	Offset	Default
MMIO	32 bit	BAR + 193Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RESIDENCY_IN_S0:** This field contains the amount of time that the SLP_S0 has been asserted before. Note that this counter can wrap and that should not be of any concern. It will also count in 122us granularity

4.2.81 Latency Limit Control (LATENCY_LIMIT_CONTROL) — Offset 1940h

Latency Limit Control

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1940h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22	0h RW	**CTR2_ENABLE:** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0
21	0h RW	**CTR2_EA_CTL:** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0

Bit Range	Default & Access	Field Name (ID): Description
20:16	00h RW	**CTR2_DEVICE:** Encoding of the LTR device to be monitored 0 - SPA 1 - SPB 2 - SPC 3 - SATA 4 - GbE 5 - XHCI 6 - ME 7 - EVA 8 - AZ 9 - ESPI 10 - LPSS 11 - SPD 12 - SPE (Reserved for LP) 13 - SPF (Reserved for LP) 14 - SDX 15 - OSE 16 - Reserved 17 - EMMC 18 - Reserved 19 - WIGIG 20 - THC0 21 - THC1
15	0h RO	**Reserved**
14	0h RW	**CTR1_ENABLE:** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0
13	0h RW	**CTR1_EA_CTL:** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0

Bit Range	Default & Access	Field Name (ID): Description
12:8	00h RW	**CTR1_DEVICE:** Encoding of the LTR device to be monitored 0 - SPA 1 - SPB 2 - SPC 3 - SATA 4 - GbE 5 - XHCI 6 - ME 7 - EVA 8 - AZ 9 - ESPI 10 - LPSS 11 - SPD 12 - SPE (Reserved for LP) 13 - SPF (Reserved for LP) 14 - SDX 15 - OSE 16 - Reserved 17 - EMMC 18 - Reserved 19 - WIGIG 20 - THC0 21 - THC1
7	0h RO	**Reserved**
6	0h RW	**CTR0_ENABLE:** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0
5	0h RW	**CTR0_EA_CTL:** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0

Bit Range	Default & Access	Field Name (ID): Description
4:0	00h RW	**CTR0_DEVICE:** Encoding of the LTR device to be monitored 0 - SPA 1 - SPB 2 - SPC 3 - SATA 4 - GbE 5 - XHCI 6 - ME 7 - EVA 8 - AZ 9 - ESPI 10 - LPSS 11 - SPD 12 - SPE (Reserved for LP) 13 - SPF (Reserved for LP) 14 - SDX 15 - OSE 16 - Reserved 17 - EMMC 18 - Reserved 19 - WIGIG 20 - THC0 21 - THC1

4.2.82 DBG SLP S0 WAKE1 (DBG_SLP_S0_WAKE1) — Offset 1A78h

This register captures the value of SLP_S0 wake events whenever the SLP_S0 s/m moves out of the SLP_S0 state. This register is in the core power well and it is reset by pmc_pltrst_b.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1A78h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**CLKRQ:** This bit indicates the combined PCIECLKREQ state.
30	0h RW/1S/V	**PMSYNC_REQ:** PM_SYNC activity indication.
29	0h RW/1S/V	**PLT_COND:** Platform latence indication.

Bit Range	Default & Access	Field Name (ID): Description
28	0h RW/1S/V	**FIVR_WAKE:** FIVR SLP_S0 wake indication.
27	0h RW/1S/V	**EA:** This bit indicates the state of EA.
26	0h RW/1S/V	**AON2 Trunk Gated Indication (AON2_TRUNK_GATED):** AON2 trunk gated indication.
25	0h RW/1S/V	**GBL_RST_REQ:** Global reset request indication.
24	0h RW/1S/V	**PMC_IDLE:** Internal PMC idle indication.
23	0h RW/1S/V	**CPU_PKG_C10:** CPU package C10 indication.
22	0h RW/1S/V	**ISCLK_PLL_OFF:** ISCLK PLL OFF indication.
21	0h RW/1S/V	**MPHY_OFF:** MPHY power gated indication.
20	0h RW/1S/V	**AUDIO_PLL_OFF:** Audio PLL off indication.
19	0h RW/1S/V	**XTAL_OFF:** XTAL off indication.
18	0h RW/1S/V	**ADSP_D3:** ADSP D3 indication.
17	0h RW/1S/V	**ADSP_ROSC_OFF:** ADSP_ROSC_OFF indication.
16	0h RW/1S/V	**FIA_PM_REQ:** FIA_PM_REQ to PMC.
15	0h RW/1S/V	**USB2 powergated (USB2_PG):** USB2 power gated indication.
14	0h RW/1S/V	**USB2 PLLOFF (USB2_PLLOFF):** USB2 PLL OFF indication.
13	0h RW/1S/V	**XHCI D3 (XHCI_D3):** XHCI D3 indication.
12	0h RW/1S/V	**GbE Connected (GBE_CONNECTED):** GbE device connected indication.
11	0h RW/1S/V	**LPSS D3 (LPSS_D3):** LPSS D3 indication.
10	0h RW/1S/V	**Thermal Sensor Disabled (THRM_SENS_DISABLED):** Thermal Sensor Disabled indication.
9	0h RW/1S/V	**SDX D3 (SDX_D3):** SDx D3 indication.
8	0h RW/1S/V	**EMMC D3 (EMMC_D3):** EMMC D3 indication.
7	0h RW/1S/V	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**Reserved**
5	0h RW/1S/V	**Reserved**
4	0h RW/1S/V	**SP DEEP PM (SP_DEEPPM):** Deep PM indication of all south port controllers.
3	0h RW/1S/V	**SATA D3 (SATA_D3):** SATA D3 indication.
2	0h RW/1S/V	**OTG D3 (OTG_D3):** OTG D3 indication.
1	0h RW/1S/V	**ITSS CLKREQ (ITSS_CLKREQ):** ITSS CLKREQ indication.
0	0h RW/1S/V	**ISH VNNREQ (ISH_VNNREQ):** ISH VNN REQ indication.

4.2.83 DBG SLP S0 WAKE2 (DBG_SLP_S0_WAKE2) — Offset 1A7Ch

This register captures the value of SLP_S0 wake events whenever the SLP_S0 s/m moves out of the SLP_S0 state. This register is in the core power well and it is reset by pmc_pltrst_b.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1A7Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW/1S/V	**IOTG PLL SHUTDOWN (IOTG_PLL_OFF):** IOTG PLL shutdown indication.
6	0h RW/1S/V	**CSME POWER GATING (CSME_POWER_GATING):** CSME Power gating indication.
5	0h RW/1S/V	**TSC ALARM EXPIRATION (TSC_ALARM_EXPIRATION):** TSC ALARM indication.
4	0h RW/1S/V	**ISH VNNAONREQ (ISH_VNNAONREQ):** ISH VNNAON request indication.
3	0h RW/1S/V	**CNV_VNNREQ:** CNV VNNREQ indication
2	0h RW/1S/V	**LPC_AGG_CLKREQ:** LPC Aggregated Clockreq Indication.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW/1S/V	Reserved
0	0h RW/1S/V	Reserved

4.2.84 CWB MDID Status Register (CWBMDIDSTATUS) — Offset 1BD4h

CWB MDID Status Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1BD4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**CWB Status (CWB_STS):** When set, DMI Central Write Buffer is enabled. Reflects DMI's np_pmc_cwb_en_ack status. 1: CWB on 0: CWB off
30:27	0h RO	**Reserved**
26:18	000h RW/V	**WIGIG MDID Value (WIGIG_MDID):** WIGIG sent MDID value.
17:9	000h RW/V	**DMI MDID Value (DMI_MDID):** DMI sent MDID value.
8:0	000h RW/V	Reserved

4.2.85 ACPI Control (ACTL) — Offset 1BD8h

ACPI Control

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1BD8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**ACPI Enable (EN):** When set, decode of the I/O range pointed to by the ACPI base register is enabled and the ACPI power management function is enabled.
6:3	0h RO	**Reserved**
2:0	0h RW	**SCI IRQ Select (SCIS):** Specifies on which IRQ the SCI will internally appear. If not using the APIC, the SCI must be routed to IRQ[9-11], and that interrupt is not sharable with the SERIRQ stream, but is shareable with other PCI interrupts. If using the APIC, the SCI can also be mapped to IRQ20-23, and can be shared with other interrupts. Bits - SCI Map ---- - ------- 000 - IRQ9 001 - IRQ10 010 - IRQ11 011 - Reserved 100 - IRQ20 (only if APIC is enabled) 101 - IRQ21 (only if APIC is enabled) 110 - IRQ22 (only if APIC is enabled) 111 - IRQ23 (only if APIC is enabled) When the interrupt is mapped to APIC interrupts 9, 10 or 11, the APIC should be programmed for active-high reception. When the interrupt is mapped to APIC interrupts 20 through 23, the APIC should be programmed for active-low reception.

4.2.86 Clock Source Shutdown Control Reg 2 (CS_SD_CTL2) — Offset 1BECh

This register configures if and how CPPM interacts with PCH clock gating and PLL shutdown.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1BECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW	**Clock Source 6 Override Value (CS6_OVR_VAL):** See CS1_OVR_VAL; when CS6_OVR_EN = 1, CS6_OVR_VAL will be driven on the FORCE_ON signal for clock source 6.
28	0h RW	**Clock Source 5 Override Value (CS5_OVR_VAL):** See CS1_OVR_VAL; when CS5_OVR_EN = 1, CS5_OVR_VAL will be driven on the FORCE_ON signal for clock source 5.
27	0h RW	**Clock Source 4 Override Value (CS4_OVR_VAL):** See CS1_OVR_VAL; when CS4_OVR_EN = 1, CS5_OVR_VAL will be driven on the FORCE_ON signal for clock source 4.
26	0h RW	**Clock Source 3 Override Value (CS3_OVR_VAL):** See CS1_OVR_VAL; when CS3_OVR_EN = 1, CS5_OVR_VAL will be driven on the FORCE_ON signal for clock source 3.
25	0h RW	**Clock Source 5 Override Value (CS2_OVR_VAL):** See CS1_OVR_VAL; when CS2_OVR_EN = 1, CS5_OVR_VAL will be driven on the FORCE_ON signal for clock source 2.
24	0h RW	**Clock Source 1 Override Value (CS1_OVR_VAL):** See CS1_OVR_VAL; when CS1_OVR_EN = 1, CS5_OVR_VAL will be driven on the FORCE_ON signal for clock source 1.
23:22	0h RO	**Reserved**
21	0h RW	**Clock Source 6 Override Enable (CS6_OVR_EN):** See CS1_OVR_EN; when CS6_OVR_EN = 1, CS6_OVR_VAL will be driven on the FORCE_ON signal for clock source 6.
20	0h RW	**Clock Source 5 Override Enable (CS5_OVR_EN):** See CS1_OVR_EN; when CS5_OVR_EN = 1, CS5_OVR_VAL will be driven on the FORCE_ON signal for clock source 5.
19	0h RW	**Clock Source 4 Override Enable (CS4_OVR_EN):** See CS1_OVR_EN; when CS4_OVR_EN = 1, CS4_OVR_VAL will be driven on the FORCE_ON signal for clock source 4.
18	0h RW	**Clock Source 3 Override Enable (CS3_OVR_EN):** See CS1_OVR_EN; when CS3_OVR_EN = 1, CS3_OVR_VAL will be driven on the FORCE_ON signal for clock source 3.
17	0h RW	**Clock Source 2 Override Enable (CS2_OVR_EN):** See CS1_OVR_EN; when CS2_OVR_EN = 1, CS2_OVR_VAL will be driven on the FORCE_ON signal for clock source 2.
16	0h RW	**Clock Source 1 Override Enable (CS1_OVR_EN):** See CS1_OVR_EN; when CS1_OVR_EN = 1, CS1_OVR_VAL will be driven on the FORCE_ON signal for clock source 1.

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RW	**Clock Source 6 EA Enable (CS6_EA_EN):** See CS1_EA_EN; controls application of EA value to shutting down clock source 5.
4	0h RW	**Clock Source 5 EA Enable (CS5_EA_EN):** See CS1_EA_EN; controls application of EA value to shutting down clock source 5.
3	0h RW	**Clock Source 4 EA Enable (CS4_EA_EN):** See CS1_EA_EN; controls application of EA value to shutting down clock source 4.
2	0h RW	**Clock Source 3 EA Enable (CS3_EA_EN):** See CS1_EA_EN; controls application of EA value to shutting down clock source 3.
1	0h RW	**Clock Source 2 EA Enable (CS2_EA_EN):** See CS1_EA_EN; controls application of EA value to shutting down clock source 2.
0	0h RW	**Clock Source 1 EA Enable (CS1_EA_EN):** When this bit is set to 1, the FORCE_ON signal for clock source 1 will always be 1 while EA is 1. This bit takes precedence over the CPPM dynamic qualifiers. So if this bit is 1 and EA is 1, FORCE_ON will be 1 even if the dynamic qualifiers are satisfied. Note: The static BIOS and PMC overrides, if enabled, will force FORCE_ON to 0 or 1 regardless of how this bit is programmed.

4.2.87 PGD PG_ACK Status Register 0 (PPASR0) — Offset 1D80h

PGD PG ACK Status Register 0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1D80h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Agent 31 Power Gate Ack Status (AGT31_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
30	0h RO/V	**Agent 30 Power Gate Ack Status (AGT30_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
29	0h RO/V	**Agent 29 Power Gate Ack Status (AGT29_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
28	0h RO/V	**Agent 28 Power Gate Ack Status (AGT28_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
27	0h RO/V	**Agent 27 Power Gate Ack Status (AGT27_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
26	0h RO/V	**Agent 26 Power Gate Ack Status (AGT26_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RO/V	**Agent 25 Power Gate Ack Status (AGT25_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
24	0h RO/V	**Agent 24 Power Gate Ack Status (AGT24_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
23	0h RO/V	**Agent 23 Power Gate Ack Status (AGT23_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
22	0h RO/V	**Agent 22 Power Gate Ack Status (AGT22_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
21	0h RO/V	**Agent 21 Power Gate Ack Status (AGT21_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
20	0h RO/V	**Agent 20 Power Gate Ack Status (AGT20_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
19	0h RO/V	**Agent 19 Power Gate Ack Status (AGT19_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
18	0h RO/V	**Agent 18 Power Gate Ack Status (AGT18_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
17	0h RO/V	**Agent 17 Power Gate Ack Status (AGT17_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
16	0h RO/V	**Agent 16 Power Gate Ack Status (AGT16_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
15	0h RO/V	**Agent 15 Power Gate Ack Status (AGT15_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
14	0h RO/V	**Agent 14 Power Gate Ack Status (AGT14_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
13	0h RO/V	**Agent 13 Power Gate Ack Status (AGT13_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
12	0h RO/V	**Agent 12 Power Gate Ack Status (AGT12_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
11	0h RO/V	**Agent 11 Power Gate Ack Status (AGT11_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
10	0h RO/V	**Agent 10 Power Gate Ack Status (AGT10_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
9	0h RO/V	**Agent 9 Power Gate Ack Status (AGT9_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
8	0h RO/V	**Agent 8 Power Gate Ack Status (AGT8_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
7	0h RO/V	**Agent 7 Power Gate Ack Status (AGT7_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
6	0h RO/V	**Agent 6 Power Gate Ack Status (AGT6_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
5	0h RO/V	**Agent 5 Power Gate Ack Status (AGT5_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
4	0h RO/V	**Agent 4 Power Gate Ack Status (AGT4_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
3	0h RO/V	**Agent 3 Power Gate Ack Status (AGT3_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO/V	**Agent 2 Power Gate Ack Status (AGT2_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
1	0h RO/V	**Agent 1 Power Gate Ack Status (AGT1_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
0	0h RO/V	**Agent 0 Power Gate Ack Status (AGT0_PG_ACK_STS):** This indicates the current status of the pmc_ip_pg_ack_b signal, corresponding to Agent ID [n]. 0: IP may be power gated (pg_ack_b asserted) 1: IP may not be power gated (pg_ack_b deasserted)

4.2.88 PGD PG_ACK Status Register 1 (PPASR1) — Offset 1D84h

PGD PG ACK Status Register 1

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1D84h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Agent 63 Power Gate Ack Status (AGT63_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
30	0h RO/V	**Agent 62 Power Gate Ack Status (AGT62_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
29	0h RO/V	**Agent 61 Power Gate Ack Status (AGT61_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
28	0h RO/V	**Agent 60 Power Gate Ack Status (AGT60_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
27	0h RO/V	**Agent 59 Power Gate Ack Status (AGT59_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
26	0h RO/V	**Agent 58 Power Gate Ack Status (AGT58_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
25	0h RO/V	**Agent 57 Power Gate Ack Status (AGT57_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
24	0h RO/V	**Agent 56 Power Gate Ack Status (AGT56_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
23	0h RO/V	**Agent 55 Power Gate Ack Status (AGT55_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
22	0h RO/V	**Agent 54 Power Gate Ack Status (AGT54_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
21	0h RO/V	**Agent 53 Power Gate Ack Status (AGT53_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO/V	**Agent 52 Power Gate Ack Status (AGT52_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
19	0h RO/V	**Agent 51 Power Gate Ack Status (AGT51_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
18	0h RO/V	**Agent 50 Power Gate Ack Status (AGT50_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
17	0h RO/V	**Agent 49 Power Gate Ack Status (AGT49_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
16	0h RO/V	**Agent 48 Power Gate Ack Status (AGT48_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
15	0h RO/V	**Agent 47 Power Gate Ack Status (AGT47_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
14	0h RO/V	**Agent 46 Power Gate Ack Status (AGT46_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
13	0h RO/V	**Agent 45 Power Gate Ack Status (AGT45_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
12	0h RO/V	**Agent 44 Power Gate Ack Status (AGT44_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
11	0h RO/V	**Agent 43 Power Gate Ack Status (AGT43_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
10	0h RO/V	**Agent 42 Power Gate Ack Status (AGT42_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
9	0h RO/V	**Agent 41 Power Gate Ack Status (AGT41_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
8	0h RO/V	**Agent 40 Power Gate Ack Status (AGT40_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
7	0h RO/V	**Agent 39 Power Gate Ack Status (AGT39_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
6	0h RO/V	**Agent 38 Power Gate Ack Status (AGT38_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
5	0h RO/V	**Agent 37 Power Gate Ack Status (AGT37_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
4	0h RO/V	**Agent 36 Power Gate Ack Status (AGT36_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
3	0h RO/V	**Agent 35 Power Gate Ack Status (AGT35_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
2	0h RO/V	**Agent 34 Power Gate Ack Status (AGT34_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
1	0h RO/V	**Agent 33 Power Gate Ack Status (AGT33_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.
0	0h RO/V	**Agent 32 Power Gate Ack Status (AGT32_PG_ACK_STS):** Please see PPASR0.AGT0_PG_ACK_STS for details.

4.2.89 PGD PFET Enable Ack Status Register 0 (PPFEAR0) — Offset 1D90h

PGD PFET Enable Ack Status Register 0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1D90h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Agent 31 PFET Enable Ack Status (AGT31_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
30	0h RO/V	**Agent 30 PFET Enable Ack Status (AGT30_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
29	0h RO/V	**Agent 29 PFET Enable Ack Status (AGT29_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
28	0h RO/V	**Agent 28 PFET Enable Ack Status (AGT28_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
27	0h RO/V	**Agent 27 PFET Enable Ack Status (AGT27_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
26	0h RO/V	**Agent 26 PFET Enable Ack Status (AGT26_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
25	0h RO/V	**Agent 25 PFET Enable Ack Status (AGT25_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
24	0h RO/V	**Agent 24 PFET Enable Ack Status (AGT24_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
23	0h RO/V	**Agent 23 PFET Enable Ack Status (AGT23_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
22	0h RO/V	**Agent 22 PFET Enable Ack Status (AGT22_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
21	0h RO/V	**Agent 21 PFET Enable Ack Status (AGT21_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
20	0h RO/V	**Agent 20 PFET Enable Ack Status (AGT20_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
19	0h RO/V	**Agent 19 PFET Enable Ack Status (AGT19_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
18	0h RO/V	**Agent 18 PFET Enable Ack Status (AGT18_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
17	0h RO/V	**Agent 17 PFET Enable Ack Status (AGT17_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
16	0h RO/V	**Agent 16 PFET Enable Ack Status (AGT16_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO/V	**Agent 15 PFET Enable Ack Status (AGT15_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
14	0h RO/V	**Agent 14 PFET Enable Ack Status (AGT14_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
13	0h RO/V	**Agent 13 PFET Enable Ack Status (AGT13_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
12	0h RO/V	**Agent 12 PFET Enable Ack Status (AGT12_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
11	0h RO/V	**Agent 11 PFET Enable Ack Status (AGT11_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
10	0h RO/V	**Agent 10 PFET Enable Ack Status (AGT10_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
9	0h RO/V	**Agent 9 PFET Enable Ack Status (AGT9_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
8	0h RO/V	**Agent 8 PFET Enable Ack Status (AGT8_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
7	0h RO/V	**Agent 7 PFET Enable Ack Status (AGT7_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
6	0h RO/V	**Agent 6 PFET Enable Ack Status (AGT6_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
5	0h RO/V	**Agent 5 PFET Enable Ack Status (AGT5_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
4	0h RO/V	**Agent 4 PFET Enable Ack Status (AGT4_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
3	0h RO/V	**Agent 3 PFET Enable Ack Status (AGT3_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
2	0h RO/V	**Agent 2 PFET Enable Ack Status (AGT2_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
1	0h RO/V	**Agent 1 PFET Enable Ack Status (AGT1_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
0	0h RO/V	**Agent 0 PFET Enable Ack Status (AGT0_PFET_EN_ACK_STS):** This is the value of the corresponding agent's fet_en_ack_b indication. 0 - PFET is turned ON 1 - PFET is turned OFF

4.2.90 PGD PFET Enable Ack Status Register 1 (PPFEAR1) — Offset 1D94h

PGD PFET Enable Ack Status Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1D94h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Agent 63 PFET Enable Ack Status (AGT63_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
30	0h RO/V	**Agent 62 PFET Enable Ack Status (AGT62_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
29	0h RO/V	**Agent 61 PFET Enable Ack Status (AGT61_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
28	0h RO/V	**Agent 60 PFET Enable Ack Status (AGT60_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
27	0h RO/V	**Agent 59 PFET Enable Ack Status (AGT59_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
26	0h RO/V	**Agent 58 PFET Enable Ack Status (AGT58_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
25	0h RO/V	**Agent 57 PFET Enable Ack Status (AGT57_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
24	0h RO/V	**Agent 56 PFET Enable Ack Status (AGT56_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
23	0h RO/V	**Agent 55 PFET Enable Ack Status (AGT55_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
22	0h RO/V	**Agent 54 PFET Enable Ack Status (AGT54_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
21	0h RO/V	**Agent 53 PFET Enable Ack Status (AGT53_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
20	0h RO/V	**Agent 52 PFET Enable Ack Status (AGT52_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
19	0h RO/V	**Agent 51 PFET Enable Ack Status (AGT51_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
18	0h RO/V	**Agent 50 PFET Enable Ack Status (AGT50_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
17	0h RO/V	**Agent 49 PFET Enable Ack Status (AGT49_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
16	0h RO/V	**Agent 48 PFET Enable Ack Status (AGT48_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
15	0h RO/V	**Agent 47 PFET Enable Ack Status (AGT47_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
14	0h RO/V	**Agent 46 PFET Enable Ack Status (AGT46_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO/V	**Agent 45 PFET Enable Ack Status (AGT45_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
12	0h RO/V	**Agent 44 PFET Enable Ack Status (AGT44_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
11	0h RO/V	**Agent 43 PFET Enable Ack Status (AGT43_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
10	0h RO/V	**Agent 42 PFET Enable Ack Status (AGT42_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
9	0h RO/V	**Agent 41 PFET Enable Ack Status (AGT41_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
8	0h RO/V	**Agent 40 PFET Enable Ack Status (AGT40_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
7	0h RO/V	**Agent 39 PFET Enable Ack Status (AGT39_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
6	0h RO/V	**Agent 38 PFET Enable Ack Status (AGT38_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
5	0h RO/V	**Agent 37 PFET Enable Ack Status (AGT37_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
4	0h RO/V	**Agent 36 PFET Enable Ack Status (AGT36_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
3	0h RO/V	**Agent 35 PFET Enable Ack Status (AGT35_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
2	0h RO/V	**Agent 34 PFET Enable Ack Status (AGT34_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
1	0h RO/V	**Agent 33 PFET Enable Ack Status (AGT33_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.
0	0h RO/V	**Agent 32 PFET Enable Ack Status (AGT32_PFET_EN_ACK_STS):** Please see PPFEAR0.AGT0_PFET_EN_ACK_STS for details.

4.2.91 Static PG Related Function Disable Register 1 (ST_PG_FDIS_PMC_1) — Offset 1E20h

Static PG Related Function Disable Register 1

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1E20h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Static Function Disable Lock (ST_FDIS_LK):** Lock control for all ST_PG_FDIS_PMC_* and NST_PG_FDIS_* registers (also self-locks when written to 1). **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
30:6	0h RO	**Reserved**
5	0h RW/L	**OSE Function Disable (PMC Version) (OSE_FDIS_PMC):** BIOS is required to set this bit when OSE function is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
4:2	0h RO	**Reserved**
1	0h RW/L	Reserved
0	0h RW/L	**GBE Function Disable (PMC Version) (GBE_FDIS_PMC):** BIOS is required to set this bit when GBE function is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK

4.2.92 Static Function Disable Control 2 Register (ST_PG_FDIS_PMC_2) — Offset 1E24h

Static Function Disable Control 2 Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1E24h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/L	**LPSS Controller GSPI Device 1 Function Disable (PMC Version) (LPSS_GSPI2_FDIS_PMC): (LPSS_GSPI2_FDIS_PMC):** BIOS is required to set this bit when this LPSS Device (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
10	0h RW/L	**LPSS Controller GSPI Device 1 Function Disable (PMC Version) (LPSS_GSPI1_FDIS_PMC): (LPSS_GSPI1_FDIS_PMC):** BIOS is required to set this bit when this LPSS Device (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
9	0h RW/L	**LPSS Controller GSPI Device 0 Function Disable (PMC Version) (LPSS_GSPI0_FDIS_PMC): (LPSS_GSPI0_FDIS_PMC):** BIOS is required to set this bit when this LPSS Device (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
8	0h RW/L	**LPSS Controller UART Device 2 Function Disable (PMC Version) (LPSS_UART2_FDIS_PMC): (LPSS_UART2_FDIS_PMC):** BIOS is required to set this bit when this LPSS Device (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
7	0h RW/L	**LPSS Controller UART Device 1 Function Disable (PMC Version) (LPSS_UART1_FDIS_PMC): (LPSS_UART1_FDIS_PMC):** BIOS is required to set this bit when this LPSS Device (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
6	0h RW/L	**LPSS Controller UART Device 0 Function Disable (PMC Version) (LPSS_UART0_FDIS_PMC): (LPSS_UART0_FDIS_PMC):** BIOS is required to set this bit when this LPSS Device (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
5	0h RW/L	**LPSS Controller I2C Device 5 Function Disable (PMC Version) (LPSS_I2C5_FDIS_PMC): (LPSS_I2C5_FDIS_PMC):** BIOS is required to set this bit when this LPSS Device (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
4	0h RW/L	**LPSS Controller I2C Device 4 Function Disable (PMC Version) (LPSS_I2C4_FDIS_PMC): (LPSS_I2C4_FDIS_PMC):** BIOS is required to set this bit when this LPSS Device (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
3	0h RW/L	**LPSS Controller I2C Device 3 Function Disable (PMC Version) (LPSS_I2C3_FDIS_PMC): (LPSS_I2C3_FDIS_PMC):** BIOS is required to set this bit when this LPSS Device (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
2	0h RW/L	**LPSS Controller I2C Device 2 Function Disable (PMC Version) (LPSS_I2C2_FDIS_PMC): (LPSS_I2C2_FDIS_PMC):** BIOS is required to set this bit when this LPSS Device (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
1	0h RW/L	**LPSS Controller I2C Device 1 Function Disable (PMC Version) (LPSS_I2C1_FDIS_PMC): (LPSS_I2C1_FDIS_PMC):** BIOS is required to set this bit when this LPSS Device (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/L	**LPSS Controller I2C Device 0 Function Disable (PMC Version) (LPSS_I2C0_FDIS_PMC): (LPSS_I2C0_FDIS_PMC):** BIOS is required to set this bit when this LPSS Device (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK

4.2.93 Non-Static PG Related Function Disable Register 1 (NST_PG_FDIS_1) — Offset 1E28h

Non-Static PG Related Function Disable Register 1

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1E28h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW/L	**SDX Function Disable (PMC Version) (SDX_FDIS_PMC):** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
28	0h RW/L	**EMMC Function Disable (PMC Version) (EMMC_FDIS_PMC):** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
27	0h RW/L	**Reserved**
26	0h RW/L	**XDCI Function Disable (PMC Version) (XDCI_FDIS_PMC):** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
25	0h RW/L	**SMB Function Disable (PMC Version) (SMB_FDIS_PMC):** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
24	0h RW/L	**LPC Function Disable (PMC Version) (LPC_FDIS_PMC):** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
23	0h RW/L	**ADSP Function Disable (PMC Version) (ADSP_FDIS_PMC):** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK

Bit Range	Default & Access	Field Name (ID): Description
22	0h RW/L	**SATA Controller Function Disable (PMC Version) (ST_FDIS_PMC):** BIOS is required to set this bit when the SATA controller (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
21:18	0h RO	**Reserved**
17	0h RW/L	**PCIe Controller D Port 3 Function Disable [PMC Version] (PCIE_D3_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
16	0h RW/L	**PCIe Controller D Port 2 Function Disable [PMC Version] (PCIE_D2_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
15	0h RW/L	**PCIe Controller D Port 1 Function Disable [PMC Version] (PCIE_D1_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
14	0h RW/L	**PCIe Controller D Port 0 Function Disable [PMC Version] (PCIE_D0_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
13	0h RW/L	**PCIe Controller C Port 3 Function Disable (PMC Version) (PCIE_C3_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
12	0h RW/L	**PCIe Controller C Port 2 Function Disable (PMC Version) (PCIE_C2_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
11	0h RW/L	**PCIe Controller C Port 1 Function Disable (PMC Version) (PCIE_C1_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
10	0h RW/L	**PCIe Controller C Port 0 Function Disable (PMC Version) (PCIE_C0_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
9	0h RW/L	**PCIe Controller B Port 3 Function Disable (PMC Version) (PCIE_B3_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/L	**PCIe Controller B Port 2 Function Disable (PMC Version) (PCIE_B2_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
7	0h RW/L	**PCIe Controller B Port 1 Function Disable (PMC Version) (PCIE_B1_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
6	0h RW/L	**PCIe Controller B Port 0 Function Disable (PMC Version) (PCIE_B0_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
5	0h RW/L	**PCIe Controller A Port 3 Function Disable (PMC Version) (PCIE_A3_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
4	0h RW/L	**PCIe Controller A Port 2 Function Disable (PMC Version) (PCIE_A2_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
3	0h RW/L	**PCIe Controller A Port 1 Function Disable (PMC Version) (PCIE_A1_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
2	0h RW/L	**PCIe Controller A Port 0 Function Disable (PMC Version) (PCIE_A0_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK
1	0h RO	**Reserved**
0	0h RW/L	**XHCI Function Disable (PMC Version) (XHCI_FDIS_PMC):** BIOS is required to set this bit when this IP block (single logical function) is configured to be function disabled. **Locked by:** ST_PG_FDIS_PMC_1.ST_FDIS_LK

4.2.94 Non-Static PG Fuse Disable Read 1 Register (N_STPG_FUSE_SS_DIS_RD_1) — Offset 1E40h

This register contains fuse disable based information - which is not used for static power gating (this information is provided only for host/BIOS read access).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1E40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RO/V	**PCIe Controller D Port 3 Fuse Disable (PCIE_D3_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is fuse disabled.
16	0h RO/V	**PCIe Controller D Port 2 Fuse Disable (PCIE_D2_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is fuse disabled.
15	0h RO/V	**PCIe Controller D Port 1 Fuse Disable (PCIE_D1_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is fuse disabled.
14	0h RO/V	**PCIe Controller D Port 0 Fuse Disable (PCIE_D0_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is fuse disabled.
13	0h RO/V	**PCIe Controller C Port 3 Fuse Disable (PCIE_C3_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is fuse disabled.
12	0h RO/V	**PCIe Controller C Port 2 Fuse Disable (PCIE_C2_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is fuse disabled.
11	0h RO/V	**PCIe Controller C Port 1 Fuse Disable (PCIE_C1_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is fuse disabled.
10	0h RO/V	**PCIe Controller C Port 0 Fuse Disable (PCIE_C0_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is fuse disabled.
9	0h RO/V	**PCIe Controller B Port 3 Fuse Disable (PCIE_B3_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is fuse disabled.
8	0h RO/V	**PCIe Controller B Port 2 Fuse Disable (PCIE_B2_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is fuse disabled.
7	0h RO/V	**PCIe Controller B Port 1 Fuse Disable (PCIE_B1_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is fuse disabled.
6	0h RO/V	**PCIe Controller B Port 0 Fuse Disable (PCIE_B0_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is fuse disabled.
5	0h RO/V	**PCIe Controller A Port 3 Fuse Disable (PCIE_A3_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is fuse disabled.
4	0h RO/V	**PCIe Controller A Port 2 Fuse Disable (PCIE_A2_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is fuse disabled.
3	0h RO/V	**PCIe Controller A Port 1 Fuse Disable (PCIE_A1_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is fuse disabled.
2	0h RO/V	**PCIe Controller A Port 0 Fuse Disable (PCIE_A0_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is fuse disabled.
1	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO/V	**XHCI Fuse Disable (XHCI_FUSE_DIS):** XHCI fuse disable placeholder if this information is used by PMC due to specific XHCI requirements.

4.2.95 Static PG Fuse and Soft Strap Disable Read Register 2 (STPG_FUSE_SS_DIS_RD_2) — Offset 1E44h

This register contains fuse and soft strap disable based information - all of which is used for static power-gating (for example, if a bit is set in this register for a particular IP, PMC keeps that IP in a power-gated state - except as noted below.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1E44h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RO/V	**ISI Fuse or Soft Strap Disable (ISI_FUSE_SS_DIS):** RO bit indicating if ISI function is disabled through fuse/soft strap. Note: Each port within this function has individual disable fuse - listed in N_STPG_FUSE_SS_DIS_RD_1 register that does not contribute to static power gating.
29	0h RO/V	**TBTLSX Fuse or Soft Strap Disable (TBTLSX_FUSE_SS_DIS):** RO bit indicating if TBTLSX function is disabled through fuse/soft strap. Note: Each port within this function has individual disable fuse - listed in N_STPG_FUSE_SS_DIS_RD_1 register that does not contribute to static power gating.
28	0h RO/V	**WIGIG Fuse or Soft Strap Disable (WIGIG_FUSE_SS_DIS):** RO bit indicating if WIGIG function is disabled through fuse or soft strap.
27	0h RO	**Reserved**
26	0h RO/V	**SPD Soft Strap Disable (SPD_SS_DIS):** RO bit indicating if SPD function is disabled through soft strap. Note: Each port within this function has individual disable fuse - listed in N_STPG_FUSE_SS_DIS_RD_1 register that does not contribute to static power gating.
25	0h RO/V	**SPC Soft Strap Disable (SPC_SS_DIS):** RO bit indicating if SPC function is disabled through soft strap. Note: Each port within this function has individual disable fuse - listed in N_STPG_FUSE_SS_DIS_RD_1 register that does not contribute to static power gating.

Bit Range	Default & Access	Field Name (ID): Description
24	0h RO/V	**SPB Soft Strap Disable (SPB_SS_DIS):** RO bit indicating if SPB function is disabled through fuse/soft strap. Note: Each port within this function has individual disable fuse - listed in N_STPG_FUSE_SS_DIS_RD_1 register that does not contribute to static power gating.
23	0h RO/V	**SPA Soft Strap Disable (SPA_SS_DIS):** RO bit indicating if SPA function is disabled through soft strap. Note: Each port within this function has individual disable fuse - listed in N_STPG_FUSE_SS_DIS_RD_1 register that does not contribute to static power gating.
22	0h RO/V	**PPBR Fuse or Soft Strap Disable (PPBR_SS_DIS):** RO bit indicating if PPBR function is disabled through soft strap.
21	0h RO/V	**PSTH Fuse or Soft Strap Disable (PSTH_FUSE_SS_DIS):** RO bit indicating if PSTH function is disabled through fuse/soft strap.
20	0h RO/V	**DMI Fuse or Soft Strap Disable (DMI_FUSE_SS_DIS):** RO bit indicating if DMI function is disabled through fuse/soft strap.
19	0h RO/V	**XDCI Fuse or Soft Strap Disable (XDCI_FUSE_SS_DIS):** RO bit indicating if XDCI function is disabled through fuse/soft strap.
18	0h RO/V	**XHCI Soft Strap Disable (XHCI_SS_DIS):** RO bit indicating if XHCI function is disabled through soft strap. Note: This is intended for use only as a debug tool (to work around any issues related to XHCI in reset/boot/Sx entry flows), since disabling XHCI prevents ModPhy power-gating on the lanes driven by the XHCI controller. The corresponding XHCI disable fuse bit is located in N_STPG_FUSE_SS_DIS_RD_1 register.
17	0h RO/V	**FIA Fuse or Soft Strap Disable (FIA_FUSE_SS_DIS):** RO bit indicating if FIA function is disabled through fuse/soft strap.
16	0h RO/V	**DSP Fuse or Soft Strap Disable (DSP_FUSE_SS_DIS):** RO bit indicating if DSP function is disabled through fuse/soft strap.
15	0h RO/V	**SATA Fuse or Soft Strap Disable (SATA_FUSE_SS_DIS):** RO bit indicating if SATA function is disabled through fuse/soft strap.
14	0h RO/V	**ICC Fuse or Soft Strap Disable (ICC_FUSE_SS_DIS):** RO bit indicating if ICC function is disabled through fuse/soft strap.
13	0h RO/V	**LPC Fuse or Soft Strap Disable (LPC_FUSE_SS_DIS):** RO bit indicating if LPC function is disabled through fuse/soft strap.
12	0h RO/V	**RTC Fuse or Soft Strap Disable (RTC_FUSE_SS_DIS):** RO bit indicating if RTC function is disabled through fuse/soft strap.
11	0h RO/V	**P2S Fuse or Soft Strap Disable (P2S_FUSE_SS_DIS):** RO bit indicating if P2S function is disabled through fuse/soft strap.
10	0h RO/V	**TRSB Fuse or Soft Strap Disable (TRSB_FUSE_SS_DIS):** RO bit indicating if TRSB function is disabled through fuse/soft strap.
9	0h RO/V	**SMB Fuse or Soft Strap Disable (SMB_FUSE_SS_DIS):** RO bit indicating if SMB function is disabled through fuse/soft strap.
8	0h RO/V	**ITSS Fuse or Soft Strap Disable (ITSS_FUSE_SS_DIS):** RO bit indicating if ITSS function is disabled through fuse/soft strap.
7	0h RO/V	Reserved
6	0h RO/V	**LPSS Fuse or Soft Strap Disable (LPSS_FUSE_SS_DIS):** RO bit indicating if LPSS function is disabled through fuse/soft strap.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO/V	**EMMC Fuse or Soft Strap Disable (EMMC_FUSE_SS_DIS):** RO bit indicating if EMMC function is disabled through fuse/soft strap.
4	0h RO/V	Reserved
3	0h RO/V	**P2D Fuse or Soft Strap Disable (P2D_FUSE_SS_DIS):** RO bit indicating if 2D function is disabled through fuse/soft strap.
2	0h RO/V	**SD Controller Fuse or Soft Strap Disable (SDX_FUSE_SS_DIS):** RO bit indicating if SD Controller function is disabled through fuse/soft strap.
1	0h RO/V	**ISH Fuse or Soft Strap Disable (ISH_FUSE_SS_DIS):** RO bit indicating if OSE function is disabled through fuse or soft strap.
0	0h RO/V	**GBE Fuse or Soft Strap Disable (GBE_FUSE_SS_DIS):** RO bit indicating if GBE function is disabled through fuse or Soft strap.

4.2.96 CPPMVRIC3 CPPM VR Idle Control 3 (CPPMVRIC3) — Offset 1E4Ch

This register contains misc. configuration related to SLP_S0# control / VR Idle.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1E4Ch	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**SLPS0_PIN_MODE:** This bit determines whether the behavior of the SLP_S0# pin is driven by the CPPMVRIC logic/register bit policies or the LPM logic/register bit policies. 0: SLP_S0# behavior driven by LPM logic 1: SLP_S0# behavior driven by CPPMVRIC logic
30:25	0h RO	**Reserved**
24	0h RW	**IOTG PLL force off enable (IPLLFOEN):** 0 IOTG PLL force_off signal to ICC is not asserted following graceful park assertion 1 =IOTG PLL force_off signal to ICC is asserted following graceful_park assertion
23	0h RW	**IOTG PLL is off Qualification Disable (IPLLSDQDIS):** 0 SLP_S0# assertion requires the IOTG PLL to be shut down. 1 =SLP_S0# assertion does not require the IOTG PLL to be shut down
22	0h RW	**IOTG PLL Graceful Park Enable (IPLLGPEN):** 0 PMC does not assert the graceful_park signal to ICC for the IOTG PLL prior to asserting SLP_S0# to 0 1 = PMC asserts the graceful_park signal to ICC for the IOTG PLL prior to asserting SLP_S0#

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**AON1 ROSC force off enable (AON1ROSCFOEN):** 0 Aon1 ROSC force_off signal to ICC is not asserted following graceful park assertion 1 =Aon1 ROSC force_off signal to ICC is asserted following graceful_park assertion
20	0h RW	**AON1 CLK_ACK Mask (AON1_CLKACK_MASK):** 1 PMC does not wait for the aggregated AON1 CLK_ACK to de-assert during graceful_park handshake prior to asserting SLP_S0# to 0 0 = PMC waits for the aggregated AON1 CLK_ACK to de-assert during graceful_park handshake prior to asserting SLP_S0#
19	0h RW	**AON2 CLK_ACK Mask (AON2_CLKACK_MASK):** 1 PMC does not wait for the aggregated AON2 CLK_ACK to de-assert during graceful_park handshake prior to asserting SLP_S0# to 0 0 = PMC waits for the aggregated AON2 CLK_ACK to de-assert during graceful_park handshake prior to asserting SLP_S0#
18	0h RW	**AON1 ROSC Graceful Park Enable (AON1ROSCTGPEN):** 0 PMC does not assert the graceful_park signal to ICC for the AON1 ROSC trunks (rosc_clk, rosc_med_clk, rosc_s0ix_clk) prior to asserting SLP_S0# to 0 1 = PMC asserts the graceful_park signal to ICC for the AON1 ROSC trunks (rosc_slow_clk, rosc_med_clk, rosc_s0ix_clk) prior to asserting SLP_S0#
17	0h RW	**Audio PLL Graceful Park Disable (APLLGPEN):** 1 PMC does not assert the graceful_park signal to ICC for the Audio PLL prior to asserting SLP_S0# 0 = PMC asserts the graceful_park signal to ICC for the Audio PLL prior to asserting SLP_S0#
16	0h RW	**Dynamic Flex IO Change is not in progress Qualification Disable (DFLEXIOQDIS):** 0 SLP_S0# assertion requires that a Flex IO change is not in progress 1 =SLP_S0# assertion does not require that Flex IO change is not in progress
15	0h RW	**USB SUS Power Gate Qualification Disable (USBSUSPGQDIS):** 0 SLP_S0# assertion requires the USB2 PHY sus power gate domain to be gated 1 =SLP_S0# assertion does not require the USB2 PHY sus power gate domain to be gated
14:13	0h RO	**Reserved**
12	0h RW	**GPIO S0iX CLOCK Switch Enable (GPIOS0IXCKSEN):** 1 PMC switches the GPIO controllers from 24MHz to 3 MHz clock domain prior to asserting SLP_S0# 0 = PMC does not switch the GPIO controllers from 24MHz to 3 MHz clock domain prior to asserting SLP_S0#
11	0h RW	**Audio PLL force_off enable (APLLFOEN):** 0 Audio PLL force_off signal to ICC is not asserted following graceful_park assertion 1 = Audio PLL force_off signal to ICC is asserted following graceful_park assertion
10	0h RW	**ADSPROSC force_off enable (ADSPROSCFOEN):** 0 ADSPROSC force_off signal to ICC is not asserted following graceful_park assertion 1 = ADSPROSC force_off signal to ICC is asserted following graceful_park assertion
9	0h RW	**CLKOUT_LPC force_off enable (LPCCLKFOEN):** 0 = CLKOUT_LPC force_off signal to ICC is not asserted following graceful_park assertion 1 = CLKOUT_LPC force_off signal to ICC is asserted following graceful_park assertion
8	0h RW	**ISCLK PLL force_off enable (ICCPLLFOEN):** 0 = ISCLK PLL force_off signal to ICC is not asserted following graceful_park assertion 1 = ISCLK PLL force_off signal to ICC is asserted following graceful_park assertion

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**AON2 ROSC force_off enable (AON2ROSCFOEN):** 0 = ROSC force_off signal to ICC is not asserted following graceful_park assertion 1 = ROSC force_off signal to ICC is asserted following graceful_park assertion
6	0h RW	**XTAL force_off enable (XTALFOEN):** 0 = XTAL force_off signal to ICC is not asserted following graceful_park assertion 1 = XTAL force_off signal to ICC is asserted following graceful_park assertion
5	0h RW	**PMC Clock Switch Disable (PMCCLKDIS):** 0 = PMC switches to a low speed ROSC during SLP_S0# entry 1 = PMC does not switch to a low speed ROSC during SLP_S0#
4	0h RW	**Reserved**
3	0h RW	**Reserved**
2	0h RW	**SDX (SD3/4/SDIO) Controller in D3 Qualification Disable (SDCD3QDIS) (SDCD3QDIS):** 0 = SLP_S0# assertion requires the SDX controller to be in D3 1 = SLP_S0# assertion does not require the SDX controller to be in D3
1	0h RW	**eMMC Controller in D3 Qualification Disable (EMMCD3QDIS):** 0 = SLP_S0# assertion requires the eMMC controller to be in D3 1 = SLP_S0# assertion does not require the eMMC controller to be in D3
0	1h RW	**SD4 PLL Shutdown Qualification Disable (SD4PLLSDQDIS):** 0 = SLP_S0# assertion requires the SD4 PLL to be shut down. 1 = SLP_S0# assertion does not require the SD4 PLL to be shut down.

4.3 PMC ACPI IO Registers Summary

Table 4-3. Summary of PMC ACPI IO Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Power Management 1 Enables and Status (PM1_EN_STS)	00000000h
4h	4	Power Management 1 Control (PM1_CNT)	00000000h
8h	4	Power Management 1 Timer (PM1_TMR)	00000000h
20h	4	Therm Timer Delay Register (THERM_TIMER_DELAY)	00000000h
30h	4	SMI Control and Enable (SMI_EN)	00000002h
34h	4	SMI Status Register (SMI_STS)	00000000h
40h	4	General Purpose Event Control (GPE_CTRL)	00000000h
44h	4	Device Trap Status Register (DEVTRAP_STS)	00000000h
50h	4	PM2a Control Block (PM2A_CNT_BLK)	00000000h
54h	4	Over-Clocking WDT Control (OC_WDT_CTL)	00002000h
60h	4	General Purpose Event 0 Status [31:0] (GPE0_STS_31_0)	00000000h
64h	4	General Purpose Event 0 Status [63:32] (GPE0_STS_63_32)	00000000h
68h	4	General Purpose Event 0 Status [95:64] (GPE0_STS_95_64)	00000000h
6Ch	4	General Purpose Event 0 Status [127:96] (GPE0_STS_127_96)	00000000h
70h	4	General Purpose Event 0 Enable [31:0] (GPE0_EN_31_0)	00000000h
74h	4	General Purpose Event 0 Enable [63:32] (GPE0_EN_63_32)	00000000h
78h	4	General Purpose Event 0 Enable [95:64] (GPE0_EN_95_64)	00000000h
7Ch	4	General Purpose Event 0 Enable [127:96] (GPE0_EN_127_96)	00000000h

4.3.1 Power Management 1 Enables and Status (PM1_EN_STS) — Offset 0h

Power Management 1 Enables and Status

Type	Size	Offset	Default
MMIO	32 bit	BAR + 0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RW	**PCI Express Wake Disable (PCIEXP_WAKE_DIS):** This bit disables the inputs to the PCIEXP_WAKE_STS bit in the PM1 Status register from waking the system. Modification of this bit has no impact on the value of the PCIEXP_WAKE_STS bit.

Bit Range	Default & Access	Field Name (ID): Description
29:27	0h RO	**Reserved**
26	0h RW/V	**RTC Alarm Enable (RTC_EN):** This is the RTC alarm enable bit. It works in conjunction with the SCI_EN bit: RTC_EN SCI_EN Effect when RTC_STS is set 0 x No SMI# or SCI. If system was in S1-S5, no wake even occurs. 1 0 SMI#. If system was in S1-S5, then a wake event occurs before the SMI#. 1 1 SCI. If system was in S1-S5, then a wake event occurs before the SCI. Note: This bit needs to be backedby the RTC well to allow an RTC event to wake after a power failure.
25	0h RO	**Reserved**
24	0h RW/V	**Power Button Enable (PWRBTN_EN):** This bit is the power button enable. It works in conjunction with the SCI_EN bit: PWRBTN_EN SCI_EN Effect when PWRBTN_STS is set 0 x No SMI# or SCI. 1 0 SMI#. 1 1 SCI. NOTE: PWRBTN_EN has no effect on the PWRBTN_STS bit being set by the assertion of the power button. The Power Button is always enabled as a Wake event.
23:22	0h RO	**Reserved**
21	0h RW	**Global Enable (GBL_EN):** The global enable bit. When both the GBL_EN and the GBL_STS are set, PCH generates an SCI.
20:17	0h RO	**Reserved**
16	0h RW	**Timer Overflow Interrupt Enable (TMROF_EN):** This is the timer overflow interrupt enable bit. It works in conjunction with the SCI_EN bit: TMROF_EN SCI_EN Effect when TMROF_STS is set 0 x No SMI# or SCI. 1 0 SMI#. 1 1 SCI.
15	0h RW/1C/V	**Wake Status (WAK_STS):** This bit is set when the system is in one of the Sleep states (via the SLP_EN bit) and an enabled Intel PCH Wake event occurs. Upon setting this bit, the Intel PCH will transition the system to the ON state. This bit can only be set by hardware and can only be cleared by writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST#. If a power failure occurs (such as removed batteries) without the SLP_EN bit set, the WAK_STS bit will not be set when the power returns if the AFTER_G3 bit is 0. If the AFTER_G3 bit is 1, then the WAK_STS bit will be set after waking from a power failure. If necessary, the BIOS can clear the WAK_STS bit in this case.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C/V	**PCI Express Wake Status (PCIEXP_WAKE_STS):** This bit is set by hardware to indicate that the system woke due to a PCI Express wakeup event. This event can be caused by the PCI Express WAKE# pin being active, or one or more of the PCI Express ports being in beacon state, or receipt of a PCI Express PME message at root port. This bit should only be set when one of these events causes the system to transition from a non-S0 system power state to the S0 system power state. This bit is set independent of the PCIEXP_WAKE_DIS bit. Software writes a 1 to clear this bit. If WAKE# pin is still active during the write or one or more PCI Express ports is in the beacon state or PME message received indication is not cleared in the root port, then the bit will remain active (i.e. all inputs to this bit are level sensitive) Note: This bit does not itself cause a wake event or prevent entry to a sleeping state. Thus if the bit is 1 and the system is put into a sleeping state, the system will not automatically wake.
13:12	0h RO	**Reserved**
11	0h RW/1C/V	**Power Button Override (PWRBTNOR_STS):** This bit is set any time a Power Button Override Event occurs (i.e. the power button is pressed for at least 4 consecutive seconds), the corresponding bit is received in the SMBus slave message, the ME-Initiated Power Button Override bit is set, the ME-Initiated Host Reset with Power Down is set, or due to an internal thermal sensor catastrophic condition. These events cause an unconditional transition to the S5 state. The BIOS or SCI handler clears this bit by writing a 1 to it. This bit is not affected by hard resets via CF9h writes, and is not reset by pri_pwrgood_rst_b. Thus, this bit is preserved through power failures. Note that this bit is still asserted when the global SCI_EN is set to '1' then an SCI will be generated.
10	0h RW/1C/V	**RTC Status (RTC_STS):** This bit is set when the RTC generates an alarm (assertion of the IRQ8# signal), and is not affected by any other enable bit. See RTC_EN for the effect when RTC_STS goes active. This bit is only set by hardware and can only be reset by writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by dsw_pwrgood_rst_b.
9	0h RO	**Reserved**
8	0h RW/1C/V	**Power Button Status (PWRBTN_STS):** This bit is set when the PWRBTN# signal is asserted (low), independent of any other enable bit. See PWRBTN_EN for the effect when PWRBTN_STS goes active. PWRBTN_STS is always a wake event. This bit is only set by hardware and can be cleared by software writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by dsw_pwrgood_rst_b. If the PWRBTN# signal is held low for more than 4 seconds, the Intel PCH clears the PWRBTN_STS bit, sets the PWRBTNOR_STS bit, the system transitions to the S5 state, and only PWRBTN# is enabled as a wake event. If PWRBTN_STS bit is cleared by software while the PWRBTN# pin is still held low, this will not cause the PWRBTN_STS bit to be set. The PWRBTN# signal must go inactive and active again to set the PWRBTN_STS bit. Note that the SMBus Unconditional Powerdown message, the CPU Thermal Trip and the Internal Thermal Sensors' Catastrophic Condition result in behavior matching the Powerbutton Override, which includes clearing this bit.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C/V	**GBL Status (GBL_STS):** This bit is set when an SCI is generated due to the BIOS wanting the attention of the SCI handler. BIOS has a corresponding bit, BIOS_RLS, which will cause an SCI and set this bit. The SCI handler should then clear this bit by writing a 1 to it. This bit will not cause wake events or SMI#. This bit is not effected by SCI_EN. Note: GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place.
4	0h RW/1C/V	**Bus Master Status (BM_STS):** This bit is set to 1 by the Intel PCH when a PCH-visible bus master requests access to memory or the BM_BUSY# signal is active. This bit is cleared by the CPU writing a 1 to this bit position. This bit will not cause a wake event, SCI, or SMI. Implementation Details There are several conditions that can result in this bit being set based on various qualifications: o Qualified by BM_STS_ZERO_EN = 0 - any live snoopable backbone request - any pegged activeevent (see EN_PA_* registers) >> includes the BM_BUSY# pin o Qualified by PHOLD_BM_STS_BLOCK = 0 - PHOLD (LPC DMA or LPC bus master activity) o Qualified by individual BM_BREAK_EN bits being set to '1' - See BM_BREAK_EN register for list of devices
3:1	0h RO	**Reserved**
0	0h RW/1C/V	**Timer Overflow Status (TMROF_STS):** This is the timer overflow status bit. This bit gets set anytime bit 22 of the 24 bit timer goes low (bits are counted from 0 to 23). This will occur every 2.3435 seconds. See TMROF_EN for the effect when TMROF_STS goes active. Software clears this bit by writing a 1 to it.

4.3.2 Power Management 1 Control (PM1_CNT) — Offset 4h

Lockable: No Usage: ACPI or Legacy Power Well: Bits 0-9, 13-31: Primary, Bits 10-12: RTC Available: Desktop, Mobile

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h WO	**Sleep Enable (SLP_EN):** This is a write-only bit and reads to it always return a zero. Setting this bit causes the system to sequence into the Sleep state defined by the SLP_TYP field.

Bit Range	Default & Access	Field Name (ID): Description
12:10	0h RW	**Sleep Type (SLP_TYP):** This 3-bit field defines the type of Sleep the system should enter when the SLP_EN bit is set to 1. These bits are reset by rtc_pwrgood_rst_b only. Bits Mode Typical Mapping 000 ON S0 001 Puts CPU in S1 state. S1 010 Reserved 011 Reserved 100 Reserved 101 Suspend-To-RAM S3 110 Suspend-To-Disk S4 111 Soft Off S5
9:3	0h RO	**Reserved**
2	0h WO	**GBL_RLS:** This bit is used by the ACPI software to raise an event to the BIOS software. BIOS software has a corresponding enable and status bits to control its ability to receive ACPI events. This bit always reads as 0.
1	0h RW	**BM_RLD:** This bit is treated as a scratchpad bit.
0	0h RW	**SCI Enable (SCI_EN):** Selects the SCI interrupt or the SMI# for various events. When this bit is 1, then the events will generate an SCI interrupt. When this bit is 0, these events will generate an SMI#.

4.3.3 Power Management 1 Timer (PM1_TMR) — Offset 8h

Lockable: No Usage: ACPI Power Well: Primary Available: Desktop, Mobile

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO/V	**Timer Value (TMR_VAL):** This read-only field returns the running count of the PM timer. This counter runs off a 3.579545 MHz clock (derived from 14.31818 MHz divided by 4). It is reset (to 0) during a PCI reset, and then continues counting as long as the system is in the S0 state. After an S1 state, the counter will not be reset (it will continue counting from the last value in S0 state). Anytime bit 22 of the timer goes HIGH to LOW (bits referenced from 0 to 23), the TMROF_STS bit is set. The High-to-Low transition will occur every 2.3435 seconds. Writes to this register have no effect.

4.3.4 Therm Timer Delay Register (THERM_TIMER_DELAY) — Offset 20h

Thermal timer delay register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 20h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Thermal Timer Delay (THERM_TIMER_DELAY_VALUE):** Thermal Timer Delay

4.3.5 SMI Control and Enable (SMI_EN) — Offset 30h

I/O Address: PMBASE + 30h Attribute: Read/Write

Default Value: 00000000h Size: 32-bit

Lockable: No Usage: ACPI or Legacy

Power Well: Primary Available: Desktop, Mobile

Note: This register is symmetrical to the SMI Status Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 30h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**XHCI SMI Enable (XHCI_SMI_EN):** Software sets this bit to enable XHCI SMI events.
30	0h RW	**ME SMI Enable (ME_SMI_EN):** Software sets this bit to enable ME SMI# events.
29	0h RW	**LPSS SMI Enable (LPSS_SMI_EN):** Software sets this bit to enable LPSS SMII events

Bit Range	Default & Access	Field Name (ID): Description
28	0h RW/L	**eSPI SMI Enable (ESPI_SMI_EN):** Software sets this bit to enable eSPI SMI events. NOTE: When the ESPI_SMI_LOCK bit is set, this bit cannot be changed. **Locked by:** PCI_MMR.GEN_PMCON_A.ESPI_SMI_LOCK
27	0h RW/1S	**GPIO Unlock SMI Enable (GPIO_UNLOCK_SMI_EN):** Setting this bit will cause the Intel PCH to generate an SMI# when the GPIO_UNLOCK_SMI_STS bit is set in the SMI_STS register. Once written to '1', this bit can only be cleared by host_prim_rst_b.
26	0h RO	**Reserved**
25	0h RW	**SDX SMI Enable (SDX_SMI_EN):** Software sets this bit to enable SCC SMI events
24:19	0h RO	**Reserved**
18	0h RW	**THERM SMI Enable (THERM_SMI_EN):** Software sets this bit to enable Thermal SMI# events.
17	0h RW	**Legacy USB 2 Enable (LEGACY_USB2_EN):** Enables legacy USB2 logic to cause SMI#.
16:15	0h RO	**Reserved**
14	0h RW	**Periodic Enable (PERIODIC_EN):** Setting this bit will cause the Intel PCH to generate an SMI# when the PERIODIC_STS bit is set in the SMI_STS register..
13	0h RW/L	**TCO Enable (TCO_EN):** 1 = Enables the TCO logic to generate SMI#. 0 = Disables TCO logic generating an SMI#. If the NMI2SMI_EN bit is set, then SMI's that are caused by NMI's (i.e. rerouted) will not be gated by the TCO_EN bit. Even if the TCO_EN bit is 0, the NMI's will still be routed to cause the SMI#. NOTE: This bit can not be written once the TCO_LOCK bit (at offset 08h of TCO I/O Space) is set. This prevents unauthorized software from disabling the generation of TCO-based SMI's **Locked by:** `PMCIUNIT_WRAPPER.I_PMCIACPI.I_PMCIACPIR.MSUS_PMCI_TCO_LOCK_SYNCPMC
12	0h RO	**Reserved**
11	0h RW	**MCSMI Enable (MCSMI_EN):** Software sets this bit to 1 to enables Intel PCH to trap access to the microcontroller range (62h or 66h). A 'trapped' cycles will be claimed by Intel PCH, but not forwarded to LPC. An SMI# will also be generated.
10:8	0h RO	**Reserved**
7	0h WO	**BIOS_RLS:** Enables the generation of an SCI interrupt for ACPI software when a one is written to this bit position by BIOS software. This bit always reads a zero. NOTE: GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Software SMI Timer Enable (SWSMI_TMR_EN):** Software sets this bit to a 1 to start the Software SMI# Timer. When the timer expires (depending on the SWSMI_RATE_SEL bits), it will generate an SMI# and set the SWSMI_TMR_STS bit. The SWSMI_TMR_EN bit will remain at 1 until software sets it back to 0. Clearing the SWSMI_TMR_EN bit before the timer expires will reset the timer and the SMI# will not be generated. The default for this bit is 0.
5	0h RW	**APMC Enable (APMC_EN):** If set, this enables writes to the APM_CNT register to cause an SMI#
4	0h RW	**SMI On Sleep Enable (SMI_ON_SLP_EN):** If this bit is set, the Intel PCH will generate an SMI# when a write access attempts to set the SLP_EN bit (in the PM1_CNT register). Furthermore, the Intel PCH will not put the system to a sleep state. This allows the SMI# handler work around chip-level bugs. It is expected that the SMI# handler will turn off the SMI_ON_SLP_EN bit before actually setting the SLP_EN bit.
3	0h RW	**Legacy USB Enable (LEGACY_USB_EN):** Enables legacy USB circuit to cause SMI#.
2	0h RW	**BIOS Enable (BIOS_EN):** Enables the generation of SMI# when ACPI software writes a 1 to the GBL_RLS bit. Note that if the BIOS_STS bit, which gets set when software writes a 1 to GBL_RLS bit, is already a 1 at the time that BIOS_EN becomes 1, an SMI# will be generated when BIOS_EN gets set.
1	1h RW/1S/V	**End of SMI (EOS):** This bit controls the arbitration of the SMI signal to the processor. This bit must be set in order for Intel PCH to assert SMI# low to the processor after SMI# has been asserted previously. Once Intel ICH asserts SMI# low, the EOS bit is automatically cleared. In the SMI handler, the CPU should clear all pending SMIs (by servicing them and then clearing their respective status bits), set the EOS bit, and exit SMM. This will allow the SMI arbiter to reassert SMI upon detection of an SMI event and the setting of a SMI status bit. The SMI# signal will go inactive for 4 PCI clocks.
0	0h RW/L	**Global SMI Enable (GBL_SMI_EN):** When set, this bit enables the generation of SMIs in the system upon any enabled SMI event. This bit is reset by a PCI reset event. If this bit is not set, no SMI# will be generated. NOTE: When the SMI_LOCK bit is set, this bit cannot be changed. **Locked by:** PCI_MMR.GEN_PMCON_B.SMI_LOCK

4.3.6 SMI Status Register (SMI_STS) — Offset 34h

Lockable: No Usage: ACPI or Legacy Power Well: Primary Available: Desktop, Mobile

Note: If the corresponding _EN bit is set when the _STS bit is set, the Intel PCH will cause an SMI# (except bits 8-10, which don't cause SMI#)

Type	Size	Offset	Default
MMIO	32 bit	BAR + 34h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**XHCI SMI Status (XHCI_SMI_STS):** This bit will be set when any USB3 (XHCI) Host Controller is requesting an SMI.
30	0h RO/V	**ME SMI Status (ME_SMI_STS):** This bit will be set when ME is requesting an SMI#.
29	0h RW/1C/V	**LPSS SMI Status (LPSS_SMI_STS):** This bit gets set when LPSS agent is requesting SMI #. This bit is set by hardware and cleared by software writing a 1 to this bit position
28	0h RO/V	**eSPI SMI Status (ESPI_SMI_STS):** This bit is set if an eSPI agent is requesting an SMI#. This bit is set by hardware and cleared by software writing a 1 to its bit position.
27	0h RW/1C/V	**GPIO Unlock SMI Status (GPIO_UNLOCK_SMI_STS):** This bit will be set of the GPIO registers lockdown logic is requesting an SMI#. Writing a '1' to this bit position clears this bit to '0'.
26	0h RO/V	**SPI_SMI Status (SPI_SMI_STS):** This bit will be set when the SPI logic is requesting an SMI#. This bit is read only because the sticky status and enable bits associated with this function are located in the SPI registers.
25	0h RW/1C/V	**SCC SMI Status (SDX_SMI_STS):** This bit gets set when SCC agent is requesting SMI#.This bit is set by hardware and cleared by software writing a 1 to this bit position
24	0h RO/V	**Reserved**
23	0h RO	**Reserved**
22	0h RO/V	**INTERNAL_TT Status (INTERNAL_TT_STS):** This bit will be set if the internal thermal throttle mechanism has changed state. This bit is read only because the sticky status and enable bit associated with this function is in the other unit.
21	0h RO/V	**Monitor Status (MONITOR_STS):** This bit will be set if the Trap/SMI logic has caused the SMI. This will occur when the CPU or a bus master accesses an assigned register (or a sequence of accesses).
20	0h RO/V	**PCI_EXP_SMI Status (PCI_EXP_SMI_STS):** 1- PCI Express SMI event occurred. This could be due to a PCI Express PME event or Hot Plug Event.
19	0h RO/V	**RTC Update-In-Progress SMI Status (RTC_UIP_SMI_STS):** This bit will be set when the RTC Update-In-Progress signal transitions either from low-to-high or high-to-low, depending on the enables in the I/O Trap register space. This bit is Read Only. The sticky Read/Write Clear status bits are implemented in the I/O Trap register space. There is no need for a corresponding enable because individual enables are provided in the the I/O Trap register space.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/1C/V	**Thermal SMI Status (THERM_SMI_STS):** This bit will be set when the FW sets DRV_THERM_SMI_SCI_STS.DRV_SMI_STS bit. It is cleared by the Host Software
17	0h RO/V	**Legacy USB 2 Status (LEGACY_USB2_STS):** This non-sticky read-only bit is a logical OR of each of the SMI status bits in the USB2 Legacy Support Register ANDed with the corresponding enable bits. This bit will not be active if the enable bits are not set. Writes to this bit will have no effect. All integrated USB2 Host Controllers are represented with this bit.
16	0h RW/1C/V	**SMBUS_SMI Status (SMBUS_SMI_STS):** Intel PCH sets this bit to 1 to indicate that the SMI# was caused by: 1. The SMBus Slave receiving a message that an SMI# should be caused, or 2. The SMBALERT# signal goes active and the SMB_SMI_EN bit is set and the SMBALERT_DIS bit is cleared. 3. The SMBus Slave receiving a HOST_NOTIFY message and the HOST_NOTIFY_INTREN and the SMB_SMI_EN bits are set. 4. The SMBus Slave receiving a SMI in S0message. This bit is sticky. It is cleared by writing a 1 to this bit position. Note that this bit is set from the 64 KHz clock domain used by the SMBus. Software must wait at least 15.63 microseconds
15	0h RO/V	**SERIRQ_SMI Status (SERIRQ_SMI_STS):** 1 = Indicates the SMI# was caused by the SERIRQ decoder. 0 = SMI# not caused by SERIRQ decoder. Note, this bit is not sticky. Writes to this bit will have no effect.
14	0h RW/1C/V	**Periodic Status (PERIODIC_STS):** This bit will be set at the rate determined by the PER_SMI_SEL bits. If the PERIODIC_EN bit is also set, the Intel PCH will generate an SMI#. This bit is cleared by writing a 1 to this bit position.
13	0h RW/1C/V	**TCO Status (TCO_STS):** 1 = Indicates SMI was caused by the TCO logic. 0 = SMI not caused by TCO logic. NOTE: Will not cause wake event. This bit is cleared by writing a 1 to this bit position.
12	0h RO/V	**DEVMON Status (DEVMON_STS):** This read-only bit is set when bit 0 in the DEVTRAP_STS register is set. It is not sticky, so writes to this bit will have no effect.
11	0h RW/1C/V	**MCSMI Status (MCSMI_STS):** This bit is set if there is an access to the power management microcontroller range (62h or 66h). If this bit is set, and the MCSMI_EN bit is also set, the Intel PCH will generate an SMI#. This bit is set by hardware and cleared by software writing a 1 to its bit position.
10	0h RO/V	**GPIO SMI Status (GPIO_SMI_STS):** This bit will be a 1 if any GPIO that is enabled to trigger SMI is asserted. GPIOs that are not routed to cause an SMI will have no effect on this bit. This bit is NOT sticky. Writes to this bit will have no effect.
9	0h RO/V	**GPE0 Status (GPE0_STS):** There are several status/enable bit pairs in GPE0_STS/EN_127_96 that are capable of triggering SMIs. This bit is a logical OR of all of those pairs (i.e. this bit is asserted whenever at least one of those pairs has both the status and enable bit asserted). This bit is NOT sticky. Writes to this bit will have no effect. Note: The setting of this bit does not cause the SMI#. The following bit pairs are included in this logical OR: - GPE0_STS/EN_127_96 [18, 17, 16, 13, 11, 10, 8, 2]
8	0h RO/V	**PM1 Status Register (PM1_STS_REG):** This is an OR of the bits (except for bits 5 and 4) in the ACPI PM1 Status Reg. (offset PMBASE+00h). Not sticky. Writes to this bit have no effect. Note: The setting of this bit does not cause the SMI#.
7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/1C/V	**Software SMI Timer Status (SWSMI_TMR_STS):** This bit will be set to 1 by the hardware when the Software SMI# Timer expires. This bit will remain 1 until the software writes a 1 to this bit.
5	0h RW/1C/V	**APM Status (APM_STS):** SMI# was generated by a write access to the APM control register and if the APMC_EN bit is set. This bit is cleared by writing a one to its bit position.
4	0h RW/1C/V	**SMI_ON_SLP_EN Status (SMI_ON_SLP_EN_STS):** This bit will be set by the Intel PCH when a write access attempts to set the SLP_EN bit. This bit is cleared by writing a 1 to this bit position
3	0h RO/V	**Legacy USB Status (LEGACY_USB_STS):** This non-sticky read-only bit is a logical OR of each of the SMI status bits in the USB Legacy Keybd Register ANDed with the corresponding enable bits. This bit will not be active if the enable bits are not set. Writes to this bit will have no effect.
2	0h RW/1C/V	**BIOS Status (BIOS_STS):** This bit gets set by hardware when a 1 is written by software to the GBL_RLS bit. When both BIOS_EN and the BIOS_STS bit are set, an SMI# will be generated. The BIOS_STS bit is cleared when software writes a 1 to this bit position.
1:0	0h RO	**Reserved**

4.3.7 General Purpose Event Control (GPE_CTRL) — Offset 40h

Lockable: No Usage: ACPI or Legacy Power Well: Primary Available: Desktop, Mobile

Type	Size	Offset	Default
MMIO	32 bit	BAR + 40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RW/V	**Software GPE Control (SWGPE_CTRL):** This bit allows software to control the assertion of SWGPE_STS bit. This bit is used by hardware as the level input signal for the SWGPE_STS bit in the GPE0_STS register. When SWGPE_CTRL is 1, SWGPE_STS will be set to 1, and writes to SWGPE_STS with a value of 1 to clear SWGPE_STS will result in SWGPE_STS being set back to 1 by hardware. When SWGPE_CTRL is 0, writes to SWGPE_STS with a value of 1 will clear SWGPE_STS to 0.
16:0	0h RO	**Reserved**

4.3.8 Device Trap Status Register (DEVTRAP_STS) — Offset 44h

Lockable: No Usage: Legacy Only Power Well: Primary Available: Desktop, Mobile

Each bit indicates if an access has occurred to the corresponding device's trap range, or for bits 6:9 if the corresponding PCI interrupt is active. Write 1 to the same bit position to clear it. This register is used by APM power management software to see if there has been system activity. The periodic SMI# timer indicates if it is the right time to read the DEVTRAP_STS register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 44h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RW/1C/V	**D12 Trap Status (D12_TRP_STS):** KBC (60/64h)
11:10	0h RO	**Reserved**
9	0h RW/1C/V	**D9 Trap Status (D9_TRP_STS):** PIRQ[D or H]
8	0h RW/1C/V	**D8 Trap Status (D8_TRP_STS):** PIRQ[C or G]
7	0h RW/1C/V	**D7 Trap Status (D7_TRP_STS):** PIRQ
6	0h RW/1C/V	**D6 Trap Status (D6_TRP_STS):** PIRQ[A or E] This bit will be set if PCI IRQ A or PCI IRQ E goes active (by the pin or internal signal).
5	0h RW/1C/V	**D5 Trap Status (D5_TRP_STS):** This will be set if any of the following are accessed (as determined by the I/O ranges in the LPC decoder (even if the LPC forwarding is not enabled): SP1, SP2, PP, FDC.
4:1	0h RO	**Reserved**
0	0h RW/1C/V	**D0 Trap Status (D0_TRP_STS):** The access/SMI was due to the SATA logic. There is no corresponding bit in the DEVTRAP_EN register because the enables are in the new SATA registers.

4.3.9 PM2a Control Block (PM2A_CNT_BLK) — Offset 50h

Lockable: No Usage: ACPI or Legacy Power Well: Primary Available: Desktop, Mobile

Note: BIOS must describe this register as 1 byte wide to the OS

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**ARB_DIS:** This bit is essentially just a scratchpad bit for legacy software compatibility.

4.3.10 Over-Clocking WDT Control (OC_WDT_CTL) — Offset 54h

This register controls the operation of the PCHs Over-Clocking Watchdog Timer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 54h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h WO	**Over-Clocking WDT Reload (OC_WDT_RLD):** Software can write a '1' to this bit to reload (ping) the PCH over-clocking watchdog timer while it is running. A write of '0' to this bit has no effect. A write of '1' to this bit while OC_WDT_EN=0, or with the clearing of OC_WDT_EN, does not start or reload the WDT (i.e. OC_WDT_EN takes precedence). The value in OC_WDT_TOV may be changed by software along with its setting of this bit. On a WDT reload, the current (potentially new) value in OC_WDT_TOV is loaded into the WDT as the new timeout value.
30:26	0h RO	**Reserved**
25	0h RW/1C/V	**Over-Clocking WDT ICC Survivability Mode Timeout Status (OC_WDT_ICCSURV_STS):** This bit is set to '1' if the over-clocking WDT has timed out and triggered a global reset while running in a mode that has ICC survivability impact (OC_WDT_ICCSURV=1). It is cleared by a software write of '1' or by the RSMRST# pin.
24	0h RW/1C/V	**Over-Clocking WDT Non-ICC Survivability Mode Timeout Status (OC_WDT_NO_ICCSURV_STS):** This bit is set to '1' if the over-clocking WDT has timed out and triggered a global reset while running in a mode that does not have ICC survivability impact (OC_WDT_ICCSURV=0). It is cleared by a software write of '1' or by the RSMRST# pin.

Bit Range	Default & Access	Field Name (ID): Description
23:16	00h RW	**Over-Clocking WDT Scratchpad (OC_WDT_SCRATCH):** This field is available as scratchpad space for software and has no effect on PCH HW operation.
15	0h RW/L	**Over-Clocking WDT Force All (OC_WDT_FORCE_ALL):** GATE_BIT:OC_WDT_CTL.OC_WDT_CTL_LCK.HIGH When this bit is set to 1 and the OC_WDT is running, any included global reset source will behave as though the OC_WDT expired. **Locked by:** OC_WDT_CTL.OC_WDT_CTL_LCK
14	0h RW/V/L	**Over-Clocking WDT Enable (OC_WDT_EN):** Software sets this bit to '1' to enable the PCH over-clocking watchdog timer. While the counter is running, if it expires before being reloaded by software via the OC_WDT_RLD bit or halted by software clearing this bit, then one of the status bits will be set (which one depends on the WDT operating mode at the time - see the OC_WDT_ICCSURV bit description), and a global reset will be triggered. This bit is also set by the hardware when conditions allow the OC_WDT to self-start at power cycle reboot (effectively changes the default of this bit as seen by software). **Locked by:** OC_WDT_CTL.OC_WDT_CTL_LCK
13	1h RW/L	**Over-Clocking WDT ICC Survivability Impact (OC_WDT_ICCSURV):** This bit determines whether OC_WDT expiration will have an impact on ICC (Integrated Clock Controller) bootstrap survivability. OC_WDT_ICCSURV=1 (default) An OC_WDT timeout while operating in this mode causes certain ICC hardware auto-recovery actions to take place. A timeout in this mode will set OC_WDT_ICCSURV_STS. OC_WDT_ICCSURV=0 Software should configure the OC_WDT to this mode if no ICC hardware auto-recovery actions are desired in the event of a timeout. A timeout in this mode will set OC_WDT_NO_ICCSURV_STS. **Locked by:** OC_WDT_CTL.OC_WDT_CTL_LCK
12	0h RW/L	**OC_WDT_CTL Register Lock (OC_WDT_CTL_LCK):** This bit controls write-ability to this register. Encodings: 0: All fields of register OC_WDT_CTL operate as normal and can be updated by software. Reads to the register operate as normal. 1: All RW/L fields of register OC_WDT_CTL, including this lock control bit, are locked. Writes to these register fields have no effect and the register fields retain their current states. Reads to the register operate as normal. Once this bit is set, it can only be cleared by CORE well power loss. **Locked by:** OC_WDT_CTL.OC_WDT_CTL_LCK
11:10	0h RO	**Reserved**
9:0	000h RW/V/L	**Over-Clocking WDT Timeout Value (OC_WDT_TOV):** Software programs the desired over-clocking WDT timeout value into this register. This timer is zero-based and has a granularity of 1 second. Example timeout values: 000h: 1 second 001h: 2 seconds ... 3FFh: ~17 minutes (1024 seconds) The value of OC_WDT_TOV may be changed by software along with its setting of the OC_WDT_RLD bit. On a WDT reload, the current (potentially new) value in OC_WDT_TOV is loaded into the WDT as the new timeout value. This field is also updated by the hardware when conditions allow the OC_WDT to self-start at power cycle reboot (effectively changes the default of this field as seen by software). **Locked by:** OC_WDT_CTL.OC_WDT_CTL_LCK

4.3.11 General Purpose Event 0 Status [31:0] (GPE0_STS_31_0) — Offset 60h

GPE0_STS bits 31:0 are claimed by the PMC on IOSF primary and forwarded to the GPIO unit via IOSF sideband.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C/V	**General Purpose Event 0 Status [31:0] (GPE0_STS_31_0)**

4.3.12 General Purpose Event 0 Status [63:32] (GPE0_STS_63_32) — Offset 64h

GPE0_STS bits 63:32 are claimed by the PMC on IOSF primary and forwarded to the GPIO unit via IOSF sideband.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 64h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C/V	**General Purpose Event 0 Status [63:32] (GPE0_STS_63_32)**

4.3.13 General Purpose Event 0 Status [95:64] (GPE0_STS_95_64) — Offset 68h

GPE0_STS bits 95:64 are claimed by the PMC on IOSF primary and forwarded to the GPIO unit via IOSF sideband.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 68h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C/V	**General Purpose Event 0 Status [95:64] (GPE0_STS_95_64)**

4.3.14 General Purpose Event 0 Status [127:96] (GPE0_STS_127_96) — Offset 6Ch

Note: This register is symmetrical to the General Purpose Event 0 Enable [127:96] Register. Unless indicated otherwise below, if the corresponding _EN bit is set, then when the STS bit get set, the Intel PCH will generate a Wake Event. Once back in an S0 state (or if already in an S0 state when the event occurs), the Intel PCH will also generate an SCI if the SCIEN bit is set, or an SMI# if the SCIEN bit is not set and GBL_SMI_EN is set.

Note that GPE0_STS bits 95:0 are claimed by the GPIO register block.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RO	**Reserved**
18	0h RW/1C/V	**Wake Alarm Device Timer Status (WADT_STS):** This bit is set whenever the any of the wake alarm device timers signal a timer expiration.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW/1C/V	**USB Connection in/after DeepSx Status (USB_CON_DSX_STS):** This bit is set when a connection event occurs on any unmasked USB port while in DeepSx or while in Sx immediately after DeepSx. Note: This bit will be set regardless of the value of the DSX_CFG.USB_CON_DSX_MODE bit. Note: Because this status bit is only set during DeepSx exit or while in Sx after DeepSx, SMI/SCI generation will only occur immediately as the platform enters S0. The event cannot occur and the bit cannot be set after the platform reaches S0. Hence, the event cannot generate an SMI/SCI after the platform reach S0.
16	0h RW/1C/V	**GPIO[27] Status (LANWAKE_STS):** This bit is set whenever GPIO[27] is seen asserted low. Note that unlike the GPI[n]_STS bits, GPIO[27] is always monitored as an input for the purpose of setting this bit, regardless of the actual GPIO configuration.
15	0h RW/1C/V	**GPIO Tier2 SCI Status (GPIO_TIER2_SCI_STS):** This bit is a logical OR of sci_wake from tier 2 GPIO's. reset_type=host_deep_rst_b
14	0h RW/1C/V	**eSPI SCI Status (ESPI_SCI_STS):** This bit will be set when an agent attached to eSPI is requesting an SCI. Note: This source is not able to cause a wake event.
13	0h RW/1C/V	**Power Management Event Bus 0 Status (PME_B0_STS):** This bit will be set to 1 by the Intel PCH when any internal device with PCI Power Management capabilities on bus 0 asserts the equivalent of the PME# signal. Additionally, if the PME_B0_EN and SCI_EN bits are set, and the system is in an S0 state, then the setting of the PME_B0_STS bit will generate an SCI (or SMI# if SCI_EN is not set). If the PME_B0_EN bit is set, and the system is in an S1-S4 state (or S5 state due to SLP_TYP and SLP_EN), then the setting of the PME_B0_STS bit will generate a wake event. If the system is in an S5 state due to power button override, then the PME_B0_STS bit will not cause a wake event or SCI. This bit is cleared by a software write of '1'. Internal devices which can set this bit: - Integrated LAN - HD Audio/Audio DSP - SATA - EHCI ('USB2') - XHCI ('USB3') - ME Maskable Host Wake
12	0h RW/1C/V	**ME SCI Status (ME_SCI_STS):** This bit will be set when ME is requesting an SCI. Software must clear the ME source of the SCI before clearing this bit. Note: This source is not able to cause a wake event.
11	0h RW/1C/V	**Power Management Event Status (PME_STS):** This bit will be set to 1 by hardware when the PME# signal goes active. Additionally, if the PME_EN and SCI_EN bits are set, and system is in an S0 state, then the setting of the PME_STS bit will generate an SCI (or SMI# if SCI_EN is not set). If the PME_EN bit is set, and the system is in an S1-S4 state (or S5 state due to SLP_TYP and SLP_EN), then the setting of the PME_STS bit will generate a wake event. If the system is in an S5 state due to power button override, then PME_STS will not cause a wake event or SCI. This bit is cleared by writing a 1 to this bit position.
10	0h RW/1C/V	**Battery Low Status (BATLOW_STS):** In Mobile Mode this bit will be set to 1 by hardware when the BATLOW# signal goes low. Software clears the bit by writing a 1 to the bit position. In Desktop Mode, this bit will be treated as Reserved.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/1C/V	**PCI Express Status (PCI_EXP_STS):** This bit will be set to 1 by hardware to indicate that: The PME event message was received on one or more of the PCI-Express Ports An Assert PMEGPE message received from the MCH via DMI Note: The PCI WAKE# pin and the PCI-Express Beacons have no impact on this bit. Software attempts to clear this bit by writing a 1 to this bit position. If the PCI_EXP_STS bit went active due to an Assert PMEGPE message, then a Deassert PMEGPE message must be received prior to the software write in order for the bit to be cleared. If the bit is not cleared and the corresponding PCI_EXP_EN bit is set, the leveltriggered SCI will remain active. Note that a race condition exists where the PCI Express device sends another PME message because the PCI Express device was not serviced within the time when it must resend the message. This may result in a spurious interrupt, and this is comprehended and approved by the PCI Express specification. The window for this race condition is approximately 95-105 milliseconds.
8	0h RW/1C/V	**OSE Status (OSE_STS):** This bit will be set to1 by hardware when the OSE# input signal goes active. This bit can be reset by writing a 1 to this bit position.
7	0h RW/1C/V	**SMBus Wake Status (SMB_WAK_STS):** This bit is set to 1 by the hardware to indicate that the wake event was caused by the PCH's SMBus logic. This could be due to either the SM Bus slave unit receiving a message or the SMBALERT# signal going active. NOTES: 1. The SMBus controller will independently cause an SMI# so this bit does not need to do so (unlike the other bits in this register). 2. This bit is set by the SMBus slave command 01h (Wake/SMI#) even when the system is in the S0 state. Therefore, to avoid an instant wake on subsequent transitions to sleep states, software must clear this bit after each reception of the Wake/SMI# command or just prior to entering the sleep state. 3. The SMBALERT_STS bit (SMBus I/O Offset 00h:bit 5) should be cleared by software before clearing this bit.
6	0h RW/1C/V	**TCOSCI Status (TCOSCI_STS):** This bit will be set to 1 by hardware when the TCO logic or Thermal Sensor logic causes an SCI. This bit can be reset by writing a one to this bit position.
5	0h RO	**Reserved**
4	0h RW/1C/V	**Thermal SCI Status (THERM_SCI_STS):** This bit will be set to 1 by hardware when the firmware sets the DRV_THERM_SMI_SCI_STS.DRV_SCI_STS. This bit can be cleared by writing a one to this bit position.
3	0h RW/1C/V	**eSPI Unconditional Wake Status (ESPIUWAK_STS):** This bit is set to 1 by hardware upon reception of an unconditional wake message from eSPI
2	0h RW/1C/V	**Software GPE Status (SWGPE_STS):** The SWGPE_CTRL bit (bit 1 of GPE_CTRL reg) acts as a level input to this bit.
1	0h RW/1C/V	**Hot Plug Status (HOT_PLUG_STS):** This bit is set to 1 by hardware when a PCI-Express hotplug event occurs. This will cause an SCI if the HOT_PLUG_EN and SCI_EN bits are set. This bit is cleared by writing a 1 to this bit position. The following events cause this bit to set Assert_GPE message received from any of the PCI_E ports in PCH Assert_HPGPE message received from any of the PCI_E ports in PCH Assert_GPE message received downstream from MCH Assert_HPGPE message received downstream from MCH
0	0h RW/1C/V	**FIA dFlex SCI Status (FIA_DFLEX_STS):** This bit will be set when requests an SCI as part of the dFlex flow.

4.3.15 General Purpose Event 0 Enable [31:0] (GPE0_EN_31_0) — Offset 70h

GPE0_EN bits 31:0 are claimed by the PMC on IOSF primary and forwarded to the GPIO unit via IOSF sideband.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 70h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Event 0 Enable [31:0] (GPE0_EN_31_0)**

4.3.16 General Purpose Event 0 Enable [63:32] (GPE0_EN_63_32) — Offset 74h

GPE0_EN bits 63:32 are claimed by the PMC on IOSF primary and forwarded to the GPIO unit via IOSF sideband.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 74h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Event 0 Enable [63:32] (GPE0_EN_63_32)**

4.3.17 General Purpose Event 0 Enable [95:64] (GPE0_EN_95_64) — Offset 78h

GPE0_EN bits 95:64 are claimed by the PMC on IOSF primary and forwarded to the GPIO unit via IOSF sideband.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 78h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Event 0 Enable [95:64] (GPE0_EN_95_64)**

4.3.18 General Purpose Event 0 Enable [127:96] (GPE0_EN_127_96) — Offset 7Ch

Note: This register is symmetrical to the General Purpose Event 0 Status [127:96] Register.

Note that GPE0_STS bits 95:0 are claimed by the GPIO register block.reset_type=host_deep_rst_b

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RO	**Reserved**
18	0h RW	**Wake Alarm Device Timer Enable (WADT_EN):** Used to enable the setting of the WADT_STS bit to generate wake/SMI#/SCI.
17	0h RW	**USB Connection in/after DeepSx Enable (USB_CON_DSX_EN):** Used to enable the setting of the USB_CON_DSX_STS bit to generate wake/SMI#/SCI.
16	0h RW	**GPIO[27] Enable (LANWAKE_EN):** Used to enable the setting of the LANWAKE_STS bit to generate wake/SMI#/SCI. Host wake events from the PHY through LANWAKE cannot be disabled by clearing this bit. Note that GPIO[27] is a valid host wake event from Deep-Sx. But the wake enable configuration must persist even after a G3. So this bit is in the RTC well.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/V	**GPIO Tier2 SCI EN (GPIO_TIER2_SCI_EN):** Used to enable the setting of GPIO_TIER2_SCI_STS to generate wake/SCI# reset_type=host_deep_rst_b
14	0h RW/V	**eSPI SCI Enable (ESPI_SCI_EN):** Used to enable the setting of the ESPI_SCI_STS bit to generate a SCI.
13	0h RW/V	**PME_B0 Enable (PME_B0_EN):** Enables the setting of the PME_B0_STS bit to generate a wake event and/or an SCI or SMI#.
12	0h RW/V	**ME SCI Enable (ME_SCI_EN):** Used to enable the setting of the ME_SCI_STS bit to generate a SCI.
11	0h RW/V	**Power Management Event Enable (PME_EN):** Enables the setting of the PME_STS to generate a wake event and/or an SCI.
10	0h RW/V	**Low Battery Enable (BATLOW_EN):** In Mobile Mode, this bit enables the BATLOW# signal to cause an SMI# or SCI (depending on the SCI_EN bit) when it goes low.This bit does not prevent the BATLOW# signal from inhibiting the wake event. In Desktop Mode this bit will be treated as Reserved.
9	0h RW/V	**PCI Express Enable (PCI_EXP_EN):** Enables PCH to cause an SCI when PCI_EXP_STS bit is set. This is used to allow the PCI Express ports, including the link to the MCH, to cause an SCI due to wake/PME events.
8	0h RW/V	**OSE Enable (OSE_EN):** When OSE_EN and OSE_STS are both set, a Wake event will occur. If OSE_EN is not set, then when OSE_STS is set, no Wake event will occur.
7	0h RO	**Reserved**
6	0h RW/V	**TCOSCI Enable (TCOSCI_EN):** When TCOSCI_EN and TCOSCI_STS are both set, an SCI will be generated.
5	0h RO	**Reserved**
4	0h RW	**Thermal SCI Enable (THERM_EN):** When THERM_EN and THERM_SCI_STS are both set, an SCI will be generated.
3	0h RO	**Reserved**
2	0h RW/V	**Software GPE Enable (SWGPE_EN):** This bit, when set to 1, enables the SW GPE function. If SWGPE_CTRL is written to a 1, hardware will set SWGPE_STS (acts as a level input) If SWGPE_STS, SWGPE_EN, and SCI_EN are all 1's, an SCI will be generated If SWGPE_STS = 1, SWGPE_EN = 1, SCI_EN = 0, and GBL_SMI_EN = 1 then an SMI# will be generated
1	0h RW/V	**Hot Plug Enable (HOT_PLUG_EN):** Enables PCH to cause an SCI when the HOT_PLUG_STS bit is set. This is used to allow the PCI Express ports to cause an SCI due to hot-plug events. (The following events cause HOT_PLUG_STS bit to set Assert_GPE message received from any of the PCI_E ports in PCH Assert_HPGPE message received from any of the PCI_E ports in PCH Assert_GPE message received downstream from MCH Assert_HPGPE message received downstream from MCH)
0	0h RW	**FIA dFlex SCI Enable (FIA_DFLEX_EN):** Used to enable the setting of the FIA_DFLEX_STS bit to generate an SCI.

5 Converged Audio, Voice, Speech (cAVS) Controller

5.1 cAVS Configuration Registers Summary

This chapter documents the registers in Bus: 0, Device 31, Function 3.

DID Values:

cAVS Controller - D27: F0 - 4B5xh

4B55h, 4B56h, 4B57h, 4B58h, 4B59h, 4B5Ah, 4B5Bh, 4B5Ch.

Table 5-1. Summary of Bus: 0, Device: 31, Function: 3 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	Vendor Identification (VID)	8086h
2h	2	Device ID (DID)	4B5xh
4h	2	CMD	0000h
6h	2	STS	0010h
8h	1	Revision Identification (RID)	00h
9h	1	Programming Interface (PI)	00h
Ah	1	Sub Class Code (SCC)	03h
Bh	1	Base Class Code (BCC)	04h
Ch	1	Cache Line Size (CLS)	00h
Dh	1	Latency Timer (LT)	00h
Eh	1	Header Type (HTYPE)	00h
Fh	1	Built-in Self Test (BIST)	00h
10h	4	Intel HD Audio Base Lower Address (HDALBA)	00000004h
14h	4	Intel HD Audio Base Upper Address (HDAUBA)	00000000h
18h	4	Shadowed PCI Configuration Lower Base Address (SPCLBA)	00000000h
1Ch	4	Shadowed PCI Configuration Upper Base Address (SPCUBA)	00000000h
20h	4	Audio DSP Lower Base Address (ADSPLBA)	00000004h
24h	4	Audio DSP Upper Base Address (ADSPUBA)	00000000h
2Ch	2	Subsystem Vendor ID (SVID)	0000h
2Eh	2	Subsystem ID (SID)	0000h
34h	1	Capability Pointer (CAPPTR)	50h
3Ch	1	Interrupt Line (INTLN)	00h
3Dh	1	Interrupt Pin (INTPN)	01h
50h	2	PCI Power Management Capability ID (PID)	6001h
52h	2	Power Management Capabilities (PC)	C043h
54h	4	Power Management Control And Status (PCS)	00000008h

Table 5-1. Summary of Bus: 0, Device: 31, Function: 3 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
60h	2	MSI Capability ID (MID)	7005h
62h	2	MSI Message Control (MMC)	0080h
64h	4	MSI Message Lower Address (MMLA)	00000000h
68h	4	MSI Message Upper Address (MMUA)	00000000h
6Ch	2	MSI Message Data (MMD)	0000h
70h	2	PCI Express Capability ID (PXID)	0010h
72h	2	PCI Express Capabilities (PXC)	0091h
74h	4	Device Capabilities (DEVCAP)	10000000h
78h	2	Device Control (DEVC)	2800h
7Ah	2	Device Status (DEVS)	0010h
80h	4	Vendor Specific Capability Identifiers (VSCID)	F0146009h
84h	4	Vendor Specific Extended Capability (VSECID)	01400010h
8Ch	4	Device Idle Pointer (DEVIDLEPTR)	000104A1h
90h	2	Device Idle Power On Latency (DEVIDLEPOL)	0800h
F8h	4	Manufacturing Process (MANID)	00000000h
100h	4	Virtual Channel Enhanced Capability Header (VCCAP)	00000000h
104h	4	Port VC Capability Register 1 (PVCCAP1)	00000001h
108h	4	Port VC Capability Register 2 (PVCCAP2)	00000000h
10Ch	2	Port VC Control Register (PVCCTL)	0000h
10Eh	2	Port VC Status Register (PVCSTS)	0000h
110h	4	VC0 Resource Capability Register (VC0CAP)	00000000h
114h	4	VC0 Resource Control Register (VC0CTL)	800000FFh
11Ah	2	VC0 Resource Status Register (VC0STS)	0000h
11Ch	4	VCi Resource Capability Register (VCICAP)	00000000h
120h	4	VCi Resource Control Register (VCICTL)	00000000h
126h	2	VCi Resource Status Register (VCISTS)	0000h
130h	4	Root Complex Link Declaration Enhanced (RCCAP)	00010005h
134h	4	Element Self Description (ESD)	0F000100h
140h	4	Link 1 Description (L1DESC)	00000001h
148h	4	Link 1 Lower Address (L1LADD)	00000000h
14Ch	4	Link 1 Upper Address (L1UADD)	00000000h

5.1.1 Vendor Identification (VID) - Offset 0h

This register identifies the manufacturer of the device. Valid vendor identifiers are allocated by the PCI SIG to ensure uniqueness. FFFFh is an invalid value for Vendor ID.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:3] + 0h	8086h

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**Vendor ID (VID):** Indicates that Intel is the vendor.

5.1.2 Device ID (DID) - Offset 2h

This register is not affected by D3HOT to D0 reset or FLR.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:3] + 2h	8C20h

Bit Range	Default & Access	Field Name (ID): Description
15:0	4B5xh RO/V	**Device ID (DID):** Indicates the device number assigned by the SIG. Bits(2:0) of the DID is controlled by fuse. IOSF Sideband Set ID Value message initializes bits 15:7 of this register value, while bits 6:0 of this register value are hard-coded. See the Global Device ID table in Intel Atom® x6000E Series, and Intel® Pentium® and Celeron® N and J Series Processors for Internet of Things (IoT) Applications Volume 1.

5.1.3 CMD - Offset 4h

This Register Provides Coarse Control Over A Device's Ability To Generate And Respond To PCI Cycles.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:3] + 4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable (ID):** Enables the device to assert an INTx#. When set, the Intel® HD Audio controller's INTx# signal will be de-asserted. When cleared, the INTx# signal may be asserted. Note that this bit does not affect the generation of MSI's.
9	0h RO	**Fast Back to Back Enable (FBE):** Not implemented. Hardwired to 0.
8	0h RW	**SERR Enable (SEN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
7	0h RO	**Wait Cycle Control (WCC):** Not implemented. Hardwired to 0.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Parity Error Response (PER):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
5	0h RO	**VGA Palette Snoop (VPS):** Not implemented. Hardwired to 0.
4	0h RO	**Memory Write and Invalidate Enable (MWI):** Not implemented. Hardwired to 0.
3	0h RO	**Special Cycle Enable (SCE):** Not implemented. Hardwired to 0.
2	0h RW	**Bus Master Enable (BME):** 1 = Enable, 0 = Disable. Controls standard PCI Express bus mastering capabilities for Memory and IO, reads and writes. Note that this also controls MSI generation since MSI is essentially Memory writes.
1	0h RW	**Memory Space Enable (MSE):** When set, enables memory space accesses to the Intel HD Audio controller.
0	0h RO	**I/O Space (IOS):** The Intel HD Audio controller does not implement IO Space, therefore this bit is hardwired to 0.

5.1.4 STS - Offset 6h

This register is used to record status information for PCI bus related events.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:3] + 6h	0010h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Detected Parity Error (DPE):** Not implemented. Hardwired to 0.
14	0h RO	**SERR# Status (SERRS):** Not implemented. Hardwired to 0.
13	0h RW/1C/V	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, this bit is set. SW writes a 1 to this bit to clear it.
12	0h RW/1C/V	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, this bit is set. SW writes a 1 to this bit to clear it.
11	0h RO	**Signaled Target-Abort (STA):** Not implemented. Hardwired to 0.
10:9	0h RO	**DEVSEL# Timing Status (DEVT):** Does not apply. Hardwired to 0.
8	0h RO	**Master Data Parity Error (MDPE):** Not implemented. Hardwired to 0.
7	0h RO	**Fast Back to Back Capable (FBC):** Does not apply. Hardwired to 0.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**Reserved**
5	0h RO	**66 MHz Capable (C66):** Does not apply. Hardwired to 0.
4	1h RO	**Capabilities List Exists (CLIST):** Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.
3	0h RO/V	**Interrupt Status (IS):** Reflects the state of the INTx# signal at the input of the enable/disable circuit. This bit is a 1 when the INTx# is asserted. This bit is a 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the command register). Note that this bit is not set by an MSI.
2:0	0h RO	**Reserved**

5.1.5 Revision Identification (RID) - Offset 8h

This register is not affected by D3HOT to D0 reset or FLR

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:31, F:3] + 8h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO/V	**Revision ID (RID):** Indicates the device specific revision identifier. IOSF Sideband Set ID Value message initializes this register value

5.1.6 Programming Interface (PI) - Offset 9h

This register is not affected by D3HOT to D0 reset or FLR

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:31, F:3] + 9h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/L	**Programming Interface (PI):** Value assigned to the Intel HD Audio subsystem. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD

5.1.7 Sub Class Code (SCC) - Offset Ah

This register is not affected by D3HOT to D0 reset or FLR

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:31, F:3] + Ah	03h

Bit Range	Default & Access	Field Name (ID): Description
7:0	03h RW/L	**Sub Class Code (SCC):** This indicates the device is an Intel HD Audio audio device, in the context of a multimedia device. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD

5.1.8 Base Class Code (BCC) - Offset Bh

This register is not affected by D3HOT to D0 reset or FLR

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:31, F:3] + Bh	04h

Bit Range	Default & Access	Field Name (ID): Description
7:0	04h RW/L	**Base Class Code (BCC):** This register indicates that the function implements a multimedia device. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD

5.1.9 Cache Line Size (CLS) - Offset Ch

This register specifies the system cache line size in units of DWORDs.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:31, F:3] + Ch	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Cache Line Size (CLS):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the PCH.

5.1.10 Latency Timer (LT) - Offset Dh

This register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:31, F:3] + Dh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/L	**Latency Timer (LT):** Doesn't apply to PCI Express. RO as 00h if PCI Express. If configured to appear as PCI device, maintain RW for Legacy PCI SW compliance. Locked when FNCFG.HDASPCID = 0 **Locked by:** SBPR.FNCFG.HDASPCID

5.1.11 Header Type (HTYPE) - Offset Eh

This register identifies the layout of the second part of the predefined header and also whether or not the device contains multiple functions.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:31, F:3] + Eh	00h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/L	**Multi Function Device (MFD):** Value of 0 indicates a single function device. Value of 1 indicates a multi-function device. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
6:0	00h RO	**Header Type (HTYPE):** Implements Type 0 Configuration header.

5.1.12 Built-in Self Test (BIST) - Offset Fh

This optional register is used for control and status of BIST.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:31, F:3] + Fh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Built-in Self Test (BIST):** Not implemented in the Intel HD Audio subsystem. Hardwired to 00h.

5.1.13 Intel HD Audio Base Lower Address (HDALBA) - Offset 10h

This BAR creates a selected size of memory space to signify the base address of the Intel HD Audio memory mapped configuration registers depending on implementation.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 10h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:14	00000h RW	**Lower Base Address (LBA):** Base address for the Intel HD Audio subsystem s memory mapped configuration registers. 16 Kbytes are requested by hardwiring bits 13:4 to 0 s.
13:4	0h RO	**Reserved**
3	0h RO	**PREF:** Indicates that this BAR is NOT pre-fetchable.
2:1	2h RO	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in 64-bit address space.
0	0h RO	**Space Type (SPTYP):** Indicates that this BAR is located in memory space.

5.1.14 Intel HD Audio Base Upper Address (HDAUBA) - Offset 14h

This BAR creates a selected size of memory space to signify the base address (upper 32 bits) of the Intel HD Audio memory mapped configuration registers, depending on implementation.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Intel HD Audio Upper Base Address (UBA):** Upper 32 bits of the Base address for the Intel(r) HD Audio controller's memory mapped configuration registers.

5.1.15 Shadowed PCI Configuration Lower Base Address (SPCLBA) - Offset 18h

This BAR creates 4 Kbytes of memory space to signify the base address (lower 32 bits) of the shadowed PCI configuration when used as an ACPI device.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW/L	**Lower Base Address (LBA):** Base address for the PCI Configuration registers shadowed to memory mapped. 4 KB is requested by hardwiring bits 11:4 to 0 s. Locked when PCICFGCTL0.SPCBAD = 1. **Locked by:** SBPR.PCICFGCTL.SPCBAD
11:4	0h RO	**Reserved**
3	0h RO	**PREF:** Indicates that this BAR is NOT pre-fetchable.
2:1	0h RO/V	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in 64-bit address space.
0	0h RO	**Space Type (SPTYP):** Indicates that this BAR is located in memory space.

5.1.16 Shadowed PCI Configuration Upper Base Address (SPCUBA) - Offset 1Ch

This BAR creates 4 Kbytes of memory space to signify the base address (upper 32 bits) of the shadowed PCI configuration when used as an ACPI device.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**Upper Base Address (UBA):** Upper 32 bits of the Base address for the PCI Configuration register shadowed to memory mapped. Locked when PCICFGCTL0.SPCBAD = 1. **Locked by:** SBPR.PCICFGCTL.SPCBAD

5.1.17 Audio DSP Lower Base Address (ADSPLBA) - Offset 20h

This BAR creates a selected size of memory space to signify the base address of the Audio DSP memory mapped configuration registers depending on implementation.

The number of LBA bits in this register is depending on the size of the memory window implemented, represented as x in the register table. The x value is determined by the parameter HDMBABC.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 20h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW	**Lower Base Address (LBA):** Base address for the Audio DSP memory mapped configuration registers.
19:4	0h RO	**Reserved**
3	0h RO	**PREF:** Indicates that this BAR is NOT pre-fetchable.
2:1	2h RO	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in 64-bit address space.
0	0h RO	**Space Type (SPTYP):** Indicates that this BAR is located in memory space.

5.1.18 Audio DSP Upper Base Address (ADSPUBA) - Offset 24h

This BAR creates a selected size of memory space to signify the base address (upper 32 bits) of the Audio DSP memory-mapped configuration registers, depending on implementation.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 24h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Upper Base Address (UBA):** Upper 32 bits of the Base address for the Audio DSP memory mapped configuration registers.

5.1.19 Subsystem Vendor ID (SVID) - Offset 2Ch

This register should be implemented for any function that could be instantiated more than once in a given system, for example, a system with 2 audio subsystems, one down on the motherboard and the other plugged into a PCI expansion slot, should have the SVID register implemented. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one audio subsystem from the other(s).

Software (BIOS) will write the value to this register. After that, the value can be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SID to create one 32-bit write. This register is not affected by D3HOT to D0 reset or FLR

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:3] + 2Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/L	**SVID:** These RW bits have no functionality. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD

5.1.20 Subsystem ID (SID) - Offset 2Eh

This register should be implemented for any function that could be instantiated more than once in a given system, for example, a system with 2 audio subsystems, one down on the motherboard and the other plugged into a PCI expansion slot. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other(s).

Software (BIOS) will write the value to this register. After that, the value can be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SVID to create one 32-bit write. This register is not affected by D3HOT to D0 reset or FLR.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:3] + 2Eh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/L	**SID:** These RW bits have no functionality. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD

5.1.21 Capability Pointer (CAPPTR) - Offset 34h

This optional register is used to point to a linked list of new capabilities implemented by this device.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:31, F:3] + 34h	50h

Bit Range	Default & Access	Field Name (ID): Description
7:0	50h RO	**Capability Pointer (CAPPTR):** Indicates that the first capability pointer offset is offset 50h (Power Management Capability).

5.1.22 Interrupt Line (INTLN) - Offset 3Ch

This register is not affected by FLR. ***Implementation Notes:*** Due to legacy implementation of the INTLN field being implemented as reset by D3HOT to D0 Reset but not FLR and already work well with existing SW (despite FLR section in PCIe

Specification does not have this register in the preservation list), this legacy implementation remains no change and documented here as reset by D3ONLY, which is a deviation from D3RST definition by excluding FLR.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:31, F:3] + 3Ch	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Interrupt Line (INTLN):** Hardware does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

5.1.23 Interrupt Pin (INTPN) - Offset 3Dh

This register is not affected by D3HOT to D0 reset or FLR.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:31, F:3] + 3Dh	01h

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**Reserved**
3:0	1h RW/L	**Interrupt Pin (INTPN):** Identifies the interrupt pin the function uses. 0h: No interrupt pin 1h: INTA 2h: INTB 3h: INTC 4h: INTD 5h Fh: reserved Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD

5.1.24 PCI Power Management Capability ID (PID) - Offset 50h

This register declares the power management capability structure.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:3] + 50h	6001h

Bit Range	Default & Access	Field Name (ID): Description
15:8	60h RW/L	**Next Capability (NEXT):** Points to the next capability structure (MSI). Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
7:0	01h RO	**Cap ID (CAP):** Indicates that this pointer is a PCI power management capability

5.1.25 Power Management Capabilities (PC) - Offset 52h

This register provides information on the capabilities of the function related to power management.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:3] + 52h	C043h

Bit Range	Default & Access	Field Name (ID): Description
15:11	18h RW/L	**PMES:** Indicates PME# can be generated from D3 and D0 states. Programmable by BIOS for the option to declare SUS well wake is supported or not: 19h (SUS well wake supported) or 09h (SUS well wake not supported). Locked when FNCFG.BCLD = 1 **Locked by:** SBPR.FNCFG.BCLD
10	0h RO	**D2S:** The D2 state is not supported.
9	0h RO	**D1S:** The D1 state is not supported.
8:6	1h RW/L	**AC:** Reports 55 mA maximum Suspend well current required when in the D3cold state. Programmable by BIOS for the option to declare SUS well wake is supported or not: 001b (SUS well wake supported) or 000b (SUS well wake not supported). Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
5	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
4	0h RO	**Reserved**
3	0h RO	**PME Clock (PMEC):** Does not apply. Hardwired to 0.
2:0	3h RW/L	**VS:** Indicates support for Revision 1.2 of the PCI Power Management Specification. Programmable by BIOS to older revision if compatibility issue is found. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD

5.1.26 Power Management Control And Status (PCS) - Offset 54h

PMES and PMEE bits reside in Resume well, and reset by resume reset.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 54h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**DT:** Does not apply. Hardwired to 0's.
23	0h RO	**Bus Power/Clock Control Enable (BPCCE):** Does not apply. Hardwired to0.
22	0h RO	**B2/B3 Support (B23):** Does not apply. Hardwired to 0.
21:16	0h RO	**Reserved**
15	0h RW/1C/V	**PME Status (PMES):** This bit is set when the Intel HD Audio controller would normally assert the PME# signal independent of the state of the PME bit. This bit is cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
14:9	0h RO	**Reserved**
8	0h RW	**PME Enable (PMEE):** When set, and if corresponding PMES is also set, the Intel HD Audio subsystem send PME to PMC. This bit is cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
7:4	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
3	1h RW/L	**No Soft Reset (NSR):** When set (1), this bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the Power State bits. When clear (0), devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the Power State bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
2	0h RO	**Reserved**
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the Intel HD Audio subsystem and to set a new power state. The values are: 00 D0 state 11 D3HOT state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3HOT states, the Intel HD Audio subsystem s configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. When software changes this value from the D3HOT state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the function. **Locked by:** SBPR.FNCFG.BCLD

5.1.27 MSI Capability ID (MID) - Offset 60h

NEXT field is not affected by D3HOT to D0 reset or FLR

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:3] + 60h	7005h

Bit Range	Default & Access	Field Name (ID): Description
15:8	70h RO/V	**Next Capability (NEXT):** Points to the PCI Express* capability structure. The value of this field depends on the FNCFG.HDASPCID bit. When FNCFG.HDASPCID is 0 , this field has a value of 70h where it points to the PCI Express capability structure. When FNCFG.HDASPCID bit is 1, this field has a value of 00h to indicate that this is the last capability structure in the list.
7:0	05h RO	**Cap ID (CAP):** Indicates that this pointer is a MSI capability

5.1.28 MSI Message Control (MMC) - Offset 62h

This register provides system software control over MSI.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:3] + 62h	0080h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7	1h RO	**64b Address Capability (ADD64):** Indicates the ability to generate a 64-bit message address
6:4	0h RO	**Multiple Message Enable (MME):** Normally this is a R/W register. However since only 1 message is supported, these bits are hardwired to 000 = 1 message.
3:1	0h RO	**Multiple Message Capable (MMC):** Hardwired to 0 indicating request for 1 message
0	0h RW	**MSI Enable (ME):** If set to 1 an MSI will be generated instead of an INTx# signal. If set to 0, an MSI may not be generated.

5.1.29 MSI Message Lower Address (MMLA) - Offset 64h

This register specifies the MSI message address (lower 32 bits).

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**MSI Message Lower Address (MMLA):** Lower Address used for MSI Message.
1:0	0h RO	**Reserved**

5.1.30 MSI Message Upper Address (MMUA) - Offset 68h

This register specifies the MSI message address (upper 32 bits).

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Message Upper Address (MMUA):** Upper 32 bits of address used for MSI Message.

5.1.31 MSI Message Data (MMD) - Offset 6Ch

This register specifies the MSI message data.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:3] + 6Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**MSI Message Data (MMD):** Data used for MSI Message.

5.1.32 PCI Express Capability ID (PXID) - Offset 70h

This register declares the PCI Express capability structure.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:3] + 70h	0010h

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RO	**Next Capability (NEXT):** Indicates that this is the last capability structure in the list.
7:0	10h RO	**Cap ID (CAP):** Indicates that this pointer is a PCI Express capability structure.

5.1.33 PCI Express Capabilities (PXC) - Offset 72h

This register identifies PCI Express device Function type and associated capabilities.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:3] + 72h	0091h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Reserved**
13:9	00h RO	**Interrupt Message Number (IMN):** Hardwired to 0.
8	0h RO	**Slot Implemented (SI):** Hardwired to 0.
7:4	9h RO	**Device/Port Type (DPT):** Indicates that this is a Root Complex Integrated Endpoint Device.
3:0	1h RO	**Capability Version (CV):** Indicates version #1 PCI Express capability

5.1.34 Device Capabilities (DEVCAP) - Offset 74h

This register is not affected by D3HOT to D0 reset or FLR.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 74h	10000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	1h RW/L	**Functional Level Reset (FLR):** A 1 indicates that the Intel HD Audio subsystem supports the Function Level Reset capability. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
27:26	0h RO	**Captured Slot Power Limit Scale (SPLS):** Hardwired to 0.
25:18	00h RO	**Captured Slot Power Limit Value (SPLV):** Hardwired to 0.
17:15	0h RO	**Reserved**
14	0h RO	**Power Indicator Present (PIP):** Hardwired to 0.
13	0h RO	**Attention Indicator Present (AIP):** Hardwired to 0.
12	0h RO	**Attention Button Present (ABP):** Hardwired to 0.

Bit Range	Default & Access	Field Name (ID): Description
11:9	0h RW/L	**Endpoint L1 Acceptable Latency (L1CAP):** This bit field is defined in the PCI Express spec as RO. At this time it is risky to assign a hardwired value to this bit field. Making it RW would cause a WHQL failure. By making it RW/L it will appear as RO to WHQL testing while allowing BIOS to write a value at boot that is determined by post silicon system testing. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
8:6	0h RW/L	**Endpoint L0s Acceptable Latency (L0SCAP):** This bit field is defined in the PCI Express spec as RO. At this time it is risky to assign a hardwired value to this bit field. Making it RW would cause a WHQL failure. By making it RW/L it will appear as RO to WHQL testing while allowing BIOS to write a value at boot that is determined by post silicon system testing. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
5	0h RO	**Extended Tag Field Support (ETCAP):** Indicates 5 bit tag supported.
4:3	0h RO	**Phantom Functions Supported (PFCAP):** Indicates phantom functions not supported.
2:0	0h RO	**Max Payload Size Supported (MPCAP):** Indicates 128B maximum payload size capability.

5.1.35 Device Control (DEVC) - Offset 78h

NSNPEN bit is not affected by D3HOT to D0 reset or FLR.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:3] + 78h	2800h

Bit Range	Default & Access	Field Name (ID): Description
15	0h WO	**Initiate FLR (IF):** Used to initiate FLR transition. A write of 1 initiates FLR transition. Since hardware must not respond to any cycles until FLR completion, the read value by software from this bit is 0.
14:12	2h RW	**Max Read Request Size (MRRS):** This field sets the maximum Read Request size for the Function as a Requester. The Function must not generate Read Requests with size exceeding the set value. Defined encodings for this field are: 000: 128 B 001: 256 B 010: 512 B 011: 1024 B 100: 2048 B 101: 4096 B 110 111: Reserved
11	1h RW	**Enable No Snoop (NSNPEN):** When set to 1 (or EM2.FNSNPEN = 1) the Intel HD Audio controller is permitted to set the No Snoop bit in the Requester Attributes of a bus master transaction. In this case VC0, VCp, or VC1 may be used for isochronous transfers. When set to 0 (and EM2.FNSNPEN = 0) the Intel HD Audio controller will not set the No Snoop bit. In the case isochronous transfers will not use VC1(VCi) even if it is enabled since VC1 is never snooped. Isochronous transfers will use either VCp or VC0. This bit is not affected by D3HOT to D0 reset or FLR.
10	0h RO	**Auxiliary (AUX) Power PM Enable (AUXPEN):** Hardwired to 0 indicating Intel HD Audio device does not draw AUX power.
9	0h RO	**Phantom Functions Enable (PFEN):** Hardwired to 0 disabling phantom functions.
8	0h RO	**Extended Tag Field Enable (ETEN):** Hardwired to 0 enabling 5-bit tag.
7:5	0h RO	**Max Payload Size (MAXPAY):** Hardwired to 000 indicating 128 B.
4	0h RO	**Enable Relaxed Ordering (ROEN):** Hardwired to 0 disabling relaxed ordering.
3	0h RW	**Unsupported Request Reporting Enable (URREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
2	0h RW	**Fatal Error Reporting Enable (FEREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
1	0h RW	**Non-Fatal Error Reporting Enable (NFEREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
0	0h RW	**Correctable Error Reporting Enable (CEREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.

5.1.36 Device Status (DEVS) - Offset 7Ah

This register provides information about PCI Express device (Function) specific parameters.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:3] + 7Ah	0010h

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RO/V	**Transactions Pending (TXP):** A 1 indicates that the Intel HD Audio controller has issued Non-Posted requests which have not been completed. A 0 indicates that Completions for all Non-Posted Requests have been received.
4	1h RW/L	**AUX Power Detected (AUXDET):** Hardwired to 1 indicating the device is connected to Suspend power. Programmable by BIOS for the option to declare SUS well wake is supported or not: 1b (SUS well wake supported) or 0b (SUS well wake not supported). Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
3	0h RO	**Unsupported Request Detected (URDET):** Not implemented. Hardwired to 0.
2	0h RO	**Fatal Error Detected (FEDET):** Not implemented. Hardwired to 0.
1	0h RO	**Non-Fatal Error Detected (NFEDET):** Not implemented. Hardwired to 0.
0	0h RO	**Correctable Error Detected (CEDET):** Not implemented. Hardwired to 0.

5.1.37 Vendor Specific Capability Identifiers (VSCID) - Offset 80h

This register declares the vendor specific capability structure.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 80h	F0146009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor-Specific Capability ID (VSID):** A value of Fh in this 4-bit field identifies this Vendor Specific Capability as an Extended Capability, which uses a VSEC 16-bit Extended Capability ID in the subsequent four bytes. This field allows software to differentiate this capability from other Vendor Specific capabilities.
27:24	0h RO	**Vendor Specific Capability Revision (VSREV):** For a VSID of Fh, this field is reserved 0h.

Bit Range	Default & Access	Field Name (ID): Description
23:16	14h RO	**Vendor Specific Capability Length (VSLEN):** This field indicates the # of bytes of this Vendor Specific capability as required by the PCI spec inclusive of the CapID and Next Pointer.
15:8	60h RW/L	**Next Capability (NEXT):** Points to the next capability structure (MSI). Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
7:0	09h RO	**Cap ID (CAP):** Indicates that this pointer is a vendor specific capability.

5.1.38 Vendor Specific Extended Capability (VSECID) - Offset 84h

This register declares the vendor specific extended capability structure.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 84h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific Extended Capability Length (VSECLEN):** This field indicates the # of bytes of this Vendor Specific capability inclusive of the 1st DW which includes the capability ID and Next pointer. For DevIdle, this is 14h.
19:16	0h RO	**Vendor Specific Extended Capability Revision (VSEREV):** For this revision of DevIdle, this field is 0h.
15:0	0010h RO	**Vendor Specific Extended Capability ID (VSECID):** DevIdle has been assigned the Intel VSEC ID of 10h.

5.1.39 Device Idle Pointer (DEVIDLEPTR) - Offset 8Ch

This register specifies the location pointer to the DevIdle register in MMIO space.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 8Ch	000104A1h

Bit Range	Default & Access	Field Name (ID): Description
31:4	000104Ah RO	**DevIdle MMIO Offset Location (DEVIDLELOC):** This register contains the location pointer to the DevIdle register in MMIO space, as an offset from the specified BAR.
3:1	0h RO	**Base Address Register Number (BARNUM):** Contains the 0s based BAR Number of the BAR which contains the location of the DevIdle MMIO register.
0	1h RO	**VALID:** Set to 1 to indicate that the function has implemented a DevIdle register as specified in the DevIdle that can be located using the DEVIDLELOC register and BARNUM.

5.1.40 Device Idle Power On Latency (DEVIDLEPOL) - Offset 90h

This register specifies the device idle power on latency.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:3] + 90h	0800h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**Reserved**
12:10	2h RW/L	**Power On Latency Scale (POLS):** Latency Scale multiplier: 010: 1 us 011: 32 us All other settings are reserved. The value of this register is multiplied with the Power On Latency Value (POLV) to provide the DevIdle power on exit latency multiplier scale from 1us to 32us. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
9:0	000h RW/L	**Power On Latency Value (POLV):** Contains the 0#s based BAR Number of the BAR which contains the location of the DevIdle MMIO register. **Locked by:** SBPR.FNCFG.BCLD

5.1.41 Manufacturing Process (MANID) - Offset F8h

This register reports the manufacturing and process details.

Implementation Notes: The actual implementation of the register needs on be on IOSF Sideband reset which de-asserts earlier than platform reset, so that it may receive the Set ID message over IOSF Sideband during initialization (before platform reset de-asserts).

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/P	**Manufacturers ID Field (MANID)**: Manufacturer ID: Default value comes from straps.

5.1.42 Virtual Channel Enhanced Capability Header (VCCAP) - Offset 100h

This register is not affected by D3HOT to D0 reset or FLR.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 100h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/L	**Next Capability Offset (NXTCAP):** Points to the next capability header, which is the Root Complex Link Declaration Enhanced Capability Header. This register is RW/L to support removing the Root Complex Topology Capability from the PCI Express Extended Capability List. For systems which support the Root Complex Topology Capability Structure, boot BIOS should write a 130h to this register, otherwise boot BIOS should write a 000h to this register. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
19:16	0h RW/L	**Capability Version (CV):** This register is RW/L to support removing the PCI Express Extended Capabilities from the Intel HD Audio subsystem. For systems which support the PCI Express Virtual Channel capability and the Root Complex Topology Capability Structure, boot BIOS should write a 1h to this register, otherwise boot BIOS should write a 0h to this register. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
15:0	0000h RW/L	**PCI Express Extended Capability ID (PCIEECID):** This register is RW/L to support removing the PCI Express Extended Capabilities from the Intel HD Audio subsystem. For systems which support the PCI Express Virtual Channel capability and the Root Complex Topology Capability Structure, boot BIOS should write a 0002h to this register, otherwise boot BIOS should write a 0000h to this register. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD

5.1.43 Port VC Capability Register 1 (PVCCAP1) - Offset 104h

This register describes the configuration of the Virtual Channels associated with a PCI Express Port.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 104h	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:10	0h RO	**Port Arbitration Table Entry Size (PARBTBLES):** This is an endpoint device therefore this field is hardwired to 0 s.
9:8	0h RO	**Reference Clock (RC):** This is an endpoint device therefore this field is hardwired to 0 s.
7	0h RO	**Reserved**
6:4	0h RO	**Low Priority Extended VC Count (LPVCCNT):** Indicates that only VC0 belongs to the low-priority VC group.
3	0h RO	**Reserved**
2:0	1h RO	**Extended VC Count (VCCNT):** Indicates that one extended VC (in addition to VC0) is supported by the Intel(r) HD Audio controller.

5.1.44 Port VC Capability Register 2 (PVCCAP2) - Offset 108h

This register provides further information about the configuration of the Virtual Channels associated with a PCI Express Port.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 108h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**VC Arbitration Table Offset (VCARBTBL):** Hardwired to 0 indicating that a VC Arbitration Table is not present.
23:8	0h RO	**Reserved**
7:0	00h RO	**VC Arbitration Capability (VCARBCAP):** Hardwired to 0 s. These bits are not applicable since the Intel HD Audio controller reports a 0 in the Low Priority Extended VC Count field.

5.1.45 Port VC Control Register (PVCCTL) - Offset 10Ch

This register provides control of the configuration of Virtual Channels associated with a Port.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:3] + 10Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:4	0h RO	**Reserved**
3:1	0h RO	**VC Arbitration Select (VCARBSEL):** Hardwired to 0 s. Normally these bits are RW. But these bits are not applicable since the Intel HD Audio controller reports a 0 in the Low Priority Extended VC Count field.
0	0h RO	**Load VC Arbitration Table (LVCARBTBL):** Hardwired to 0 since an arbitration table is not present.

5.1.46 Port VC Status Register (PVCSTS) - Offset 10Eh

This register provides status of the configuration of Virtual Channels associated with a Port.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:3] + 10Eh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:1	0h RO	**Reserved**
0	0h RO	**VC Arbitration Table Status (VCARBTBLSTS):** Hardwired to 0 since the VC Arbitration Table is not present.

5.1.47 VC0 Resource Capability Register (VC0CAP) - Offset 110h

This register describes the capabilities and configuration of VC0 Virtual Channel resource.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 110h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Port Arbitration Table Offset (PARBTBL):** Hardwired to 0 since this field is not valid for endpoint devices.
23	0h RO	**Reserved**
22:16	00h RO	**Maximum Time Slots (MTS):** Hardwired to 0 since this field is not valid for endpoint devices.
15	0h RO	**Reject Snoop Transactions (RST):** Hardwired to 0 since this field is not valid for endpoint devices.
14	0h RO	**Advanced Packet Switching (APS):** Hardwired to 0 since this field is not valid for endpoint devices.
13:8	0h RO	**Reserved**
7:0	00h RO	**Port Arbitration Capability (PARBCAP):** Hardwired to 0 since this field is not valid for endpoint devices.

5.1.48 VC0 Resource Control Register (VC0CTL) - Offset 114h

VC0MAP(7:1) field is not affected by FLR.

Implementation Notes: Due to legacy implementation of the VC0MAP field being implemented as reset by D3HOT to D0 Reset but not FLR and already work well with existing SW (and there is no clear definition in the PCI and PCIe Specification whether it should be reset by D3HOT to D0 Reset or not), this legacy implementation remains no change and documented here as reset by D3ONLY, which is a deviation from D3RST definition by excluding FLR.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 114h	800000FFh

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**VC0 Enable (VC0EN):** Hardwired to 1 for VC0.
30:27	0h RO	**Reserved**
26:24	0h RO	**VC0 ID (VC0ID):** Hardwired to 0 since the first VC is always assigned as VC0.
23:20	0h RO	**Reserved**
19:17	0h RO	**Port Arbitration Select (PARBSEL):** Hardwired to 0 since this field is not valid for endpoint devices.
16	0h RO	**Load Port Arbitration Table (LPARBTBL):** Hardwired to 0 since this field is not valid for endpoint devices.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:1	7Fh RW	**TC/VC0 Map (VC0MAP):** Bits (7:1) are implemented as R/W bits. This field is not used by the hardware, but it is RW to avoid confusing software.
0	1h RO	**TC/VC0 Map (VC0MAP_0):** Bit 0 is hardwired to 1 since TC0 is always mapped to VC0

5.1.49 VC0 Resource Status Register (VC0STS) - Offset 11Ah

This register provides status of the configuration of VC0 Virtual Channels.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:3] + 11Ah	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**
1	0h RO	**VC0 Negotiation Pending (VCNP):** This bit does not apply to the integrated Intel HD Audio device and is therefore hardwired to 0.
0	0h RO	**Port Arbitration Table Status (PARBTBLSTS):** Hardwired to 0 since this field is not valid for endpoint devices.

5.1.50 VCI Resource Capability Register (VCICAP) - Offset 11Ch

This register describes the capabilities and configuration of VC1 Virtual Channel resource.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 11Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Port Arbitration Table Offset (PARBTBL):** Hardwired to 0 since this field is not valid for endpoint devices.
23	0h RO	**Reserved**
22:16	00h RO	**Maximum Time Slots (MTS):** Hardwired to 0 since this field is not valid for endpoint devices.
15	0h RO	**Reject Snoop Transactions (RST):** Hardwired to 0 since this field is not valid for endpoint devices.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**Advanced Packet Switching (APS):** Hardwired to 0 since this field is not valid for endpoint devices.
13:8	0h RO	**Reserved**
7:0	00h RO	**Port Arbitration Capability (PARBCAP):** Hardwired to 0 since this field is not valid for endpoint devices.

5.1.51 VCI Resource Control Register (VCICTL) - Offset 120h

VCIEN bit and VCIID field are not affected by D3HOT to D0 Reset or FLR. VCiM(7:1) field is not affected by FLR.

Implementation Notes: Due to legacy implementation of the VCiM field being implemented as reset by D3HOT to D0 Reset but not FLR and already work well with existing SW (and there is no clear definition in the PCI and PCIe. Specification whether it should be reset by D3HOT to D0 Reset or not), this legacy implementation remains no change and documented here as reset by D3ONLY, which is a deviation from D3RST definition by excluding FLR.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 120h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**VCi Enable (VCIEN):** When set to 1, VCi is enabled. This bit is not affected by D3HOT to D0 reset.
30:27	0h RO	**Reserved**
26:24	0h RW	**VCI ID (VCIID):** This field assigns a VC ID to the VCI resource. This field is not used by the PCH hardware, but it is RW to avoid confusing software. These bits are not affected by D3HOT to D0 reset.
23:20	0h RO	**Reserved**
19:17	0h RO	**Port Arbitration Select (PARBSEL):** Hardwired to 0 since this field is not valid for endpoint devices.
16	0h RO	**Load Port Arbitration Table (LPARBTBL):** Hardwired to 0 since this field is not valid for endpoint devices.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:1	00h RW	**TC/VCI Map (VCIM):** This field indicates the TCs that are mapped to the VCi resource. Bits (7:1) are implemented as RW bits. This field is not used by the hardware, but it is RW to avoid confusing software.
0	0h RO	**TC/VCI Map (VCIM_0):** This field indicates the TCs that are mapped to the VCI resource. Bit 0 is hardwired to 0 indicating it can not be mapped to VCI. This field is not used by the hardware.

5.1.52 VCI Resource Status Register (VCISTS) - Offset 126h

This register provides status of the configuration of VC1 Virtual Channels.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:3] + 126h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**
1	0h RO	**VCI Negotiation Pending (VCNP):** This bit does not apply to the integrated Intel HD Audio subsystem and is therefore hardwired to 0.
0	0h RO	**Port Arbitration Table Status (PARBTBLSTS):** Hardwired to 0 since this field is not valid for endpoint devices.

5.1.53 Root Complex Link Declaration Enhanced (RCCAP) - Offset 130h

This register declares the root complex link enhanced capability structure.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 130h	00010005h

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RO	**Next Capability Offset (NXTCAP):** Indicates this is the last capability.
19:16	1h RO	**Capability Version (CV):** Indicates the version of the capability structure present.
15:0	0005h RO	**PCI Express Extended Capability ID (PCIEECID):** Indicates that this pointer is a Root Complex Link Declaration Enhanced capability.

5.1.54 Element Self Description (ESD) - Offset 134h

This register provides information about the Root Complex element containing the Link Declaration Capability.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 134h	0F000100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0Fh RO	**Port Number (PORT):** Intel HD Audio assigned as Port #15.
23:16	00h RW/L	**Component ID (COMPID):** Indicates the component ID assigned to this element by software. This is written once by platform BIOS and is locked until a platform reset. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
15:8	01h RO	**Number of Link Entries (LNKENT):** The Intel HD Audio controller only connects to one device, the SOC egress port. Therefore this field reports a value of 1.
7:4	0h RO	**Reserved**
3:0	0h RO	**Element Type (ELTYP):** The Intel HD Audio controller is an Integrated Root Complex Device. Therefore this field reports a value of 0h.

5.1.55 Link 1 Description (L1DESC) - Offset 140h

This register describes the link entry attributes.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 140h	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Target Port Number (TPORT):** The Intel HD Audio controller targets the SOC RCRB egress port, which is port #0.
23:16	00h RW/L	**Target Component ID (TCOMPID):** This field is programmed by platform BIOS to match the component ID of the SOC RCRB that is attached to this RCRB Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**
1	0h RO	**Link Type (LNKTYP):** Indicates Type 0.
0	1h RO	**Link Valid (LNKVLD):** Hardwired to 1.

5.1.56 Link 1 Lower Address (L1LADD) - Offset 148h

This register specifies the pointer (lower 32 bits) to a memory-mapped RCRB.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 148h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	00000h RO/V	**Link 1 Lower Address (L1LADD):** Hardwired to match the RCBA register value in the PCI-LPC bridge.
13:0	0h RO	**Reserved**

5.1.57 Link 1 Upper Address (L1UADD) - Offset 14Ch

This register specifies the pointer (upper 32 bits) to a memory-mapped RCRB.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:3] + 14Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link 1 Upper Address (L1UADD):** Hardwired to match the RCBA register value in the PCI-LPC bridge.

5.2 cAVS Memory Mapped Register Summary

Table 5-2. Summary of cAVS Memory Mapped Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	Global Capabilities (GCAP)	9701h
2h	1	Minor Version (VMIN)	00h
3h	1	Major Version (VMAJ)	01h
4h	2	Output Payload Capability (OUTPAY)	003Ch
6h	2	Input Payload Capability (INPAY)	001Dh
8h	4	Global Control (GCTL)	00000000h
Ch	2	Wake Enable (WAKEEN)	0000h
Eh	2	Wake Status (WAKESTS)	0000h
10h	2	Global Status (GSTS)	0000h
12h	2	Global Capabilities 2 (GCAP2)	0001h
14h	2	Linked List Capabilities Header (LLCH)	0C00h
18h	2	Output Stream Payload Capability (OUTSTRMPAY)	0030h
1Ah	2	Input Stream Payload Capability (INSTRMPAY)	0018h
20h	4	Interrupt Control (INTCTL)	00000000h
24h	4	Interrupt Status (INTSTS)	00000000h
30h	4	Wall Clock Counter (WALCLK)	00000000h
38h	4	Stream Synchronization (SSYNC)	00000000h
40h	4	CORB Lower Base Address (CORBLBASE)	00000000h
44h	4	CORB Upper Base Address (CORBUBASE)	00000000h
48h	2	CORB Write Pointer (CORBWP)	0000h
4Ah	2	CORB Read Pointer (CORBRP)	0000h
4Ch	1	CORB Control (CORBCTL)	00h
4Dh	1	CORB Status (CORBSTS)	00h
4Eh	1	CORB Size (CORBSIZE)	42h
50h	4	RIRB Lower Base Address (RIRBLBASE)	00000000h
54h	4	RIRB Upper Base Address (RIRBUBASE)	00000000h
58h	2	RIRB Write Pointer (RIRBWP)	0000h
5Ah	2	Response Interrupt Count (RINTCNT)	0000h
5Ch	1	RIRB Control (RIRBCTL)	00h
5Dh	1	RIRB Status (RIRBSTS)	00h
5Eh	1	RIRB Size (RIRBSIZE)	42h
60h	4	Immediate Command (IC)	00000000h
64h	4	Immediate Response (IR)	00000000h
68h	2	Immediate Command Status (ICS)	0000h
70h	4	DMA Position Lower Base Address (DPLBASE)	00000000h
74h	4	DMA Position Upper Base Address (DPUBASE)	00000000h
80h	1	Input/Output Stream Descriptor x Control (ISD0CTLB0)	00h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
83h	1	Input/Output Stream Descriptor x Status (ISD0STS)	00h
84h	4	Input/Output Stream Descriptor x Link Position in Buffer (ISD0LPIB)	00000000h
88h	4	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD0CBL)	00000000h
8Ch	2	Input/Output Stream Descriptor x Last Valid Index (ISD0LVI)	0000h
8Eh	2	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD0FIFOW)	0004h
90h	2	Input/Output Stream Descriptor x FIFO Size (ISD0FIFOS)	0000h
92h	2	Input/Output Stream Descriptor x Format (ISD0FMT)	0000h
94h	2	Input/Output Stream Descriptor x FIFO Limit (ISD0FIFOL)	0000h
98h	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD0BDLPLBA)	00000000h
9Ch	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD0BDLPUBA)	00000000h
A0h	1	Input/Output Stream Descriptor x Control (ISD1CTLB0)	00h
A3h	1	Input/Output Stream Descriptor x Status (ISD1STS)	00h
A4h	4	Input/Output Stream Descriptor x Link Position in Buffer (ISD1LPIB)	00000000h
A8h	4	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD1CBL)	00000000h
ACh	2	Input/Output Stream Descriptor x Last Valid Index (ISD1LVI)	0000h
AEh	2	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD1FIFOW)	0004h
B0h	2	Input/Output Stream Descriptor x FIFO Size (ISD1FIFOS)	0000h
B2h	2	Input/Output Stream Descriptor x Format (ISD1FMT)	0000h
B4h	2	Input/Output Stream Descriptor x FIFO Limit (ISD1FIFOL)	0000h
B8h	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD1BDLPLBA)	00000000h
BCh	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD1BDLPUBA)	00000000h
C0h	1	Input/Output Stream Descriptor x Control (ISD2CTLB0)	00h
C3h	1	Input/Output Stream Descriptor x Status (ISD2STS)	00h
C4h	4	Input/Output Stream Descriptor x Link Position in Buffer (ISD2LPIB)	00000000h
C8h	4	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD2CBL)	00000000h
CCh	2	Input/Output Stream Descriptor x Last Valid Index (ISD2LVI)	0000h
CEh	2	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD2FIFOW)	0004h
D0h	2	Input/Output Stream Descriptor x FIFO Size (ISD2FIFOS)	0000h
D2h	2	Input/Output Stream Descriptor x Format (ISD2FMT)	0000h
D4h	2	Input/Output Stream Descriptor x FIFO Limit (ISD2FIFOL)	0000h
D8h	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD2BDLPLBA)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
DCh	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD2BDLPUBA)	00000000h
E0h	1	Input/Output Stream Descriptor x Control (ISD3CTLB0)	00h
E3h	1	Input/Output Stream Descriptor x Status (ISD3STS)	00h
E4h	4	Input/Output Stream Descriptor x Link Position in Buffer (ISD3LPIB)	00000000h
E8h	4	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD3CBL)	00000000h
ECh	2	Input/Output Stream Descriptor x Last Valid Index (ISD3LVI)	0000h
EEh	2	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD3FIFOW)	0004h
F0h	2	Input/Output Stream Descriptor x FIFO Size (ISD3FIFOS)	0000h
F2h	2	Input/Output Stream Descriptor x Format (ISD3FMT)	0000h
F4h	2	Input/Output Stream Descriptor x FIFO Limit (ISD3FIFOL)	0000h
F8h	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD3BDLPLBA)	00000000h
FCh	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD3BDLPUBA)	00000000h
100h	1	Input/Output Stream Descriptor x Control (ISD4CTLB0)	00h
103h	1	Input/Output Stream Descriptor x Status (ISD4STS)	00h
104h	4	Input/Output Stream Descriptor x Link Position in Buffer (ISD4LPIB)	00000000h
108h	4	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD4CBL)	00000000h
10Ch	2	Input/Output Stream Descriptor x Last Valid Index (ISD4LVI)	0000h
10Eh	2	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD4FIFOW)	0004h
110h	2	Input/Output Stream Descriptor x FIFO Size (ISD4FIFOS)	0000h
112h	2	Input/Output Stream Descriptor x Format (ISD4FMT)	0000h
114h	2	Input/Output Stream Descriptor x FIFO Limit (ISD4FIFOL)	0000h
118h	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD4BDLPLBA)	00000000h
11Ch	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD4BDLPUBA)	00000000h
120h	1	Input/Output Stream Descriptor x Control (ISD5CTLB0)	00h
123h	1	Input/Output Stream Descriptor x Status (ISD5STS)	00h
124h	4	Input/Output Stream Descriptor x Link Position in Buffer (ISD5LPIB)	00000000h
128h	4	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD5CBL)	00000000h
12Ch	2	Input/Output Stream Descriptor x Last Valid Index (ISD5LVI)	0000h
12Eh	2	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD5FIFOW)	0004h
130h	2	Input/Output Stream Descriptor x FIFO Size (ISD5FIFOS)	0000h
132h	2	Input/Output Stream Descriptor x Format (ISD5FMT)	0000h
134h	2	Input/Output Stream Descriptor x FIFO Limit (ISD5FIFOL)	0000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
138h	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD5BDLPLBA)	00000000h
13Ch	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD5BDLPUBA)	00000000h
140h	1	Input/Output Stream Descriptor x Control (ISD6CTLB0)	00h
143h	1	Input/Output Stream Descriptor x Status (ISD6STS)	00h
144h	4	Input/Output Stream Descriptor x Link Position in Buffer (ISD6LPIB)	00000000h
148h	4	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD6CBL)	00000000h
14Ch	2	Input/Output Stream Descriptor x Last Valid Index (ISD6LVI)	0000h
14Eh	2	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD6FIFOW)	0004h
150h	2	Input/Output Stream Descriptor x FIFO Size (ISD6FIFOS)	0000h
152h	2	Input/Output Stream Descriptor x Format (ISD6FMT)	0000h
154h	2	Input/Output Stream Descriptor x FIFO Limit (ISD6FIFOL)	0000h
158h	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD6BDLPLBA)	00000000h
15Ch	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD6BDLPUBA)	00000000h
160h	1	Input/Output Stream Descriptor x Control (OSD0CTLB0)	00h
163h	1	Input/Output Stream Descriptor x Status (OSD0STS)	00h
164h	4	Input/Output Stream Descriptor x Link Position in Buffer (OSD0LPIB)	00000000h
168h	4	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD0CBL)	00000000h
16Ch	2	Input/Output Stream Descriptor x Last Valid Index (OSD0LVI)	0000h
16Eh	2	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD0FIFOW)	0004h
170h	2	Input/Output Stream Descriptor x FIFO Size (OSD0FIFOS)	0000h
172h	2	Input/Output Stream Descriptor x Format (OSD0FMT)	0000h
174h	2	Input/Output Stream Descriptor x FIFO Limit (OSD0FIFOL)	0000h
178h	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD0BDLPLBA)	00000000h
17Ch	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD0BDLPUBA)	00000000h
180h	1	Input/Output Stream Descriptor x Control (OSD1CTLB0)	00h
183h	1	Input/Output Stream Descriptor x Status (OSD1STS)	00h
184h	4	Input/Output Stream Descriptor x Link Position in Buffer (OSD1LPIB)	00000000h
188h	4	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD1CBL)	00000000h
18Ch	2	Input/Output Stream Descriptor x Last Valid Index (OSD1LVI)	0000h
18Eh	2	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD1FIFOW)	0004h
190h	2	Input/Output Stream Descriptor x FIFO Size (OSD1FIFOS)	0000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
192h	2	Input/Output Stream Descriptor x Format (OSD1FMT)	0000h
194h	2	Input/Output Stream Descriptor x FIFO Limit (OSD1FIFOL)	0000h
198h	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD1BDLPLBA)	00000000h
19Ch	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD1BDLPUBA)	00000000h
1A0h	1	Input/Output Stream Descriptor x Control (OSD2CTLB0)	00h
1A3h	1	Input/Output Stream Descriptor x Status (OSD2STS)	00h
1A4h	4	Input/Output Stream Descriptor x Link Position in Buffer (OSD2LPIB)	00000000h
1A8h	4	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD2CBL)	00000000h
1ACh	2	Input/Output Stream Descriptor x Last Valid Index (OSD2LVI)	0000h
1AEh	2	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD2FIFOW)	0004h
1B0h	2	Input/Output Stream Descriptor x FIFO Size (OSD2FIFOS)	0000h
1B2h	2	Input/Output Stream Descriptor x Format (OSD2FMT)	0000h
1B4h	2	Input/Output Stream Descriptor x FIFO Limit (OSD2FIFOL)	0000h
1B8h	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD2BDLPLBA)	00000000h
1BCh	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD2BDLPUBA)	00000000h
1C0h	1	Input/Output Stream Descriptor x Control (OSD3CTLB0)	00h
1C3h	1	Input/Output Stream Descriptor x Status (OSD3STS)	00h
1C4h	4	Input/Output Stream Descriptor x Link Position in Buffer (OSD3LPIB)	00000000h
1C8h	4	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD3CBL)	00000000h
1CCh	2	Input/Output Stream Descriptor x Last Valid Index (OSD3LVI)	0000h
1CEh	2	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD3FIFOW)	0004h
1D0h	2	Input/Output Stream Descriptor x FIFO Size (OSD3FIFOS)	0000h
1D2h	2	Input/Output Stream Descriptor x Format (OSD3FMT)	0000h
1D4h	2	Input/Output Stream Descriptor x FIFO Limit (OSD3FIFOL)	0000h
1D8h	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD3BDLPLBA)	00000000h
1DCh	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD3BDLPUBA)	00000000h
1E0h	1	Input/Output Stream Descriptor x Control (OSD4CTLB0)	00h
1E3h	1	Input/Output Stream Descriptor x Status (OSD4STS)	00h
1E4h	4	Input/Output Stream Descriptor x Link Position in Buffer (OSD4LPIB)	00000000h
1E8h	4	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD4CBL)	00000000h
1ECh	2	Input/Output Stream Descriptor x Last Valid Index (OSD4LVI)	0000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1EEh	2	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD4FIFOW)	0004h
1F0h	2	Input/Output Stream Descriptor x FIFO Size (OSD4FIFOS)	0000h
1F2h	2	Input/Output Stream Descriptor x Format (OSD4FMT)	0000h
1F4h	2	Input/Output Stream Descriptor x FIFO Limit (OSD4FIFOL)	0000h
1F8h	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD4BDLPLBA)	00000000h
1FCh	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD4BDLPUBA)	00000000h
200h	1	Input/Output Stream Descriptor x Control (OSD5CTLB0)	00h
203h	1	Input/Output Stream Descriptor x Status (OSD5STS)	00h
204h	4	Input/Output Stream Descriptor x Link Position in Buffer (OSD5LPIB)	00000000h
208h	4	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD5CBL)	00000000h
20Ch	2	Input/Output Stream Descriptor x Last Valid Index (OSD5LVI)	0000h
20Eh	2	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD5FIFOW)	0004h
210h	2	Input/Output Stream Descriptor x FIFO Size (OSD5FIFOS)	0000h
212h	2	Input/Output Stream Descriptor x Format (OSD5FMT)	0000h
214h	2	Input/Output Stream Descriptor x FIFO Limit (OSD5FIFOL)	0000h
218h	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD5BDLPLBA)	00000000h
21Ch	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD5BDLPUBA)	00000000h
220h	1	Input/Output Stream Descriptor x Control (OSD6CTLB0)	00h
223h	1	Input/Output Stream Descriptor x Status (OSD6STS)	00h
224h	4	Input/Output Stream Descriptor x Link Position in Buffer (OSD6LPIB)	00000000h
228h	4	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD6CBL)	00000000h
22Ch	2	Input/Output Stream Descriptor x Last Valid Index (OSD6LVI)	0000h
22Eh	2	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD6FIFOW)	0004h
230h	2	Input/Output Stream Descriptor x FIFO Size (OSD6FIFOS)	0000h
232h	2	Input/Output Stream Descriptor x Format (OSD6FMT)	0000h
234h	2	Input/Output Stream Descriptor x FIFO Limit (OSD6FIFOL)	0000h
238h	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD6BDLPLBA)	00000000h
23Ch	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD6BDLPUBA)	00000000h
240h	1	Input/Output Stream Descriptor x Control (OSD7CTLB0)	00h
243h	1	Input/Output Stream Descriptor x Status (OSD7STS)	00h
244h	4	Input/Output Stream Descriptor x Link Position in Buffer (OSD7LPIB)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
248h	4	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD7CBL)	00000000h
24Ch	2	Input/Output Stream Descriptor x Last Valid Index (OSD7LVI)	0000h
24Eh	2	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD7FIFOW)	0004h
250h	2	Input/Output Stream Descriptor x FIFO Size (OSD7FIFOS)	0000h
252h	2	Input/Output Stream Descriptor x Format (OSD7FMT)	0000h
254h	2	Input/Output Stream Descriptor x FIFO Limit (OSD7FIFOL)	0000h
258h	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD7BDLPLBA)	00000000h
25Ch	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD7BDLPUBA)	00000000h
260h	1	Input/Output Stream Descriptor x Control (OSD8CTLB0)	00h
263h	1	Input/Output Stream Descriptor x Status (OSD8STS)	00h
264h	4	Input/Output Stream Descriptor x Link Position in Buffer (OSD8LPIB)	00000000h
268h	4	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD8CBL)	00000000h
26Ch	2	Input/Output Stream Descriptor x Last Valid Index (OSD8LVI)	0000h
26Eh	2	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD8FIFOW)	0004h
270h	2	Input/Output Stream Descriptor x FIFO Size (OSD8FIFOS)	0000h
272h	2	Input/Output Stream Descriptor x Format (OSD8FMT)	0000h
274h	2	Input/Output Stream Descriptor x FIFO Limit (OSD8FIFOL)	0000h
278h	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD8BDLPLBA)	00000000h
27Ch	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD8BDLPUBA)	00000000h
500h	4	Global Time Synchronization Capability Header (GTSCH)	00011F00h
504h	4	Global Time Synchronization Capability Declaration (GTSCD)	00000000h
520h	4	Global Time Synchronization Capture Control (GTSCC0)	00000000h
524h	4	Wall Frame Counter Captured (WALFCC0)	00000000h
528h	4	Time Stamp Counter Captured Lower (TSCCL0)	00000000h
52Ch	4	Time Stamp Counter Captured Upper (TSCCU0)	00000000h
534h	4	Linear Link Position Frame Offset Captured (LLPFOC0)	00000000h
538h	4	Linear Link Position Captured Lower (LLPCL0)	00000000h
53Ch	4	Linear Link Position Captured Upper (LLPCU0)	00000000h
540h	4	Global Time Synchronization Capture Control (GTSCC1)	00000000h
544h	4	Wall Frame Counter Captured (WALFCC1)	00000000h
548h	4	Time Stamp Counter Captured Lower (TSCCL1)	00000000h
54Ch	4	Time Stamp Counter Captured Upper (TSCCU1)	00000000h
554h	4	Linear Link Position Frame Offset Captured (LLPFOC1)	00000000h
558h	4	Linear Link Position Captured Lower (LLPCL1)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
55Ch	4	Linear Link Position Captured Upper (LLPCU1)	00000000h
700h	4	Software Position Based FIFO Capability Header (SPBFCH)	00040000h
704h	4	Software Position Based FIFO Control (SPBFCTL)	00000000h
708h	4	Input/Output Stream Descriptor x Software Position in Buffer (ISD0SPIB)	00000000h
70Ch	4	Input/Output Stream Descriptor x Max FIFO Size (ISD0MAXFIFOS)	00000000h
710h	4	Input/Output Stream Descriptor x Software Position in Buffer (ISD1SPIB)	00000000h
714h	4	Input/Output Stream Descriptor x Max FIFO Size (ISD1MAXFIFOS)	00000000h
718h	4	Input/Output Stream Descriptor x Software Position in Buffer (ISD2SPIB)	00000000h
71Ch	4	Input/Output Stream Descriptor x Max FIFO Size (ISD2MAXFIFOS)	00000000h
720h	4	Input/Output Stream Descriptor x Software Position in Buffer (ISD3SPIB)	00000000h
724h	4	Input/Output Stream Descriptor x Max FIFO Size (ISD3MAXFIFOS)	00000000h
728h	4	Input/Output Stream Descriptor x Software Position in Buffer (ISD4SPIB)	00000000h
72Ch	4	Input/Output Stream Descriptor x Max FIFO Size (ISD4MAXFIFOS)	00000000h
730h	4	Input/Output Stream Descriptor x Software Position in Buffer (ISD5SPIB)	00000000h
734h	4	Input/Output Stream Descriptor x Max FIFO Size (ISD5MAXFIFOS)	00000000h
738h	4	Input/Output Stream Descriptor x Software Position in Buffer (ISD6SPIB)	00000000h
73Ch	4	Input/Output Stream Descriptor x Max FIFO Size (ISD6MAXFIFOS)	00000000h
740h	4	Input/Output Stream Descriptor x Software Position in Buffer (OSD0SPIB)	00000000h
744h	4	Input/Output Stream Descriptor x Max FIFO Size (OSD0MAXFIFOS)	00000000h
748h	4	Input/Output Stream Descriptor x Software Position in Buffer (OSD1SPIB)	00000000h
74Ch	4	Input/Output Stream Descriptor x Max FIFO Size (OSD1MAXFIFOS)	00000000h
750h	4	Input/Output Stream Descriptor x Software Position in Buffer (OSD2SPIB)	00000000h
754h	4	Input/Output Stream Descriptor x Max FIFO Size (OSD2MAXFIFOS)	00000000h
758h	4	Input/Output Stream Descriptor x Software Position in Buffer (OSD3SPIB)	00000000h
75Ch	4	Input/Output Stream Descriptor x Max FIFO Size (OSD3MAXFIFOS)	00000000h
760h	4	Input/Output Stream Descriptor x Software Position in Buffer (OSD4SPIB)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
764h	4	Input/Output Stream Descriptor x Max FIFO Size (OSD4MAXFIFOS)	00000000h
768h	4	Input/Output Stream Descriptor x Software Position in Buffer (OSD5SPIB)	00000000h
76Ch	4	Input/Output Stream Descriptor x Max FIFO Size (OSD5MAXFIFOS)	00000000h
770h	4	Input/Output Stream Descriptor x Software Position in Buffer (OSD6SPIB)	00000000h
774h	4	Input/Output Stream Descriptor x Max FIFO Size (OSD6MAXFIFOS)	00000000h
778h	4	Input/Output Stream Descriptor x Software Position in Buffer (OSD7SPIB)	00000000h
77Ch	4	Input/Output Stream Descriptor x Max FIFO Size (OSD7MAXFIFOS)	00000000h
780h	4	Input/Output Stream Descriptor x Software Position in Buffer (OSD8SPIB)	00000000h
784h	4	Input/Output Stream Descriptor x Max FIFO Size (OSD8MAXFIFOS)	00000000h
800h	4	Processing Pipe Capability Header (PPCH)	00030500h
804h	4	Processing Pipe Control (PPCTL)	00000000h
808h	4	Processing Pipe Status (PPSTS)	00000000h
810h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC0LLPL)	00000000h
814h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC0LLPU)	00000000h
818h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC0LDPL)	00000000h
81Ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC0LDPU)	00000000h
820h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC1LLPL)	00000000h
824h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC1LLPU)	00000000h
828h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC1LDPL)	00000000h
82Ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC1LDPU)	00000000h
830h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC2LLPL)	00000000h
834h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC2LLPU)	00000000h
838h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC2LDPL)	00000000h
83Ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC2LDPU)	00000000h
840h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC3LLPL)	00000000h
844h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC3LLPU)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
848h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC3LDPL)	00000000h
84Ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC3LDPU)	00000000h
850h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC4LLPL)	00000000h
854h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC4LLPU)	00000000h
858h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC4LDPL)	00000000h
85Ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC4LDPU)	00000000h
860h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC5LLPL)	00000000h
864h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC5LLPU)	00000000h
868h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC5LDPL)	00000000h
86Ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC5LDPU)	00000000h
870h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC6LLPL)	00000000h
874h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC6LLPU)	00000000h
878h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC6LDPL)	00000000h
87Ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC6LDPU)	00000000h
880h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC0LLPL)	00000000h
884h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC0LLPU)	00000000h
888h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC0LDPL)	00000000h
88Ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC0LDPU)	00000000h
890h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC1LLPL)	00000000h
894h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC1LLPU)	00000000h
898h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC1LDPL)	00000000h
89Ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC1LDPU)	00000000h
8A0h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC2LLPL)	00000000h
8A4h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC2LLPU)	00000000h
8A8h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC2LDPL)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8ACh	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC2LDPU)	00000000h
8B0h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC3LLPL)	00000000h
8B4h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC3LLPU)	00000000h
8B8h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC3LDPL)	00000000h
8BCh	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC3LDPU)	00000000h
8C0h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC4LLPL)	00000000h
8C4h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC4LLPU)	00000000h
8C8h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC4LDPL)	00000000h
8CCh	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC4LDPU)	00000000h
8D0h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC5LLPL)	00000000h
8D4h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC5LLPU)	00000000h
8D8h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC5LDPL)	00000000h
8DCh	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC5LDPU)	00000000h
8E0h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC6LLPL)	00000000h
8E4h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC6LLPU)	00000000h
8E8h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC6LDPL)	00000000h
8ECh	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC6LDPU)	00000000h
8F0h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC7LLPL)	00000000h
8F4h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC7LLPU)	00000000h
8F8h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC7LDPL)	00000000h
8FCh	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC7LDPU)	00000000h
900h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC8LLPL)	00000000h
904h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC8LLPU)	00000000h
908h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC8LDPL)	00000000h
90Ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC8LDPU)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
910h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC0CTL)	00000000h
914h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC0FMT)	0000h
918h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC0LLPL)	00000000h
91Ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC0LLPU)	00000000h
920h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC1CTL)	00000000h
924h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC1FMT)	0000h
928h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC1LLPL)	00000000h
92Ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC1LLPU)	00000000h
930h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC2CTL)	00000000h
934h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC2FMT)	0000h
938h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC2LLPL)	00000000h
93Ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC2LLPU)	00000000h
940h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC3CTL)	00000000h
944h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC3FMT)	0000h
948h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC3LLPL)	00000000h
94Ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC3LLPU)	00000000h
950h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC4CTL)	00000000h
954h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC4FMT)	0000h
958h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC4LLPL)	00000000h
95Ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC4LLPU)	00000000h
960h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC5CTL)	00000000h
964h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC5FMT)	0000h
968h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC5LLPL)	00000000h
96Ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC5LLPU)	00000000h
970h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC6CTL)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
974h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC6FMT)	0000h
978h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC6LLPL)	00000000h
97Ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC6LLPU)	00000000h
980h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC0CTL)	00000000h
984h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC0FMT)	0000h
988h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC0LLPL)	00000000h
98Ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC0LLPU)	00000000h
990h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC1CTL)	00000000h
994h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC1FMT)	0000h
998h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC1LLPL)	00000000h
99Ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC1LLPU)	00000000h
9A0h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC2CTL)	00000000h
9A4h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC2FMT)	0000h
9A8h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC2LLPL)	00000000h
9ACh	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC2LLPU)	00000000h
9B0h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC3CTL)	00000000h
9B4h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC3FMT)	0000h
9B8h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC3LLPL)	00000000h
9BCh	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC3LLPU)	00000000h
9C0h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC4CTL)	00000000h
9C4h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC4FMT)	0000h
9C8h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC4LLPL)	00000000h
9CCh	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC4LLPU)	00000000h
9D0h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC5CTL)	00000000h
9D4h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC5FMT)	0000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
9D8h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC5LLPL)	00000000h
9DCh	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC5LLPU)	00000000h
9E0h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC6CTL)	00000000h
9E4h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC6FMT)	0000h
9E8h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC6LLPL)	00000000h
9ECh	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC6LLPU)	00000000h
9F0h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC7CTL)	00000000h
9F4h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC7FMT)	0000h
9F8h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC7LLPL)	00000000h
9FCh	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC7LLPU)	00000000h
A00h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC8CTL)	00000000h
A04h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC8FMT)	0000h
A08h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC8LLPL)	00000000h
A0Ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC8LLPU)	00000000h
C00h	4	Multiple Links Capability Header (MLCH)	00020800h
C04h	4	Multiple Links Capability Declaration (MLCD)	00000001h
C40h	4	Link x Capabilities (LCAP0)	00000007h
C44h	4	Link x Control (LCTL0)	00010002h
C48h	4	Link x Output Stream ID Mapping Valid (LOSIDV0)	0000FFFEh
C4Ch	4	Link x SDI Identifier (LSDIID0)	00000003h
C50h	1	Link x Per Stream Output Overhead (LPSOO0)	00h
C52h	1	Link x Per Stream Input Overhead (LPSIO0)	00h
C58h	4	Link x Wall Frame Counter (LWALFC0)	00000000h
C60h	2	Link x Output Payload Capability (LOUTPAY6M0)	000Dh
C62h	2	Link x Output Payload Capability (LOUTPAY12M0)	001Ch
C64h	2	Link x Output Payload Capability (LOUTPAY24M0)	003Ch
C66h	2	Link x Output Payload Capability (LOUTPAY48M0)	0000h
C68h	2	Link x Output Payload Capability (LOUTPAY96M0)	0000h
C6Ah	2	Link x Output Payload Capability (LOUTPAY192M0)	0000h
C70h	2	Link x Input Payload Capability (LINPAY6M0)	0005h
C72h	2	Link x Input Payload Capability (LINPAY12M0)	000Dh
C74h	2	Link x Input Payload Capability (LINPAY24M0)	001Dh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
C76h	2	Link x Input Payload Capability (LINPAY48M0)	0000h
C78h	2	Link x Input Payload Capability (LINPAY96M0)	0000h
C7Ah	2	Link x Input Payload Capability (LINPAY192M0)	0000h
C80h	4	Link x Capabilities (LCAP1)	0000001Fh
C84h	4	Link x Control (LCTL1)	00010004h
C88h	4	Link x Output Stream ID Mapping Valid (LOSIDV1)	0000FFFEh
C8Ch	4	Link x SDI Identifier (LSDIID1)	00000004h
C90h	1	Link x Per Stream Output Overhead (LPSOO1)	00h
C92h	1	Link x Per Stream Input Overhead (LPSIO1)	00h
C98h	4	Link x Wall Frame Counter (LWALFC1)	00000000h
CA0h	2	Link x Output Payload Capability (LOUTPAY6M1)	0003h
CA2h	2	Link x Output Payload Capability (LOUTPAY12M1)	000Bh
CA4h	2	Link x Output Payload Capability (LOUTPAY24M1)	001Ah
CA6h	2	Link x Output Payload Capability (LOUTPAY48M1)	0038h
CA8h	2	Link x Output Payload Capability (LOUTPAY96M1)	0074h
CAAh	2	Link x Output Payload Capability (LOUTPAY192M1)	0000h
CB0h	2	Link x Input Payload Capability (LINPAY6M1)	0000h
CB2h	2	Link x Input Payload Capability (LINPAY12M1)	0000h
CB4h	2	Link x Input Payload Capability (LINPAY24M1)	0000h
CB6h	2	Link x Input Payload Capability (LINPAY48M1)	0000h
CB8h	2	Link x Input Payload Capability (LINPAY96M1)	0000h
CBAh	2	Link x Input Payload Capability (LINPAY192M1)	0000h
1F00h	4	DMA Resume Capability Header (DRSMCH)	00050700h
1F04h	4	DMA Resume Control (DRSMCTL)	00000000h
1F08h	4	DMA Position in Buffer Resume (ISD0DPIBR)	00000000h
1F10h	4	DMA Position in Buffer Resume (ISD1DPIBR)	00000000h
1F18h	4	DMA Position in Buffer Resume (ISD2DPIBR)	00000000h
1F20h	4	DMA Position in Buffer Resume (ISD3DPIBR)	00000000h
1F28h	4	DMA Position in Buffer Resume (ISD4DPIBR)	00000000h
1F30h	4	DMA Position in Buffer Resume (ISD5DPIBR)	00000000h
1F38h	4	DMA Position in Buffer Resume (ISD6DPIBR)	00000000h
1F40h	4	DMA Position in Buffer Resume (OSD0DPIBR)	00000000h
1F48h	4	DMA Position in Buffer Resume (OSD1DPIBR)	00000000h
1F50h	4	DMA Position in Buffer Resume (OSD2DPIBR)	00000000h
1F58h	4	DMA Position in Buffer Resume (OSD3DPIBR)	00000000h
1F60h	4	DMA Position in Buffer Resume (OSD4DPIBR)	00000000h
1F68h	4	DMA Position in Buffer Resume (OSD5DPIBR)	00000000h
1F70h	4	DMA Position in Buffer Resume (OSD6DPIBR)	00000000h
1F78h	4	DMA Position in Buffer Resume (OSD7DPIBR)	00000000h
1F80h	4	DMA Position in Buffer Resume (OSD8DPIBR)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1F88h	4	DMA Position in Buffer Resume (ISD7DPIBR)	00000000h
1F90h	4	DMA Position in Buffer Resume (ISD8DPIBR)	00000000h
1F98h	4	DMA Position in Buffer Resume (ISD9DPIBR)	00000000h
1FA0h	4	DMA Position in Buffer Resume (ISD10DPIBR)	00000000h
1FA8h	4	DMA Position in Buffer Resume (ISD11DPIBR)	00000000h
1FB0h	4	DMA Position in Buffer Resume (ISD12DPIBR)	00000000h
1FB8h	4	DMA Position in Buffer Resume (ISD13DPIBR)	00000000h
1FC0h	4	DMA Position in Buffer Resume (ISD14DPIBR)	00000000h
1FC8h	4	DMA Position in Buffer Resume (OSD9DPIBR)	00000000h
1FD0h	4	DMA Position in Buffer Resume (OSD10DPIBR)	00000000h
1FD8h	4	DMA Position in Buffer Resume (OSD11DPIBR)	00000000h
1FE0h	4	DMA Position in Buffer Resume (OSD12DPIBR)	00000000h
1FE8h	4	DMA Position in Buffer Resume (OSD13DPIBR)	00000000h
1FF0h	4	DMA Position in Buffer Resume (OSD14DPIBR)	00000000h
2030h	4	Wall Clock Alias (WLCLKA)	00000000h
2084h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (ISD0LPIBA)	00000000h
20A4h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (ISD1LPIBA)	00000000h
20C4h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (ISD2LPIBA)	00000000h
20E4h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (ISD3LPIBA)	00000000h
2104h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (ISD4LPIBA)	00000000h
2124h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (ISD5LPIBA)	00000000h
2144h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (ISD6LPIBA)	00000000h
2164h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (OSD0LPIBA)	00000000h
2184h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (OSD1LPIBA)	00000000h
21A4h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (OSD2LPIBA)	00000000h
21C4h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (OSD3LPIBA)	00000000h
21E4h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (OSD4LPIBA)	00000000h
2204h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (OSD5LPIBA)	00000000h
2224h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (OSD6LPIBA)	00000000h
2244h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (OSD7LPIBA)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2264h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (OSD8LPIBA)	00000000h
2284h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (ISD7LPIBA)	00000000h
22A4h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (ISD8LPIBA)	00000000h
22C4h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (ISD9LPIBA)	00000000h
22E4h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (ISD10LPIBA)	00000000h
2304h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (ISD11LPIBA)	00000000h
2324h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (ISD12LPIBA)	00000000h
2344h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (ISD13LPIBA)	00000000h
2364h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (ISD14LPIBA)	00000000h
2384h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (OSD9LPIBA)	00000000h
23A4h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (OSD10LPIBA)	00000000h
23C4h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (OSD11LPIBA)	00000000h
23E4h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (OSD12LPIBA)	00000000h
2404h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (OSD13LPIBA)	00000000h
2424h	4	Input Stream Descriptor 0 Link Position in Buffer Alias (OSD14LPIBA)	00000000h
4A10h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC7LLPL)	00000000h
4A14h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC7LLPU)	00000000h
4A18h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC7LDPL)	00000000h
4A1Ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC7LDPU)	00000000h
4A20h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC8LLPL)	00000000h
4A24h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC8LLPU)	00000000h
4A28h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC8LDPL)	00000000h
4A2Ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC8LDPU)	00000000h
4A30h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC9LLPL)	00000000h
4A34h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC9LLPU)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4A38h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC9LDPL)	00000000h
4A3Ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC9LDPU)	00000000h
4A40h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC10LLPL)	00000000h
4A44h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC10LLPU)	00000000h
4A48h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC10LDPL)	00000000h
4A4Ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC10LDPU)	00000000h
4A50h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC11LLPL)	00000000h
4A54h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC11LLPU)	00000000h
4A58h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC11LDPL)	00000000h
4A5Ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC11LDPU)	00000000h
4A60h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC12LLPL)	00000000h
4A64h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC12LLPU)	00000000h
4A68h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC12LDPL)	00000000h
4A6Ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC12LDPU)	00000000h
4A70h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC13LLPL)	00000000h
4A74h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC13LLPU)	00000000h
4A78h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC13LDPL)	00000000h
4A7Ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC13LDPU)	00000000h
4A80h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC14LLPL)	00000000h
4A84h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC14LLPU)	00000000h
4A88h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC14LDPL)	00000000h
4A8Ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC14LDPU)	00000000h
4A90h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC9LLPL)	00000000h
4A94h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC9LLPU)	00000000h
4A98h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC9LDPL)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4A9Ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC9LDPU)	00000000h
4AA0h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC10LLPL)	00000000h
4AA4h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC10LLPU)	00000000h
4AA8h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC10LDPL)	00000000h
4AACh	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC10LDPU)	00000000h
4AB0h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC11LLPL)	00000000h
4AB4h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC11LLPU)	00000000h
4AB8h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC11LDPL)	00000000h
4ABCh	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC11LDPU)	00000000h
4AC0h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC12LLPL)	00000000h
4AC4h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC12LLPU)	00000000h
4AC8h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC12LDPL)	00000000h
4ACCh	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC12LDPU)	00000000h
4AD0h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC13LLPL)	00000000h
4AD4h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC13LLPU)	00000000h
4AD8h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC13LDPL)	00000000h
4ADCh	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC13LDPU)	00000000h
4AE0h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC14LLPL)	00000000h
4AE4h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC14LLPU)	00000000h
4AE8h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC14LDPL)	00000000h
4AECh	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC14LDPU)	00000000h
4AF0h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC7CTL)	00000000h
4AF4h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC7FMT)	0000h
4AF8h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC7LLPL)	00000000h
4AFCh	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC7LLPU)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4B00h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC8CTL)	00000000h
4B04h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC8FMT)	0000h
4B08h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC8LLPL)	00000000h
4B0Ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC8LLPU)	00000000h
4B10h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC9CTL)	00000000h
4B14h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC9FMT)	0000h
4B18h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC9LLPL)	00000000h
4B1Ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC9LLPU)	00000000h
4B20h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC10CTL)	00000000h
4B24h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC10FMT)	0000h
4B28h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC10LLPL)	00000000h
4B2Ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC10LLPU)	00000000h
4B30h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC11CTL)	00000000h
4B34h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC11FMT)	0000h
4B38h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC11LLPL)	00000000h
4B3Ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC11LLPU)	00000000h
4B40h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC12CTL)	00000000h
4B44h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC12FMT)	0000h
4B48h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC12LLPL)	00000000h
4B4Ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC12LLPU)	00000000h
4B50h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC13CTL)	00000000h
4B54h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC13FMT)	0000h
4B58h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC13LLPL)	00000000h
4B5Ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC13LLPU)	00000000h
4B60h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC14CTL)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4B64h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC14FMT)	0000h
4B68h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC14LLPL)	00000000h
4B6Ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC14LLPU)	00000000h
4B70h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC9CTL)	00000000h
4B74h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC9FMT)	0000h
4B78h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC9LLPL)	00000000h
4B7Ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC9LLPU)	00000000h
4B80h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC10CTL)	00000000h
4B84h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC10FMT)	0000h
4B88h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC10LLPL)	00000000h
4B8Ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC10LLPU)	00000000h
4B90h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC11CTL)	00000000h
4B94h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC11FMT)	0000h
4B98h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC11LLPL)	00000000h
4B9Ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC11LLPU)	00000000h
4BA0h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC12CTL)	00000000h
4BA4h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC12FMT)	0000h
4BA8h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC12LLPL)	00000000h
4BACh	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC12LLPU)	00000000h
4BB0h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC13CTL)	00000000h
4BB4h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC13FMT)	0000h
4BB8h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC13LLPL)	00000000h
4BBCh	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC13LLPU)	00000000h
4BC0h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC14CTL)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4BC4h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC14FMT)	0000h
4BC8h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC14LLPL)	00000000h
4BCCh	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC14LLPU)	00000000h

5.2.1 Global Capabilities (GCAP) - Offset 0h

This register indicates the capabilities of the controller.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 0h	9701h

Bit Range	Default & Access	Field Name (ID): Description
15:12	9h RW/L	**Number of Output Streams Supported (OSS):** 0100b indicates that the Intel HD Audio controller supports four output streams. Reset value is hardcoded to parameter HSTOSC. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
11:8	7h RW/L	**Number of Input Streams Supported (ISS):** 0100b indicates that the Intel HD Audio controller supports four input streams. Reset value is hardcoded to parameter HSTISC. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
7:3	00h RO	**Number of Bidirectional Streams Supported (BSS):** 00000b indicates that the Intel HD Audio controller supports 0 bidirectional streams.
2:1	0h RW/L	**Number of Serial Data Out Signals (NSDO):** 00b indicates that the Intel HD Audio controller supports one Serial Data Output signal. For the case of multiple link segments is supported, this field indicates the number of SDO for link 0. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
0	1h RW/L	**64 Bit Address Supported (ADD64OK):** A 1 indicates that the Intel HD Audio controller supports 64 bit addressing for BDL addresses, data buffer addresses, and command buffer addresses. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD

5.2.2 Minor Version (VMIN) - Offset 2h

This register indicates minor revision number of the High Definition Audio specification.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 2h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/L	**Minor Version (VMIN):** Indicates the Intel HD Audio controller supports minor revision number 00h of the Intel HD Audio specification. **Locked by:** SBPR.FNCFG.BCLD

5.2.3 Major Version (VMAJ) - Offset 3h

This register indicates major revision number of the High Definition Audio specification.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 3h	01h

Bit Range	Default & Access	Field Name (ID): Description
7:0	01h RW/L	**Major Version (VMAJ):** Indicates the Intel HD Audio controller supports major revision number 1 of the Intel HD Audio specification. **Locked by:** SBPR.FNCFG.BCLD

5.2.4 Output Payload Capability (OUTPAY) - Offset 4h

This register indicates the total output payload available on the link.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 4h	003Ch

Bit Range	Default & Access	Field Name (ID): Description
15:0	003Ch RW/L	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. The default link clock speed of 24.000 MHz (the data is double pumped) provides 1000 bits per frame, or 62.5 words in total. 40 bits are used for command and control, leaving 60 words available for data payload. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload ***Note***: In the event that multiple links is supported (GCAP2.LCOUNT) 0), the payload advertised will be the lowest common denominator offered by the default clock frequency on each link. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD

5.2.5 Input Payload Capability (INPAY) - Offset 6h

This register indicates the total input payload available on the link.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 6h	001Dh

Bit Range	Default & Access	Field Name (ID): Description
15:0	001Dh RW/L	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link. This does not include bandwidth used for response. This measurement is in 16-bit word quantities per 48 kHz frame. The default link clock speed of 24.000 MHz provides 500 bits per frame, or 31.25 words in total. 36 bits are used for response, leaving 29 words for data payload. Note that this value does not reflect any bandwidth increase due to support for multiple SDI lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload ***Note***: In the event that multiple links are supported (GCAP2.LCOUNT) 0), the payload advertised will be the lowest common denominator offered by the default clock frequency on each link. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD

5.2.6 Global Control (GCTL) - Offset 8h

CRSTB bit is not affected by controller reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**Accept Unsolicited Response Enable (UNSOL):** If UNSOL is a 1, Unsolicited Responses from the codecs are accepted by the controller and placed into the Response Input Ring Buffer. If UNSOL is a 0, unsolicited response are not accepted, and dropped on the floor.

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW/1S/V	**Flush Control (FCNTRL):** Writing a 1 to this bit initiates a flush. When the flush completion is received by the controller, hardware sets the Flush Status bit and clears this Flush Control bit. Before a flush cycle is initiated, the DMA Position Buffer must be programmed with a valid memory address by software, but the DMA Position Buffer bit 0 need not be set to enable the position reporting mechanism. Also, all streams must be stopped (the associated RUN bit must be 0). When the flush is initiated, the controller will flush pipelines to memory to guarantee that the hardware is ready to transition to a D3 state. Setting this bit is not a critical step in the power state transition if the content of the FIFOs is not critical.
0	0h RW/V	**Controller Reset# (CRSTB):** Writing a 0 to this bit causes the Intel HD Audio controller to be reset. All state machines, FIFO's and non-suspend well memory mapped configuration registers (except ECAP, and not PCI Configuration Registers) in the controller will be reset. The Intel HD Audio link RESET# signal will be asserted and all other link signals will be driven to their "reset" values. After the hardware has completed sequencing into the reset state, it will report a 0 in this bit. Software must read a 0 from this bit to verify that the controller is in reset. Writing a 1 to this bit causes the controller to exit its reset state and deassert the Intel HD Audio link RESET# signal. Software is responsible for setting/clearing this bit such that the minimum Intel HD Audio link RESET# signal assertion pulse width specification is met. When the controller hardware is ready to begin operation, it will report a 1 in this bit. Software must read a 1 from this bit before accessing any controller registers. The CRST# bit defaults to a 0 after hardware reset, therefore software needs to write a 1 to this bit to begin operation. Note that the CORB/RIRB RUN bits and all Stream RUN bits must be verified cleared to zero before CRST# is written to 0 (asserted) in order to assure a clean re-start. When setting or clearing CRST#, software must ensure that minimum link timing requirements (minimum RESET# assertion time, etc.) are met. When CRST# is 0 indicating that the controller is in reset, writes to all Intel HD Audio memory mapped registers are ignored as if the device is not present. The only exception is the Global Control register containing the CRST# bit itself. The Global Control register is write-able as a DWord, Word, or Byte even when CRST# is 0 if the byte enable for the byte containing the CRST# bit (Byte Enable 0) is active. If Byte Enable 0 is not active, writes to the Global Control register will be ignored when CRST# is 0. When CRST# is 0, reads to Intel HD Audio memory mapped registers will return their default value except for registers that are not reset with PLTRST# or on a D3hot to D0 transition.

5.2.7 Wake Enable (WAKEEN) - Offset Ch

This register indicates which bits in the WAKESTS register may cause either a wake event or an interrupt.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2:0	0h RW	**SDIN Wake Enable Flags (WAKEEN):** Bits which control which SDI signal(s) may generate a wake event. A 1 bit in the bit mask indicates that the associated SDIN signal is enabled to generate a wake. These bits are cleared on a power-on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.

5.2.8 Wake Status (WAKESTS) - Offset Eh

This register indicates that a Status Change event has occurred on the link, which usually indicates that either the codec has just come out of reset and is requesting an address, or that a codec is signaling a wake event.

Implementation Notes: Because of the legacy implementations of the WAKESTS bits are physically located in the Resume clock domain and it takes time to clock cross the clearing event resulted from SW writing a 1, it is possible that the SW may still read back 1 after clearing the WAKESTS bits, especially if the Resume clock is tied to a slow clock in the SoC, e.g. RTC clock.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + Eh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2:0	0h RW/1C/V	**SDIN State Change Status Flags (WAKESTS):** Flag bits that indicate which SDI signal(s) received a State Change event. The bits are cleared by writing 1's to them. These bits are cleared on a power-on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.

5.2.9 Global Status (GSTS) - Offset 10h

This register provides global level status of the controller.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 10h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**
1	0h RW/1C/V	**Flush Status (FSTS):** This bit is set to a 1 by the hardware to indicate that the flush cycle initiated when the FCNTRL bit was set has completed. Software must write a 1 to clear this bit before the next time FCNTRL is set.
0	0h RO	**Reserved**

5.2.10 Global Capabilities 2 (GCAP2) - Offset 12h

This register indicates the additional capabilities of the controller.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 12h	0001h

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**
1	0h RW/L	**Dynamic FIFO Limit Change Capability (DFIFOLCC):** Indicates whether the energy efficient audio FIFOLC operation is static or dynamic. 0 = Static. FIFOLC bit only has effect before RUN bit is set for the first time. 1 = Dynamic. FIFOLC bit has effect before RUN bit is set for the first time, as well as after that. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
0	1h RW/V/L	**Energy Efficient Audio Capability (EEAC):** Indicates whether the energy efficient audio with deeper buffering is supported or not. 0 = Not supported. FIFOL register and FIFOLC bit behave as RO. 1 = Supported. FIFOL register and FIFOLC bit behave as RW. Locked when FNCFG.BCLD = 1 or FUSVAL.CPPMD = 1. **Locked by:** SBPR.FNCFG.BCLD

5.2.11 Linked List Capabilities Header (LLCH) - Offset 14h

This register provides the pointer to the first capability structure, if exists.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 14h	0C00h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0C00h RW/L	**First Capability Pointer (PTR):** This field contains the offset to the first capability structure of the linked list capabilities, or 0000h if no linked list capabilities exist. Point to Multiple Links Capability. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD

5.2.12 Output Stream Payload Capability (OUTSTRMPAY) - Offset 18h

This register indicates the maximum number of Words per frame for any single output stream.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 18h	0030h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0030h RO	**Output Stream Payload Capability (OUTSTRMPAY):** Indicates maximum number of words per frame for any single output stream. This measurement is in 16 bit word quantities per 48 kHz frame. 48 Words (96B) are the maximum supported, therefore a value of 30h is reported in this register. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Output Stream Descriptor register. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload

5.2.13 Input Stream Payload Capability (INSTRMPAY) - Offset 1Ah

This register indicates the maximum number of Words per frame for any single input stream.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 1Ah	0018h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0018h RO	**Input Stream Payload Capability (INSTRMPAY):** Indicates maximum number of words per frame for any single input stream. This measurement is in 16 bit word quantities per 48 kHz frame. 24 Words (48B) are the maximum supported, therefore a value of 18h is reported in this register. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Input Stream Descriptor register. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload

5.2.14 Interrupt Control (INTCTL) - Offset 20h

The Interrupt Status and Control register provides a central point for controlling and monitoring interrupt generation. The SIE (Stream Interrupt Enable) register controls the interrupt mask for each individual Input or Output Stream. Setting a 1 in the appropriate bit allows the particular interrupt source to generate a processor interrupt. The SIS (Stream Interrupt Status) register indicates the current interrupt status of each interrupt source. A 1 indicates that an interrupt is being requested. Note that the state of these bits is independent of the SIE bits; even if the corresponding bit is set to a 0 in the Stream Interrupt Enable register to disable processor interrupt generation, the Status bit may still be set to indicate that stream is requesting service. This can be used by polling software to determine which Streams need attention without incurring system interrupts. The CIE (Controller Interrupt Enable) and CIS (Controller Interrupt Status) control and indicate the status of the general controller interrupt. General controller interrupt sources are to a Response Interrupt, a Response Buffer Overrun, and State Change events. Note that the CIS is independent of the CIE bit; even if the CIE bit is set to a 0 to disable processor interrupt generation, the CIS bit may still be set to indicate that stream is requesting service.

The GIE (Global Interrupt Enable) and GIS (Global Interrupt Status) control and indicate the status of all hardware interrupt sources in the Intel HD Audio controller. If GIS bit is a 1, a processor interrupt is currently being requested. If GIE is a 1, a processor interrupt may be requested; if GIE is a 0, then no processor interrupt may be requested. Note that the GIS is independent of the GIE bit; even if the GIE bit is set to a 0 to disable processor interrupt generation, the GIS bit may still be set to indicate that stream is requesting service.

GIE and CIE bits are not affected by controller reset. The number of SIE bits in this register is depending on the total number of streams DMA implemented, represented as x in the register table. The x value is determined by the sum of parameter HSTISC and HSTOSC.

For SPT implementation, x = 16.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Global Interrupt Enable (GIE):** Global bit to enable device interrupt generation. When set to 1 the Intel HD Audio function is enabled to generate an interrupt. This control is in addition to any bits in the bus specific address space, such as the Interrupt Enable bit in the PCI Configuration Space.
30	0h RW	**Controller Interrupt Enable (CIE):** Enables the general interrupt for controller functions. When set to 1 (and GIE is enabled), the controller generates an interrupt when the CIS bit gets set.
29:16	0h RO	**Reserved**
15:0	0000h RW	**Stream Interrupt Enable (SIE):** When set to 1 the individual Streams are enabled to generate an interrupt when the corresponding stream status bits get set. A stream interrupt will be caused as a result of a buffer with IOC=1 in the BDL entry being completed, or as a result of a FIFO error (under run or overrun) occurring. Control over the generation of each of these sources is in the associated Stream Descriptor. The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set.

5.2.15 Interrupt Status (INTSTS) - Offset 24h

GIS and CIS bits are not affected by controller reset.

The number of SIS bits in this register is depending on the total number of streams

DMA implemented, represented as x in the register table.

The x value is determined by the sum of parameter HSTISC and HSTOSC.

For SPT implementation, x = 16.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 24h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Global Interrupt Status (GIS):** This bit is an OR of all of the interrupt status bits in this register and PPSTS register
30	0h RW/V	**Controller Interrupt Status (CIS):** Status of general controller interrupt. A 1 indicates that an interrupt condition occurred due to a Response Interrupt, a Response Buffer Overrun Interrupt, CORB Memory Error Interrupt, Error Present Interrupt, or a SDIN State Change event. The exact cause can be determined by interrogating other registers. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of the stated interrupt status bits for this register.
29:16	0h RO	**Reserved**
15:0	0000h RW/V	**Stream Interrupt Status (SIS):** A 1 indicates that an interrupt condition occurred on the corresponding Stream. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of an individual stream s interrupt status bits. The streams are numbered and the SIS bits assigned sequentially, based on their order in the register set.

5.2.16 Wall Clock Counter (WALCLK) - Offset 30h

The 32 bit monotonic counter provides a 'wall clock' that can be used by system software to synchronize independent audio controllers. The counter must be implemented.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Wall Clock Counter (WALCLK):** 32 bit counter that is incremented on each link BCLK period and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to zero with a period of approximately 179 seconds. This counter is enabled while the BCLK bit is set to 1. Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset. With the introduction of multiple link segments for the Intel HD Audio controller, and the capability of running each link segment at different clock speed, the BCLK definition for this counter is fixed at 24 MHz equivalent rate always, independent of the physical link clock speed, and reports the link 0 wall clock value.

5.2.17 Stream Synchronization (SSYNC) - Offset 38h

To synchronize two or more streams the corresponding SSYNC bits for the streams to be synchronized should be set to 1 before the 'RUN' bit for each stream is set.

The RUN bit for the corresponding stream must be set to 1 (and FIFORDY=1) prior to that stream's SSYNC bit being written to 0. To start multiple streams synchronously, the stream sync bits for those streams should be written to 0 at the same time. For all SSYNC bits on output engines that transition from 1 to 0 on the same write, the formatter will deliver a sample over the link in the same 48kHz frame. For all SSYNC bits on input engines that transition from 1 to 0 on the same write, the formatter will take stream data off the link and place it in the FIFO.

If synchronization is not desired, the stream synchronization bits may be left 0, and the stream will simply begin running normally when the stream's 'RUN' bit is set. In addition to platform reset, FLR, and controller reset, the register is also reset by stream reset. The number of SSYNC bits in this register is depending on the total number of streams DMA implemented, represented as x in the register table. The x value is determined by the sum of parameter HSTISC and HSTOSC. For SPT implementation, x = 16.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Stream Synchronization Bits (SSYNC):** The Stream Synchronization bits, when set to 1, block data from being sent on or received from the link. Each bit controls the associated Stream Descriptor, bit 0 corresponds to the first Stream Descriptor, etc. To synchronously start a set of DMA engines, the bits in the SSYNC register are first set to a 1. The RUN bits for the associated Stream Descriptors are then set to a 1 to start the DMA engines. When all streams are ready (FIFORDY=1), the associated SSYNC bits can all be set to 0 at the same time, and transmission or reception of bits to or from the link will begin together at the start of the next full link frame. To synchronously stop streams, first the bits are set in the SSYNC register, and then the individual RUN bits in the Stream Descriptors are cleared by software. The streams are numbered and the SSYNC bits assigned sequentially, based on their order in the register set.

5.2.18 CORB Lower Base Address (CORBLBASE) - Offset 40h

This register specifies the address (lower 32 bits) of the Command Output Ring Buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**CORB Lower Base Address (CORBLBASE):** Lower address of the Command Output Ring Buffer, allowing the CORB Base Address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	0h RO	**Reserved**

5.2.19 CORB Upper Base Address (CORBUBASE) - Offset 44h

This register specifies the address (upper 32 bits) of the Command Output Ring Buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 44h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**CORB Upper Base Address (CORBUBASE):** Upper 32 bits of address of the Command Output Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. Locked when GCAP.ADD64OK = 0. **Locked by:** GCAP.ADD64OK

5.2.20 CORB Write Pointer (CORBWP) - Offset 48h

This register specifies the write pointer of the Command Output Ring Buffer.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 48h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:0	00h RW	**CORB Write Pointer (CORBWP):** Software writes the last valid CORB entry offset into this field in Dword granularity. The DMA engine fetches commands from the CORB until the Read Pointer matches the Write Pointer. Supports 256 CORB entries (256 x 4B=1KB). This field may be written while the DMA engine is running.

5.2.21 CORB Read Pointer (CORBRP) - Offset 4Ah

This register reports the read pointer of the Command Output Ring Buffer.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 4Ah	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/V	**CORB Read Pointer Reset (CORBRPRST):** Software writes a 1 to this bit to reset the CORB Read Pointer to 0 and clear any residual pre-fetched commands in the CORB hardware buffer within the Intel Audio controller. The hardware will physically update this bit to 1 when the CORB Pointer reset is complete. Software must read a 1 to verify that the reset completed correctly. Software must clear this bit back to 0 and read back the 0 to verify that the clear completed correctly. The CORB DMA engine must be stopped prior to resetting the Read Pointer or else DMA transfer may be corrupted.
14:8	0h RO	**Reserved**
7:0	00h RO/V	**CORB Read Pointer (CORBRP):** Software reads this field to determine how many commands it can write to the CORB without over-running. The value read indicates the CORB Read Pointer offset in Dword granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be over-written by software. Supports 256 CORB entries (256 x 4B=1KB). This field may be read while the DMA engine is running.

5.2.22 CORB Control (CORBCTL) - Offset 4Ch

This register provides the control of the Command Output Ring Buffer.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 4Ch	00h

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW/V	**Enable CORB DMA Engine (CORBRUN):** 0 = DMA Stop 1 = DMA Run After SW writes a 0 to this bit, the HW may not stop immediately. The hardware will physically update the bit to a 0 when the DMA engine is truly stopped. SW must read a 0 from this bit to verify that the DMA is truly stopped.
0	0h RW	**CORB Memory Error Interrupt Enable (CMEIE):** If this bit is set (and GIE and CIE are enabled), the controller will generate an interrupt if the MEI status bit is set.

5.2.23 CORB Status (CORBSTS) - Offset 4Dh

This register provides the status of the Command Output Ring Buffer.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 4Dh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	**Reserved**
0	0h RW/1C/V	**CORB Memory Error Indication (CMEI):** If this status bit is set, the controller has detected an error in the pathway between the controller and memory. This may be an ECC bit error or any other type of detectable data error which renders the command data fetched invalid. Software can clear this bit by writing a 1 to it. However, this type of error leaves the audio subsystem in an unviable state and typically requires CRST#.

5.2.24 CORB Size (CORBSIZE) - Offset 4Eh

This register declares the size of the Command Output Ring Buffer.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 4Eh	42h

Bit Range	Default & Access	Field Name (ID): Description
7:4	4h RO	**CORB Size Capability (CORBSZCAP):** 0100b indicates that the ICH9 only supports a CORB size of 256 CORB entries (1024B).
3:2	0h RO	**Reserved**
1:0	2h RO	**CORB Size (CORBSIZE):** Hardwired to 10b which sets the CORB size to 256 entries (1024B).

5.2.25 RIRB Lower Base Address (RIRBLBASE) - Offset 50h

This register specifies the address (lower 32 bits) of the Response Input Ring Buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**RIRB Lower Base Address (RIRBLBASE):** Lower address of the Response Input Ring Buffer, allowing the RIRB Base Address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	0h RO	**Reserved**

5.2.26 RIRB Upper Base Address (RIRBUBASE) - Offset 54h

This register specifies the address (upper 32 bits) of the Response Input Ring Buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 54h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**RIRB Upper Base Address (RIRBUBASE):** Upper 32 bits of address of the Command Output Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0. **Locked by:** GCAP.ADD64OK

5.2.27 RIRB Write Pointer (RIRBWP) - Offset 58h

This register reports the write pointer of the Response Input Ring Buffer.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 58h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h WO	**RIRB Write Pointer Reset (RIRBWPRST):** Software writes a 1 to this bit to reset the RIRB Write Pointer to 0's. The RIRB DMA engine must be stopped prior to resetting the Write Pointer or else DMA transfer may be corrupted. This bit will always be read as 0.
14:8	0h RO	**Reserved**
7:0	00h RO/V	**RIRB Write Pointer (RIRBWP):** Indicates the last valid RIRB entry written by the DMA controller. Software reads this field to determine how many responses it can read from the RIRB. The value read indicates the RIRB Write Pointer offset in 2 Dword RIRB entry units (since each RIRB entry is 2 Dwords long). Supports up to 256 RIRB entries (256 x 8B=2KB). This field may be read while the DMA engine is running.

5.2.28 Response Interrupt Count (RINTCNT) - Offset 5Ah

This register specifies the threshold of Response Input Ring Buffer that triggers an interrupt.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 5Ah	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:0	00h RW	**N Response Interrupt Count (RINTCNT):** 0000_0001b = 1 Response sent to RIRB ... 1111_1111b = 255 Responses sent to RIRB 0000_0000b = 256 Responses sent to RIRB The DMA engine should be stopped when changing this field or else an interrupt maybe lost. Note that each Response occupies 2 Dwords in the RIRB. This is compared to the total number of responses that have been returned, as opposed to the number of frames in which there were responses. If more than one codec responds in one frame, then the count is increased by the number of responses received in the frame.

5.2.29 RIRB Control (RIRBCTL) - Offset 5Ch

This register provides the control of the Response Input Ring Buffer.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 5Ch	00h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved**
2	0h RW	**Response Overrun Interrupt Control (RIRBOIC):** If this bit is set (and GIE and CIE are enabled), the hardware will generate an interrupt when the Response Overrun Interrupt Status bit is set.
1	0h RW/V	**RIRB DMA Enable (RIRBRUN):** 0 = DMA Stop 1 = DMA Run After SW writes a 0 to this bit, the HW may not stop immediately. The hardware will physically update the bit to a 0 when the DMA engine is truly stopped. SW must read a 0 from this bit to verify that the DMA is truly stopped.
0	0h RW	**Response Interrupt Control (RINTCTL):** 0 = Disable Interrupt 1 = Generate an interrupt (if GIE and CIE are enabled) after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI_x inputs (whichever occurs first). The N counter is reset when the interrupt is generated.

5.2.30 RIRB Status (RIRBSTS) - Offset 5Dh

This register provides the status of the Response Input Ring Buffer.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 5Dh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved**
2	0h RW/1C/V	**Response Overrun Interrupt Status (RIRBOIS):** Hardware sets this bit to a 1 when the RIRB DMA engine is not able to write the incoming responses to memory before additional incoming responses overrun the internal FIFO. When the overrun occurs, the hardware will drop the responses which overrun the buffer. An interrupt may be generated if the Response Overrun Interrupt Control bit is set. Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this flag by writing a 1 to this bit.
1	0h RO	**Reserved**
0	0h RW/1C/V	**Response Interrupt (RINTFL):** Hardware sets this bit to a 1 when an interrupt has been generated after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI(x) inputs (whichever occurs first). Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this flag by writing a 1 to this bit.

5.2.31 RIRB Size (RIRBSIZE) - Offset 5Eh

This register declares the size of the Response Input Ring Buffer.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 5Eh	42h

Bit Range	Default & Access	Field Name (ID): Description
7:4	4h RO	**RIRB Size Capability (RIRBSZCAP):** 0100b indicates that the PCH only supports a RIRB size of 256 RIRB entries (2048B).
3:2	0h RO	**Reserved**
1:0	2h RO	**RIRB Size (RIRBSIZE):** Hardwired to 10b which sets the RIRB size to 256 entries (2048B).

5.2.32 Immediate Command (IC) - Offset 60h

This register provides the control of the immediate command.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Immediate Command (IC):** The command to be sent to the codec via the Immediate Command mechanism is written to this register. The command stored in this register is sent out over the link during the next available frame after a 1 is written to the ICB bit.

5.2.33 Immediate Response (IR) - Offset 64h

This register reports the response received for the immediate command.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Immediate Response (IR):** This register contains the response received from a codec resulting from a command sent via the Immediate Command mechanism. If multiple codecs responded in the same frame, there is no guarantee as to which response will be latched. Therefore broadcast-type commands must not be issued via the Immediate Command mechanism.

5.2.34 Immediate Command Status (ICS) - Offset 68h

This register provides the status of the immediate command.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 68h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**
1	0h RW/1C/V	**Immediate Result Valid (IRV):** This bit is set to a 1 by hardware when a new response is latched into the IR register. This is a status flag indicating that software may read the response from the Immediate Response register. Software must clear this bit (by writing a one to it) before issuing a new command so that the software may determine when a new response has arrived.
0	0h RW/V	**Immediate Command Busy (ICB):** When this bit as read as a 0 it indicates that a new command may be issued using the Immediate Command mechanism. When this bit transitions from a 0 to a 1 (via software writing a 1), the controller issues the command currently stored in the Immediate Command register to the codec over the link. When the corresponding response is latched into the Immediate Response register, the controller hardware sets the IRV flag and clears the ICB bit back to 0. SW may write this bit to a 0 if the bit fails to return to 0 after a reasonable timeout period. Note that an Immediate Command must not be issued while the CORB/RIRB mechanism is operating, otherwise the responses conflict. This must be enforced by software.

5.2.35 DMA Position Lower Base Address (DPLBASE) - Offset 70h

This register specifies the base address (lower 32 bits) of DMA Position Buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**DMA Position Lower Base Address (DPLBASE):** Lower 32 bits of the DMA Position Buffer Base Address. This register field must not be written when any DMA engine is running or the DMA transfer may be corrupted. This same address is used by the Flush Control, and must be programmed with a valid value before the FLCNRTL bit is set.
6:1	0h RO	**Reserved**
0	0h RW	**DMA Position Buffer Enable (DPBE):** When this bit is set to a '1', the controller will write the DMA positions of each of the DMA engines to the buffer in main memory periodically (typically once/ frame). Software can use this value to know what data in memory is valid data. The controller must guarantee that the values in the DMA Position Buffer that the software can read represent positions in the stream for which valid data exists in the Stream's DMA buffer. This has particular relevance in systems which support isochronous transfer, the stream positions in the software-visible memory buffer must represent stream data which has reached the Global Observation point.

5.2.36 DMA Position Upper Base Address (DPUBASE) - Offset 74h

This register specifies the base address (upper 32 bits) of DMA Position Buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 74h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**DMA Position Upper Base Address (DPUBASE):** Upper 32 bits of address of the DMA Position Buffer Base Address. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. Locked when GCAP.ADD64OK = 0. **Locked by:** GCAP.ADD64OK

5.2.37 Input/Output Stream Descriptor x Control (ISD0CTLB0) - Offset 80h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 80h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0. If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set). If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set). **Locked by:** SBPR.FNCFG.BCLD
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.38 Input/Output Stream Descriptor x Status (ISD0STS) - Offset 83h

This register provides the status of the stream DMA.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 83h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved**

5.2.39 Input/Output Stream Descriptor x Link Position in Buffer (ISD0LPIB) - Offset 84h

This register reports the link position in buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.40 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD0CBL) - Offset 88h

This register specifies the cyclic buffer size.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

5.2.41 Input/Output Stream Descriptor x Last Valid Index (ISD0LVI) - Offset 8Ch

This register specifies the last valid buffer descriptor index.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 8Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:0	00h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'

5.2.42 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD0FIFOW) - Offset 8Eh

This register reports the threshold of the FIFO that triggers an access to cyclic buffer.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 8Eh	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2:0	4h RO/V	**FIFOW:** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The PCH HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description 000-011 Reserved 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

5.2.43 Input/Output Stream Descriptor x FIFO Size (ISD0FIFOS) - Offset 90h

This register reports the FIFO size of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 90h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O) SDxFMT register, the min frame of buffering setting in EM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O) SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum values could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

5.2.44 Input/Output Stream Descriptor x Format (ISD0FMT) - Offset 92h

This register specifies the audio format of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 92h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8bit containers on 16bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.45 Input/Output Stream Descriptor x FIFO Limit (ISD0FIFOL) - Offset 94h

This register controls the effective FIFO size for energy efficient audio operation.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 94h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW/L	**GNL:** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. 0 = 125 us 1 = 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC
13:0	0000h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time.0 = Disabled (FIFOS is the limit)0001h 3FFFh = 1 16383 units. When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC

5.2.46 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD0BDLPLBA) - Offset 98h

This register specifies the base address (lower 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:0	0h RO	**Reserved**

5.2.47 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD0BDLPUBA) - Offset 9Ch

This register specifies the base address (upper 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0. **Locked by:** GCAP.ADD64OK

5.2.48 Input/Output Stream Descriptor x Control (ISD1CTLB0) - Offset A0h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + A0h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0.If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set).If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after he first time RUN bit is set). **Locked by:** SBPR.FNCFG.BCLD
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or under run for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will beset, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the streams registers. The RUN bit must be cleared before SRST is asserted.

5.2.49 Input/Output Stream Descriptor x Status (ISD1STS) - Offset A3h

This register provides the status of the stream DMA.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + A3h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved**

5.2.50 Input/Output Stream Descriptor x Link Position in Buffer (ISD1LPIB) - Offset A4h

This register reports the link position in buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.51 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD1CBL) - Offset A8h

This register specifies the cyclic buffer size.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is'0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

5.2.52 Input/Output Stream Descriptor x Last Valid Index (ISD1LVI) - Offset ACh

This register specifies the last valid buffer descriptor index.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + ACh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:0	00h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'

5.2.53 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD1FIFOW) - Offset AEh

This register reports the threshold of the FIFO that triggers an access to cyclic buffer.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + AEh	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2:0	4h RO/V	**FIFOW:** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The PCH HD Audio controller hardwires the FIFO Watermark, either 32B or 64Bbased on the following. Bit(2:0) Description 000-011 Reserved 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

5.2.54 Input/Output Stream Descriptor x FIFO Size (ISD1FIFOS) - Offset B0h

This register reports the FIFO size of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + B0h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O) SDxFMT register, the min frame of buffering setting inEM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O) SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum values could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

5.2.55 Input/Output Stream Descriptor x Format (ISD1FMT) - Offset B2h

This register specifies the audio format of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + B2h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8bit containers on 16bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.56 Input/Output Stream Descriptor x FIFO Limit (ISD1FIFOL) - Offset B4h

This register controls the effective FIFO size for energy efficient audio operation.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + B4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW/L	**GNL:** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. 0 = 125 us 1 = 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC
13:0	0000h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time.0 = Disabled (FIFOS is the limit)0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC

5.2.57 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD1BDLPLBA) - Offset B8h

This register specifies the base address (lower 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:0	0h RO	**Reserved**

5.2.58 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD1BDLPUBA) - Offset BCh

This register specifies the base address (upper 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0. **Locked by:** GCAP.ADD64OK

5.2.59 Input/Output Stream Descriptor x Control (ISD2CTLB0) - Offset C0h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + C0h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0.If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set).If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set). **Locked by:** SBPR.FNCFG.BCLD
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or under run for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will beset, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the streams registers. The RUN bit must be cleared before SRST is asserted.

5.2.60 Input/Output Stream Descriptor x Status (ISD2STS) - Offset C3h

This register provides the status of the stream DMA.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + C3h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on the link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved**

5.2.61 Input/Output Stream Descriptor x Link Position in Buffer (ISD2LPIB) - Offset C4h

This register reports the link position in buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.62 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD2CBL) - Offset C8h

This register specifies the cyclic buffer size.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is'0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

5.2.63 Input/Output Stream Descriptor x Last Valid Index (ISD2LVI) - Offset CCh

This register specifies the last valid buffer descriptor index.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + CCh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:0	00h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'

5.2.64 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD2FIFOW) - Offset CEh

This register reports the threshold of the FIFO that triggers an access to cyclic buffer.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + CEh	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2:0	4h RO/V	**FIFOW:** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The PCH HD Audio controller hardwires the FIFO Watermark, either 32B or 64Bbased on the following. Bit(2:0) Description 000-011 Reserved 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

5.2.65 Input/Output Stream Descriptor x FIFO Size (ISD2FIFOS) - Offset D0h

This register reports the FIFO size of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + D0h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O) SDxFMT register, the min frame of buffering setting inEM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O) SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum values could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

5.2.66 Input/Output Stream Descriptor x Format (ISD2FMT) - Offset D2h

This register specifies the audio format of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + D2h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8bit containers on 16bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.67 Input/Output Stream Descriptor x FIFO Limit (ISD2FIFOL) - Offset D4h

This register controls the effective FIFO size for energy efficient audio operation.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + D4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW/L	**GNL:** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. 0 = 125 us 1 = 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC
13:0	0000h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time.0 = Disabled (FIFOS is the limit)0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC

5.2.68 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD2BDLPLBA) - Offset D8h

This register specifies the base address (lower 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:0	0h RO	**Reserved**

5.2.69 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD2BDLPUBA) - Offset DCh

This register specifies the base address (upper 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0. **Locked by:** GCAP.ADD64OK

5.2.70 Input/Output Stream Descriptor x Control (ISD3CTLB0) - Offset E0h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + E0h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0.If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set).If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set). **Locked by:** SBPR.FNCFG.BCLD
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or under run for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will beset, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit.Software must read a 0 from this bit before accessing any of the streams registers. The RUN bit must be cleared before SRST is asserted.

5.2.71 Input/Output Stream Descriptor x Status (ISD3STS) - Offset E3h

This register provides the status of the stream DMA.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + E3h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved**

5.2.72 Input/Output Stream Descriptor x Link Position in Buffer (ISD3LPIB) - Offset E4h

This register reports the link position in buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.73 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD3CBL) - Offset E8h

This register specifies the cyclic buffer size.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is'0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

5.2.74 Input/Output Stream Descriptor x Last Valid Index (ISD3LVI) - Offset ECh

This register specifies the last valid buffer descriptor index.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + ECh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:0	00h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0”.

5.2.75 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD3FIFOW) - Offset EEh

This register reports the threshold of the FIFO that triggers an access to cyclic buffer.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + EEh	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2:0	4h RO/V	**FIFOW:** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The PCH HD Audio controller hardwires the FIFO Watermark, either 32B or 64Bbased on the following. Bit(2:0) Description 000-011 Reserved 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

5.2.76 Input/Output Stream Descriptor x FIFO Size (ISD3FIFOS) - Offset F0h

This register reports the FIFO size of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + F0h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O) SDxFMT register, the min frame of buffering setting inEM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O) SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In his case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum values could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

5.2.77 Input/Output Stream Descriptor x Format (ISD3FMT) - Offset F2h

This register specifies the audio format of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + F2h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8bit containers on 16bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.78 Input/Output Stream Descriptor x FIFO Limit (ISD3FIFOL) - Offset F4h

This register controls the effective FIFO size for energy efficient audio operation.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + F4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW/L	**GNL:** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. 0 = 125 us 1 = 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC
13:0	0000h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time.0 = Disabled (FIFOS is the limit)0001h 3FFFh = 1 16383 units. When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC

5.2.79 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD3BDLPLBA) - Offset F8h

This register specifies the base address (lower 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:0	0h RO	**Reserved**

5.2.80 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD3BDLPUBA) - Offset FCh

This register specifies the base address (upper 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + FCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0. **Locked by:** GCAP.ADD64OK

5.2.81 Input/Output Stream Descriptor x Control (ISD4CTLB0) - Offset 100h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 100h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0.If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set).If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set). **Locked by:** SBPR.FNCFG.BCLD
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will beset, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the streams registers. The RUN bit must be cleared before SRST is asserted.

5.2.82 Input/Output Stream Descriptor x Status (ISD4STS) - Offset 103h

This register provides the status of the stream DMA.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 103h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset.Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on the link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved**

5.2.83 Input/Output Stream Descriptor x Link Position in Buffer (ISD4LPIB) - Offset 104h

This register reports the link position in buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 104h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.84 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD4CBL) - Offset 108h

This register specifies the cyclic buffer size.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 108h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is'0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

5.2.85 Input/Output Stream Descriptor x Last Valid Index (ISD4LVI) - Offset 10Ch

This register specifies the last valid buffer descriptor index.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 10Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:0	00h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'

5.2.86 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD4FIFOW) - Offset 10Eh

This register reports the threshold of the FIFO that triggers an access to cyclic buffer.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 10Eh	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2:0	4h RO/V	**FIFOW:** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The PCH HD Audio controller hardwires the FIFO Watermark, either 32B or 64Bbased on the following. Bit(2:0) Description 000-011 Reserved 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

5.2.87 Input/Output Stream Descriptor x FIFO Size (ISD4FIFOS) - Offset 110h

This register reports the FIFO size of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 110h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O) SDxFMT register, the min frame of buffering setting inEM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O) SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum values could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

5.2.88 Input/Output Stream Descriptor x Format (ISD4FMT) - Offset 112h

This register specifies the audio format of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 112h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8bit containers on 16bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.89 Input/Output Stream Descriptor x FIFO Limit (ISD4FIFOL) - Offset 114h

This register controls the effective FIFO size for energy efficient audio operation.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 114h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW/L	**GNL:** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. 0 = 125 us 1 = 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC
13:0	0000h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time.0 = Disabled (FIFOS is the limit)0001h 3FFFh = 1 16383 units. When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC

5.2.90 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD4BDLPLBA) - Offset 118h

This register specifies the base address (lower 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 118h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:0	0h RO	**Reserved**

5.2.91 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD4BDLPUBA) - Offset 11Ch

This register specifies the base address (upper 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 11Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0. **Locked by:** GCAP.ADD64OK

5.2.92 Input/Output Stream Descriptor x Control (ISD5CTLB0) - Offset 120h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 120h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0.If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set).If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set). **Locked by:** SBPR.FNCFG.BCLD
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or under-run for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will beset, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the streams registers. The RUN bit must be cleared before SRST is asserted.

5.2.93 Input/Output Stream Descriptor x Status (ISD5STS) - Offset 123h

This register provides the status of the stream DMA.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 123h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on the link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved**

5.2.94 Input/Output Stream Descriptor x Link Position in Buffer (ISD5LPIB) - Offset 124h

This register reports the link position in buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 124h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.95 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD5CBL) - Offset 128h

This register specifies the cyclic buffer size.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 128h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is'0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

5.2.96 Input/Output Stream Descriptor x Last Valid Index (ISD5LVI) - Offset 12Ch

This register specifies the last valid buffer descriptor index.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 12Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:0	00h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'

5.2.97 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD5FIFOW) - Offset 12Eh

This register reports the threshold of the FIFO that triggers an access to cyclic buffer.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 12Eh	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2:0	4h RO/V	**FIFOW:** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The PCH HD Audio controller hardwires the FIFO Watermark, either 32B or 64Bbased on the following. Bit(2:0)Description000-011 Reserved 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

5.2.98 Input/Output Stream Descriptor x FIFO Size (ISD5FIFOS) - Offset 130h

This register reports the FIFO size of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 130h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O) SDxFMT register, the min frame of buffering setting inEM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O) SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum values could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

5.2.99 Input/Output Stream Descriptor x Format (ISD5FMT) - Offset 132h

This register specifies the audio format of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 132h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8bit containers on 16bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.100 Input/Output Stream Descriptor x FIFO Limit (ISD5FIFOL) - Offset 134h

This register controls the effective FIFO size for energy efficient audio operation.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 134h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW/L	**GNL:** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. 0 = 125 us 1 = 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC
13:0	0000h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time.0 = Disabled (FIFOS is the limit)0001h 3FFFh = 1 16383 units. When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC

5.2.101 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD5BDLPLBA) - Offset 138h

This register specifies the base address (lower 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 138h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:0	0h RO	**Reserved**

5.2.102 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD5BDLPUBA) - Offset 13Ch

This register specifies the base address (upper 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 13Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0. **Locked by:** GCAP.ADD64OK

5.2.103 Input/Output Stream Descriptor x Control (ISD6CTLB0) - Offset 140h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 140h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0.If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set).If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set). **Locked by:** SBPR.FNCFG.BCLD
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will beset, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the streams registers. The RUN bit must be cleared before SRST is asserted.

5.2.104 Input/Output Stream Descriptor x Status (ISD6STS) - Offset 143h

This register provides the status of the stream DMA.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 143h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on the link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved**

5.2.105 Input/Output Stream Descriptor x Link Position in Buffer (ISD6LPIB) - Offset 144h

This register reports the link position in buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 144h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.106 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD6CBL) - Offset 148h

This register specifies the cyclic buffer size.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 148h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is'0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

5.2.107 Input/Output Stream Descriptor x Last Valid Index (ISD6LVI) - Offset 14Ch

This register specifies the last valid buffer descriptor index.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 14Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:0	00h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'

5.2.108 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD6FIFOW) - Offset 14Eh

This register reports the threshold of the FIFO that triggers an access to cyclic buffer.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 14Eh	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2:0	4h RO/V	**FIFOW:** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The PCH HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0)Description000-011 Reserved 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

5.2.109 Input/Output Stream Descriptor x FIFO Size (ISD6FIFOS) - Offset 150h

This register reports the FIFO size of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 150h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O) SDxFMT register, the min frame of buffering setting inEM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O) SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum values could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

5.2.110 Input/Output Stream Descriptor x Format (ISD6FMT) - Offset 152h

This register specifies the audio format of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 152h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8bit containers on 16bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.111 Input/Output Stream Descriptor x FIFO Limit (ISD6FIFOL) - Offset 154h

This register controls the effective FIFO size for energy efficient audio operation.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 154h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW/L	**GNL:** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. 0 = 125 us 1 = 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC
13:0	0000h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time.0 = Disabled (FIFOS is the limit)0001h 3FFFh = 1 16383 units. When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC

5.2.112 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD6BDLPLBA) - Offset 158h

This register specifies the base address (lower 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 158h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:0	0h RO	**Reserved**

5.2.113 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD6BDLPUBA) - Offset 15Ch

This register specifies the base address (upper 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 15Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0. **Locked by:** GCAP.ADD64OK

5.2.114 Input/Output Stream Descriptor x Control (OSD0CTLB0) - Offset 160h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 160h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0.If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set).If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set). **Locked by:** SBPR.FNCFG.BCLD
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will beset, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the streams registers. The RUN bit must be cleared before SRST is asserted.

5.2.115 Input/Output Stream Descriptor x Status (OSD0STS) - Offset 163h

This register provides the status of the stream DMA.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 163h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on the link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved**

5.2.116 Input/Output Stream Descriptor x Link Position in Buffer (OSD0LPIB) - Offset 164h

This register reports the link position in buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 164h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.117 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD0CBL) - Offset 168h

This register specifies the cyclic buffer size.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 168h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is'0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

5.2.118 Input/Output Stream Descriptor x Last Valid Index (OSD0LVI) - Offset 16Ch

This register specifies the last valid buffer descriptor index.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 16Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:0	00h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'

5.2.119 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD0FIFOW) - Offset 16Eh

This register reports the threshold of the FIFO that triggers an access to cyclic buffer.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 16Eh	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2:0	4h RO/V	**FIFOW:** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The PCH HD Audio controller hardwires the FIFO Watermark, either 32B or 64Bbased on the following. Bit(2:0) Description 000-011 Reserved 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

5.2.120 Input/Output Stream Descriptor x FIFO Size (OSD0FIFOS) - Offset 170h

This register reports the FIFO size of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 170h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O) SDxFMT register, the min frame of buffering setting inEM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O) SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum values could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

5.2.121 Input/Output Stream Descriptor x Format (OSD0FMT) - Offset 172h

This register specifies the audio format of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 172h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8bit containers on 16bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.122 Input/Output Stream Descriptor x FIFO Limit (OSD0FIFOL) - Offset 174h

This register controls the effective FIFO size for energy efficient audio operation.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 174h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW/L	**GNL:** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. 0 = 125 us 1 = 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC
13:0	0000h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time.0 = Disabled (FIFOS is the limit)0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC

5.2.123 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD0BDLPLBA) - Offset 178h

This register specifies the base address (lower 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 178h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:0	0h RO	**Reserved**

5.2.124 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD0BDLPUBA) - Offset 17Ch

This register specifies the base address (upper 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 17Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0. **Locked by:** GCAP.ADD64OK

5.2.125 Input/Output Stream Descriptor x Control (OSD1CTLB0) - Offset 180h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 180h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0.If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set).If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set). **Locked by:** SBPR.FNCFG.BCLD
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will beset, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the streams registers. The RUN bit must be cleared before SRST is asserted.

5.2.126 Input/Output Stream Descriptor x Status (OSD1STS) - Offset 183h

This register provides the status of the stream DMA.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 183h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on the link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved**

5.2.127 Input/Output Stream Descriptor x Link Position in Buffer (OSD1LPIB) - Offset 184h

This register reports the link position in buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 184h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.128 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD1CBL) - Offset 188h

This register specifies the cyclic buffer size.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 188h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is'0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

5.2.129 Input/Output Stream Descriptor x Last Valid Index (OSD1LVI) - Offset 18Ch

This register specifies the last valid buffer descriptor index.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 18Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:0	00h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0”.

5.2.130 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD1FIFOW) - Offset 18Eh

This register reports the threshold of the FIFO that triggers an access to cyclic buffer.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 18Eh	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2:0	4h RO/V	**FIFOW:** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data .The PCH HD Audio controller hardwires the FIFO Watermark, either 32B or 64Bbased on the following. Bit(2:0) Description 000-011 Reserved 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

5.2.131 Input/Output Stream Descriptor x FIFO Size (OSD1FIFOS) - Offset 190h

This register reports the FIFO size of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 190h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/V	**FIFO Size (FIFOS):** W hen GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O) SDxFMT register, the min frame of buffering setting inEM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O) SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum values could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

5.2.132 Input/Output Stream Descriptor x Format (OSD1FMT) - Offset 192h

This register specifies the audio format of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 192h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8bit containers on 16bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.133 Input/Output Stream Descriptor x FIFO Limit (OSD1FIFOL) - Offset 194h

This register controls the effective FIFO size for energy efficient audio operation.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 194h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW/L	**GNL:** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. 0 = 125 us 1 = 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC
13:0	0000h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time.0 = Disabled (FIFOS is the limit)0001h 3FFFh = 1 16383 units. When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC

5.2.134 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD1BDLPLBA) - Offset 198h

This register specifies the base address (lower 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 198h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:0	0h RO	**Reserved**

5.2.135 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD1BDLPUBA) - Offset 19Ch

This register specifies the base address (upper 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 19Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0. **Locked by:** GCAP.ADD64OK

5.2.136 Input/Output Stream Descriptor x Control (OSD2CTLB0) - Offset 1A0h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 1A0h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0. If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set). If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set). **Locked by:** SBPR.FNCFG.BCLD
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or under run for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will beset, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the streams registers. The RUN bit must be cleared before SRST is asserted.

5.2.137 Input/Output Stream Descriptor x Status (OSD2STS) - Offset 1A3h

This register provides the status of the stream DMA.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 1A3h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on the link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved**

5.2.138 Input/Output Stream Descriptor x Link Position in Buffer (OSD2LPIB) - Offset 1A4h

This register reports the link position in buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.139 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD2CBL) - Offset 1A8h

This register specifies the cyclic buffer size.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is'0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

5.2.140 Input/Output Stream Descriptor x Last Valid Index (OSD2LVI) - Offset 1ACh

This register specifies the last valid buffer descriptor index.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 1ACh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:0	00h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'

5.2.141 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD2FIFOW) - Offset 1AEh

This register reports the threshold of the FIFO that triggers an access to cyclic buffer.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 1AEh	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2:0	4h RO/V	**FIFOW:** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The PCH HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description 000-011 Reserved 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

5.2.142 Input/Output Stream Descriptor x FIFO Size (OSD2FIFOS) - Offset 1B0h

This register reports the FIFO size of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 1B0h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O) SD x FMT register, the min frame of buffering setting inEM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O) SD x FMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum values could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

5.2.143 Input/Output Stream Descriptor x Format (OSD2FMT) - Offset 1B2h

This register specifies the audio format of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 1B2h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8bit containers on 16bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.144 Input/Output Stream Descriptor x FIFO Limit (OSD2FIFOL) - Offset 1B4h

This register controls the effective FIFO size for energy efficient audio operation.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 1B4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW/L	**GNL:** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. 0 = 125 us 1 = 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC
13:0	0000h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time.0 = Disabled (FIFOS is the limit)0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC

5.2.145 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD2BDLPLBA) - Offset 1B8h

This register specifies the base address (lower 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:0	0h RO	**Reserved**

5.2.146 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD2BDLPUBA) - Offset 1BCh

This register specifies the base address (upper 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0. **Locked by:** GCAP.ADD64OK

5.2.147 Input/Output Stream Descriptor x Control (OSD3CTLB0) - Offset 1C0h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 1C0h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0.If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first-time RUN bit is set).If GCAP2.EEAC = 1 and GCAP2. DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first-time RUN bit is set). **Locked by:** SBPR.FNCFG.BCLD
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or under run for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will beset, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the streams registers. The RUN bit must be cleared before SRST is asserted.

5.2.148 Input/Output Stream Descriptor x Status (OSD3STS) - Offset 1C3h

This register provides the status of the stream DMA.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 1C3h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on the link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved**

5.2.149 Input/Output Stream Descriptor x Link Position in Buffer (OSD3LPIB) - Offset 1C4h

This register reports the link position in buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.150 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD3CBL) - Offset 1C8h

This register specifies the cyclic buffer size.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is'0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

5.2.151 Input/Output Stream Descriptor x Last Valid Index (OSD3LVI) - Offset 1CCh

This register specifies the last valid buffer descriptor index.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 1CCh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:0	00h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'

5.2.152 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD3FIFOW) - Offset 1CEh

This register reports the threshold of the FIFO that triggers an access to cyclic buffer.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 1CEh	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2:0	4h RO/V	**FIFOW:** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The PCH HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description 000-011 Reserved 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

5.2.153 Input/Output Stream Descriptor x FIFO Size (OSD3FIFOS) - Offset 1D0h

This register reports the FIFO size of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 1D0h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O) SD x FMT register, the min frame of buffering setting inEM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O) SD x FMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum values could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

5.2.154 Input/Output Stream Descriptor x Format (OSD3FMT) - Offset 1D2h

This register specifies the audio format of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 1D2h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8bit containers on 16bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.155 Input/Output Stream Descriptor x FIFO Limit (OSD3FIFOL) - Offset 1D4h

This register controls the effective FIFO size for energy efficient audio operation.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 1D4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW/L	**GNL:** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. 0 = 125 us 1 = 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC
13:0	0000h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time.0 = Disabled (FIFOS is the limit)0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC

5.2.156 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD3BDLPLBA) - Offset 1D8h

This register specifies the base address (lower 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:0	0h RO	**Reserved**

5.2.157 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD3BDLPUBA) - Offset 1DCh

This register specifies the base address (upper 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0. **Locked by:** GCAP.ADD64OK

5.2.158 Input/Output Stream Descriptor x Control (OSD4CTLB0) - Offset 1E0h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 1E0h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0.If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set).If GCAP2.EEAC = 1 and GCAP2. DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set). **Locked by:** SBPR.FNCFG.BCLD
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or under run for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.159 Input/Output Stream Descriptor x Status (OSD4STS) - Offset 1E3h

This register provides the status of the stream DMA.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 1E3h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on the link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved**

5.2.160 Input/Output Stream Descriptor x Link Position in Buffer (OSD4LPIB) - Offset 1E4h

This register reports the link position in buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.161 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD4CBL) - Offset 1E8h

This register specifies the cyclic buffer size.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is'0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

5.2.162 Input/Output Stream Descriptor x Last Valid Index (OSD4LVI) - Offset 1ECh

This register specifies the last valid buffer descriptor index.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 1ECh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:0	00h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'

5.2.163 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD4FIFOW) - Offset 1EEh

This register reports the threshold of the FIFO that triggers an access to cyclic buffer.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 1EEh	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2:0	4h RO/V	**FIFOW:** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The PCH HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description 000-011 Reserved 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

5.2.164 Input/Output Stream Descriptor x FIFO Size (OSD4FIFOS) - Offset 1F0h

This register reports the FIFO size of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 1F0h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O) SD x FMT register, the min frame of buffering setting inEM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O) SD x FMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum values could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

5.2.165 Input/Output Stream Descriptor x Format (OSD4FMT) - Offset 1F2h

This register specifies the audio format of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 1F2h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8bit containers on 16bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.166 Input/Output Stream Descriptor x FIFO Limit (OSD4FIFOL) - Offset 1F4h

This register controls the effective FIFO size for energy efficient audio operation.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 1F4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW/L	**GNL:** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. 0 = 125 us 1 = 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC
13:0	0000h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. 0 = Disabled (FIFOS is the limit) 0001h 3FFFh = 1 16383 units When value 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2. EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC

5.2.167 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD4BDLPLBA) - Offset 1F8h

This register specifies the base address (lower 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:0	0h RO	**Reserved**

5.2.168 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD4BDLPUBA) - Offset 1FCh

This register specifies the base address (upper 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1FCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0. **Locked by:** GCAP.ADD64OK

5.2.169 Input/Output Stream Descriptor x Control (OSD5CTLB0) - Offset 200h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 200h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0. If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set).If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set). **Locked by:** SBPR.FNCFG.BCLD
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or under run for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will beset, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the streams registers. The RUN bit must be cleared before SRST is asserted.

5.2.170 Input/Output Stream Descriptor x Status (OSD5STS) - Offset 203h

This register provides the status of the stream DMA.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 203h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on the link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved**

5.2.171 Input/Output Stream Descriptor x Link Position in Buffer (OSD5LPIB) - Offset 204h

This register reports the link position in buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 204h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.172 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD5CBL) - Offset 208h

This register specifies the cyclic buffer size.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 208h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is'0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

5.2.173 Input/Output Stream Descriptor x Last Valid Index (OSD5LVI) - Offset 20Ch

This register specifies the last valid buffer descriptor index.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 20Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:0	00h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'

5.2.174 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD5FIFOW) - Offset 20Eh

This register reports the threshold of the FIFO that triggers an access to cyclic buffer.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 20Eh	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2:0	4h RO/V	**FIFOW:** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The PCH HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description 000-011 Reserved 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

5.2.175 Input/Output Stream Descriptor x FIFO Size (OSD5FIFOS) - Offset 210h

This register reports the FIFO size of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 210h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O) SDxFMT register, the min frame of buffering setting inEM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O) SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum values could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

5.2.176 Input/Output Stream Descriptor x Format (OSD5FMT) - Offset 212h

This register specifies the audio format of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 212h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8bit containers on 16bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.177 Input/Output Stream Descriptor x FIFO Limit (OSD5FIFOL) - Offset 214h

This register controls the effective FIFO size for energy efficient audio operation.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 214h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW/L	**GNL:** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. 0 = 125 us 1 = 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC
13:0	0000h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. 0 = Disabled (FIFOS is the limit) 0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC

5.2.178 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD5BDLPLBA) - Offset 218h

This register specifies the base address (lower 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 218h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:0	0h RO	**Reserved**

5.2.179 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD5BDLPUBA) - Offset 21Ch

This register specifies the base address (upper 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 21Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0. **Locked by:** GCAP.ADD64OK

5.2.180 Input/Output Stream Descriptor x Control (OSD6CTLB0) - Offset 220h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 220h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0.If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set).If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set). **Locked by:** SBPR.FNCFG.BCLD
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will beset, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the streams registers. The RUN bit must be cleared before SRST is asserted.

5.2.181 Input/Output Stream Descriptor x Status (OSD6STS) - Offset 223h

This register provides the status of the stream DMA.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 223h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on the link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved**

5.2.182 Input/Output Stream Descriptor x Link Position in Buffer (OSD6LPIB) - Offset 224h

This register reports the link position in buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 224h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.183 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD6CBL) - Offset 228h

This register specifies the cyclic buffer size.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 228h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

5.2.184 Input/Output Stream Descriptor x Last Valid Index (OSD6LVI) - Offset 22Ch

This register specifies the last valid buffer descriptor index.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 22Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:0	00h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'

5.2.185 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD6FIFOW) - Offset 22Eh

This register reports the threshold of the FIFO that triggers an access to cyclic buffer.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 22Eh	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2:0	4h RO/V	**FIFOW:** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The PCH HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description 000-011 Reserved 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

5.2.186 Input/Output Stream Descriptor x FIFO Size (OSD6FIFOS) - Offset 230h

This register reports the FIFO size of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 230h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O) SDxFMT register, the mainframe of buffering setting inEM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O) SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum values could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

5.2.187 Input/Output Stream Descriptor x Format (OSD6FMT) - Offset 232h

This register specifies the audio format of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 232h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8bit containers on 16bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.188 Input/Output Stream Descriptor x FIFO Limit (OSD6FIFOL) - Offset 234h

This register controls the effective FIFO size for energy efficient audio operation.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 234h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW/L	**GNL:** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. 0 = 125 us 1 = 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC
13:0	0000h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. 0 = Disabled (FIFOS is the limit) 0001h 3FFFh = 1 16383 units When value 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC

5.2.189 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD6BDLPLBA) - Offset 238h

This register specifies the base address (lower 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 238h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:0	0h RO	**Reserved**

5.2.190 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD6BDLPUBA) - Offset 23Ch

This register specifies the base address (upper 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 23Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0. **Locked by:** GCAP.ADD64OK

5.2.191 Input/Output Stream Descriptor x Control (OSD7CTLB0) - Offset 240h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 240h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0. If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set).If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set). **Locked by:** SBPR.FNCFG.BCLD
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will beset, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the streams registers. The RUN bit must be cleared before SRST is asserted.

5.2.192 Input/Output Stream Descriptor x Status (OSD7STS) - Offset 243h

This register provides the status of the stream DMA.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 243h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on the link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved**

5.2.193 Input/Output Stream Descriptor x Link Position in Buffer (OSD7LPIB) - Offset 244h

This register reports the link position in buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 244h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.194 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD7CBL) - Offset 248h

This register specifies the cyclic buffer size.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 248h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is'0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

5.2.195 Input/Output Stream Descriptor x Last Valid Index (OSD7LVI) - Offset 24Ch

This register specifies the last valid buffer descriptor index.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 24Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:0	00h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'

5.2.196 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD7FIFOW) - Offset 24Eh

This register reports the threshold of the FIFO that triggers an access to cyclic buffer.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 24Eh	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2:0	4h RO/V	**FIFOW:** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The PCH HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description 000-011 Reserved 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

5.2.197 Input/Output Stream Descriptor x FIFO Size (OSD7FIFOS) - Offset 250h

This register reports the FIFO size of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 250h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O) SDxFMT register, the min frame of buffering setting inEM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O) SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum values could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

5.2.198 Input/Output Stream Descriptor x Format (OSD7FMT) - Offset 252h

This register specifies the audio format of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 252h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8bit containers on 16bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.199 Input/Output Stream Descriptor x FIFO Limit (OSD7FIFOL) - Offset 254h

This register controls the effective FIFO size for energy efficient audio operation.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 254h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW/L	**GNL:** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. 0 = 125 us 1 = 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC
13:0	0000h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. 0 = Disabled (FIFOS is the limit) 0001h 3FFFh = 1 16383 units When value 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC

5.2.200 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD7BDLPLBA) - Offset 258h

This register specifies the base address (lower 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 258h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:0	0h RO	**Reserved**

5.2.201 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD7BDLPUBA) - Offset 25Ch

This register specifies the base address (upper 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 25Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0. **Locked by:** GCAP.ADD64OK

5.2.202 Input/Output Stream Descriptor x Control (OSD8CTLB0) - Offset 260h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 260h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0. If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set).If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set). **Locked by:** SBPR.FNCFG.BCLD
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will beset, but the interrupt will not occur.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the streams registers. The RUN bit must be cleared before SRST is asserted.

5.2.203 Input/Output Stream Descriptor x Status (OSD8STS) - Offset 263h

This register provides the status of the stream DMA.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + 263h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on the link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved**

5.2.204 Input/Output Stream Descriptor x Link Position in Buffer (OSD8LPIB) - Offset 264h

This register reports the link position in buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 264h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.205 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD8CBL) - Offset 268h

This register specifies the cyclic buffer size.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 268h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is'0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

5.2.206 Input/Output Stream Descriptor x Last Valid Index (OSD8LVI) - Offset 26Ch

This register specifies the last valid buffer descriptor index.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 26Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:0	00h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'

5.2.207 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD8FIFOW) - Offset 26Eh

This register reports the threshold of the FIFO that triggers an access to cyclic buffer.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 26Eh	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2:0	4h RO/V	**FIFOW:** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The PCH HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description 000-011 Reserved 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

5.2.208 Input/Output Stream Descriptor x FIFO Size (OSD8FIFOS) - Offset 270h

This register reports the FIFO size of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 270h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O) SDxFMT register, the min frame of buffering setting inEM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O) SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum values could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

5.2.209 Input/Output Stream Descriptor x Format (OSD8FMT) - Offset 272h

This register specifies the audio format of the stream DMA.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 272h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8bit containers on 16bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.210 Input/Output Stream Descriptor x FIFO Limit (OSD8FIFOL) - Offset 274h

This register controls the effective FIFO size for energy efficient audio operation.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 274h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW/L	**GNL:** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. 0 = 125 us 1 = 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC
13:0	0000h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. 0 = Disabled (FIFOS is the limit) 0001h 3FFFh = 1 16383 units When value 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO). **Locked by:** GCAP2.EEAC

5.2.211 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD8BDLPLBA) - Offset 278h

This register specifies the base address (lower 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 278h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:0	0h RO	**Reserved**

5.2.212 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD8BDLPUBA) - Offset 27Ch

This register specifies the base address (upper 32 bits) of Buffer Descriptor List.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 27Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0. **Locked by:** GCAP.ADD64OK

5.2.213 Global Time Synchronization Capability Header (GTSCH) - Offset 500h

This register declares the global time synchronization capability structure.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 500h	00011F00h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW/L	**Capability Version (VER):** This field is an Intel HD Audio Specification defined version number that indicates the version of the capability structure present. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
27:16	001h RW/L	**Capability Identifier (ID):** This field is an Intel HD Audio Specification defined ID number that indicates the nature and format of the capability. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
15:0	1F00h RW/L	**Next Capability Pointer (PTR):** This field contains the offset to the next capability structure or 000h if no other items exist in the linked list of capabilities. Point to DMA resume capability. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD

5.2.214 Global Time Synchronization Capability Declaration (GTSCD) - Offset 504h

This register identifies the general global time synchronization associated capabilities.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 504h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RO	**Controller Based Synchronization Adjust Supported (CTLSAS):** When set, it indicates that the controller based synchronization adjustment is supported. By adjusting the global link clock which is used as reference clock for the codecs DAC / ADC, the codec will indirectly changing the rate of all its active streams. Locked when FNCFG.BCLD = 1.
1:0	0h RO	**Reserved**

5.2.215 Global Time Synchronization Capture Control (GTSCC0) - Offset 520h

This register controls the global time synchronization capture operation, and snapshots ART value as the global time stamp counter value.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 520h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Time Stamp Counter Capture Done (TSCCD):** This bit is set when a valid TSC value has been captured: WALFCC, TSCCL, TSCCU, LLPFOC, LLPCL, and LLPCH contain valid data. The Intel HD Audio driver software must acknowledge the completion by writing 1 to clear this bit.
30	0h RW	**Time Stamp Counter Capture Done Interrupt Enable (TSCCDIE):** If set to 1, TSCCD bit can pass through to cause an interrupt status reported in INTSTS.CIS bit, and cause an interrupt to CPU if INTCTL.CIE = 1 and INTCTL.GIE = 1.
29:6	0h RO	**Reserved**
5	0h RW/1S/V	**Time Stamp Counter Capture Initiate (TSCCI):** Write to 1 to initiate Global Time Synchronization capture for measuring TSC offset to local wall frame info. Cleared to 0 by hardware when the process is completed.
4:0	00h RW	**Capture DMA Select (CDMAS):** To select which DMA's LLPL, and LLPU value to be captured together with the TSC value. Bit 4 = 1 for ODMA, 0 for IDMA Bit 3:0 indicates the respective DMA engine index. Programmed before TSCCI = 1.

5.2.216 Wall Frame Counter Captured (WALFCC0) - Offset 524h

This register reports the wall frame counter captured.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 524h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	000000h RO/V	**Frame Number (FN):** Indicates the 23 bit frame number captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.
8:0	000h RO/V	**Clock in Frame (CIF):** Indicates the 9 bit clock in frame value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

5.2.217 Time Stamp Counter Captured Lower (TSCCL0) - Offset 528h

This register reports the ART value snapshot as the global time stamp counter captured (lower 32 bits).

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 528h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Counter Captured Lower (CCL):** Indicates the lower 32 bit TSC value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

5.2.218 Time Stamp Counter Captured Upper (TSCCU0) - Offset 52Ch

This register reports the ART value snapshot as the global time stamp counter captured (upper 32 bits).

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 52Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Counter Captured Upper (CCU):** Indicates the upper 32 bit TSC value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

5.2.219 Linear Link Position Frame Offset Captured (LLPFOC0) - Offset 534h

This register is to report additional accuracy details for captures made in between of two updates of LLP values, in number of 48 KHz HD Audio frames of the corresponding link. Audio streams with 44.1 KHz base rate and non-zero divider FMT value will skip frames periodically on the Intel HD Audio link and Intel iDisplay Audio link in order to normalize its sampling rate to the 48 KHz HD Audio frame rate; hence; the frame offset will be useful in these cases.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 534h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RO/V	**Frame Offset Captured (FOC):** When the LLPCL and LLPCU registers are updated, this field records the elapsed number of 48 KHz HD Audio frames since the last LLP value change. Valid and static when GTSCC.TSCCD = 1

5.2.220 Linear Link Position Captured Lower (LLPCL0) - Offset 538h

This register reports the linear link position counter captured (lower 32 bits).

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 538h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Linear Link Position Captured Lower (LLPCL):** Indicates the lower 32 bit linear link position value of the link DMA captured as a result of Global Time Synchronization capture request. Note that the LLPCL value that is captured is the LLPL value at the previous HD Audio frame boundary, not the live LLPL register value which may be changing in the middle of the current frame. Valid and static when GTSCC.TSCCD = 1.

5.2.221 Linear Link Position Captured Upper (LLPCU0) - Offset 53Ch

This register reports the time stamp counter captured (upper 32 bits).

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 53Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Linear Link Position Captured Upper (LLPCU):** Indicates the upper 32 bit linear link position value of the link DMA captured as a result of Global Time Synchronization capture request. Note that the LLPCU value that is captured is the LLPU value at the previous HD Audio frame boundary, not the live LLPU register value which may be changing in the middle of the current frame. Valid and static when GTSCC.TSCCD = 1.

5.2.222 Global Time Synchronization Capture Control (GTSCC1) - Offset 540h

This register controls the global time synchronization capture operation, and snapshots ART value as the global time stamp counter value.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 540h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Time Stamp Counter Capture Done (TSCCD):** This bit is set when a valid TSC value has been captured: WALFCC, TSCCL, TSCCU, LLPFOC, LLPCL, and LLPCH contain valid data. The Intel HD Audio driver software must acknowledge the completion by writing 1 to clear this bit.
30	0h RW	**Time Stamp Counter Capture Done Interrupt Enable (TSCCDIE):** If set to 1, TSCCD bit can pass through to cause an interrupt status reported in INTSTS.CIS bit, and cause an interrupt to CPU if INTCTL.CIE = 1 and INTCTL.GIE = 1.
29:6	0h RO	**Reserved**
5	0h RW/1S/V	**Time Stamp Counter Capture Initiate (TSCCI):** Write to 1 to initiate Global Time Synchronization capture for measuring TSC offset to local wall frame info. Cleared to 0 by hardware when the process is completed.
4:0	00h RW	**Capture DMA Select (CDMAS):** To select which DMA's LLPL, and LLPU value to be captured together with the TSC value. Bit 4 = 1 for ODMA, 0 for IDMA Bit 3:0 indicates the respective DMA engine index. Programmed before TSCCI = 1.

5.2.223 Wall Frame Counter Captured (WALFCC1) - Offset 544h

This register reports the wall frame counter captured.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 544h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	000000h RO/V	**Frame Number (FN):** Indicates the 23 bit frame number captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.
8:0	000h RO/V	**Clock in Frame (CIF):** Indicates the 9 bit clock in frame value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

5.2.224 Time Stamp Counter Captured Lower (TSCCL1) - Offset 548h

This register reports the ART value snapshot as the global time stamp counter captured (lower 32 bits).

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 548h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Counter Captured Lower (CCL):** Indicates the lower 32 bit TSC value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

5.2.225 Time Stamp Counter Captured Upper (TSCCU1) - Offset 54Ch

This register reports the ART value snapshot as the global time stamp counter captured (upper 32 bits).

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 54Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Counter Captured Upper (CCU):** Indicates the upper 32 bit TSC value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

5.2.226 Linear Link Position Frame Offset Captured (LLPFOC1) - Offset 554h

This register is to report additional accuracy details for captures made in

between of two updates of LLP values, in number of 48 KHz HD Audio frames of the corresponding link. Audio streams with 44.1 KHz base rate and non-zero divider FMT value will skip frames periodically on the Intel HD Audio link and Intel iDisplay Audio link in order to normalize its sampling rate to the 48 KHz HD Audio frame rate; hence; the frame offset will be useful in these cases.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 554h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RO/V	**Frame Offset Captured (FOC):** When the LLPCL and LLPCU registers are updated, this field records the elapsed number of 48 KHz HD Audio frames since the last LLP value change. Valid and static when GTSCC.TSCCD = 1

5.2.227 Linear Link Position Captured Lower (LLPCL1) - Offset 558h

This register reports the linear link position counter captured (lower 32 bits).

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 558h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Linear Link Position Captured Lower (LLPCL):** Indicates the lower 32 bit linear link position value of the link DMA captured as a result of Global Time Synchronization capture request.Note that the LLPCL value that is captured is the LLPL value at the previous HD Audio frame boundary, not the live LLPL register value which may be changing in the middle of the current frame.Valid and static when GTSCC.TSCCD = 1.

5.2.228 Linear Link Position Captured Upper (LLPCU1) - Offset 55Ch

This register reports the time stamp counter captured (upper 32 bits).

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 55Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Linear Link Position Captured Upper (LLPCU):** Indicates the upper 32 bit linear link position value of the link DMA captured as a result of Global Time Synchronization capture request. Note that the LLPCU value that is captured is the LLPU value at the previous HD Audio frame boundary, not the live LLPU register value which may be changing in the middle of the current frame. Valid and static when GTSCC.TSCCD = 1.

5.2.229 Software Position Based FIFO Capability Header (SPBFCH) - Offset 700h

This register declares the software position FIFO capability structure.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 700h	00040000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW/L	**Capability Version (VER):** This field is an Intel HD Audio Specification defined version number that indicates the version of the capability structure present. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
27:16	004h RW/L	**Capability Identifier (ID):** This field is an Intel HD Audio Specification defined ID number that indicates the nature and format of the capability. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
15:0	0000h RW/L	**Next Capability Pointer (PTR):** This field contains the offset to the next capability structure or 000h if no other items exist in the linked list of capabilities. This is the last capability in the linked list Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD

5.2.230 Software Position Based FIFO Control (SPBFCTL) - Offset 704h

The number of SPIBE bits in this register is depending on the total number of streams DMA implemented, represented as x in the register table. The x value is determined by the parameter equation: HSTISC + HSTOSC. For SPT implementation, x = 16.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 704h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Software Position in Buffer Enable (SPIBE):** When set to 1, the SPIB register is the limit where the DMA will not access beyond the value programmed. When clear to 0, the SPIB register is ignored and DMA will operate in legacy mode with the minimum FIFO size. Note that it is possible for SW to set this SPIBE bit after the RUN bit is set as SW may only update the SPIB after it fills up a large portion of the ring buffer. However, once set, it must remain set until SRST take place.

5.2.231 Input/Output Stream Descriptor x Software Position in Buffer (ISD0SPIB) - Offset 708h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 708h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.232 Input/Output Stream Descriptor x Max FIFO Size (ISD0MAXFIFOS) - Offset 70Ch

This register reports the max FIFO size for software position based FIFO operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 70Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allows through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

5.2.233 Input/Output Stream Descriptor x Software Position in Buffer (ISD1SPIB) - Offset 710h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 710h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.234 Input/Output Stream Descriptor x Max FIFO Size (ISD1MAXFIFOS) - Offset 714h

This register reports the max FIFO size for software position based FIFO operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 714h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allows through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

5.2.235 Input/Output Stream Descriptor x Software Position in Buffer (ISD2SPIB) - Offset 718h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 718h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.236 Input/Output Stream Descriptor x Max FIFO Size (ISD2MAXFIFOS) - Offset 71Ch

This register reports the max FIFO size for software position based FIFO operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 71Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allows through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

5.2.237 Input/Output Stream Descriptor x Software Position in Buffer (ISD3SPIB) - Offset 720h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 720h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.238 Input/Output Stream Descriptor x Max FIFO Size (ISD3MAXFIFOS) - Offset 724h

This register reports the max FIFO size for software position based FIFO operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 724h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allows through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

5.2.239 Input/Output Stream Descriptor x Software Position in Buffer (ISD4SPIB) - Offset 728h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 728h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.240 Input/Output Stream Descriptor x Max FIFO Size (ISD4MAXFIFOS) - Offset 72Ch

This register reports the max FIFO size for software position based FIFO operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 72Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allows through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

5.2.241 Input/Output Stream Descriptor x Software Position in Buffer (ISD5SPIB) - Offset 730h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 730h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.242 Input/Output Stream Descriptor x Max FIFO Size (ISD5MAXFIFOS) - Offset 734h

This register reports the max FIFO size for software position based FIFO operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 734h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allows through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

5.2.243 Input/Output Stream Descriptor x Software Position in Buffer (ISD6SPIB) - Offset 738h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 738h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.244 Input/Output Stream Descriptor x Max FIFO Size (ISD6MAXFIFOS) - Offset 73Ch

This register reports the max FIFO size for software position based FIFO operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 73Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allows through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

5.2.245 Input/Output Stream Descriptor x Software Position in Buffer (OSD0SPIB) - Offset 740h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 740h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.246 Input/Output Stream Descriptor x Max FIFO Size (OSD0MAXFIFOS) - Offset 744h

This register reports the max FIFO size for software position based FIFO operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 744h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allows through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

5.2.247 Input/Output Stream Descriptor x Software Position in Buffer (OSD1SPIB) - Offset 748h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 748h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.248 Input/Output Stream Descriptor x Max FIFO Size (OSD1MAXFIFOS) - Offset 74Ch

This register reports the max FIFO size for software position based FIFO operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 74Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allows through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

5.2.249 Input/Output Stream Descriptor x Software Position in Buffer (OSD2SPIB) - Offset 750h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 750h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.250 Input/Output Stream Descriptor x Max FIFO Size (OSD2MAXFIFOS) - Offset 754h

This register reports the max FIFO size for software position based FIFO operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 754h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allows through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

5.2.251 Input/Output Stream Descriptor x Software Position in Buffer (OSD3SPIB) - Offset 758h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 758h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.252 Input/Output Stream Descriptor x Max FIFO Size (OSD3MAXFIFOS) - Offset 75Ch

This register reports the max FIFO size for software position based FIFO operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 75Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allows through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

5.2.253 Input/Output Stream Descriptor x Software Position in Buffer (OSD4SPIB) - Offset 760h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 760h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.254 Input/Output Stream Descriptor x Max FIFO Size (OSD4MAXFIFOS) - Offset 764h

This register reports the max FIFO size for software position based FIFO operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 764h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allows through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

5.2.255 Input/Output Stream Descriptor x Software Position in Buffer (OSD5SPIB) - Offset 768h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 768h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.256 Input/Output Stream Descriptor x Max FIFO Size (OSD5MAXFIFOS) - Offset 76Ch

This register reports the max FIFO size for software position based FIFO operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 76Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allows through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

5.2.257 Input/Output Stream Descriptor x Software Position in Buffer (OSD6SPIB) - Offset 770h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 770h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.258 Input/Output Stream Descriptor x Max FIFO Size (OSD6MAXFIFOS) - Offset 774h

This register reports the max FIFO size for software position based FIFO operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 774h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allow through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

5.2.259 Input/Output Stream Descriptor x Software Position in Buffer (OSD7SPIB) - Offset 778h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 778h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.260 Input/Output Stream Descriptor x Max FIFO Size (OSD7MAXFIFOS) - Offset 77Ch

This register reports the max FIFO size for software position based FIFO operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 77Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allows through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

5.2.261 Input/Output Stream Descriptor x Software Position in Buffer (OSD8SPIB) - Offset 780h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 780h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.262 Input/Output Stream Descriptor x Max FIFO Size (OSD8MAXFIFOS) - Offset 784h

This register reports the max FIFO size for software position based FIFO operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 784h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allows through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

5.2.263 Processing Pipe Capability Header (PPCH) - Offset 800h

This register declares the processing pipe capability structure.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 800h	00030500h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW/L	**Capability Version (VER):** This field is an Intel HD Audio Specification defined version number that indicates the version of the capability structure present. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
27:16	003h RW/L	**Capability Identifier (ID):** This field is an Intel HD Audio Specification defined ID number that indicates the nature and format of the capability. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
15:0	0500h RW/L	**Next Capability Pointer (PTR):** This field contains the offset to the next capability structure or 000h if no other item sexist in the linked list of capabilities. Point to Global Time Synchronization capability. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD

5.2.264 Processing Pipe Control (PPCTL) - Offset 804h

This register is not affected by stream reset.

Note that the PROCEN bit should only be modified when the corresponding host DMA and link DMA are idle, i.e. RUN bits are cleared, and the DMA contexts have been destroyed through SRST bits if it was previously activated.

Note that GPROCEN bit does not really enable or disable the Audio DSP operation, but mainly to work around some legacy Intel HD Audio driver software such that if GPROCEN = 0, ADSPxBA (BAR2) is mapped to the Intel HD Audio memory mapped configuration registers, for compliance with some legacy SW implementation. If GPROCEN = 1, only then ADSPxBA (BAR2) is mapped to the actual Audio DSP memory mapped configuration registers.

The number of PROCEN bits in this register is depending on the total number of streams DMA implemented, represented as x in the register table. The x value is determined by the parameter equation: HSTISC + HSTOSC. For SPT implementation, x = 16.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 804h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Processing Interrupt Enable (PIE):** Enables the general interrupt for the Audio DSP function. When set to 1 (and GIE is enabled), the Audio DSP generates an interrupt when the PIS bit gets set.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RW	**Global Processing Enable (GPROCEN):** When set to 1, it indicates that the Audio DSP is enabled for operation.
29:16	0h RO	**Reserved**
15:0	0000h RW	**Processing Enable (PROCEN):** When set to 1 the DMA engine associated with this stream will be enabled to route the audio stream to DSP audio pipes in the Audio DSP for processing. When cleared to 0 the DMA engine associated with this stream will be bypassing the Audio DSP and route the audio stream directly to the audio link.

5.2.265 Processing Pipe Status (PPSTS) - Offset 808h

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 808h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Processing Interrupt Status (PIS):** Status of general interrupt for the Audio DSP function. A 1 indicates that an interrupt condition occurred in the Audio DSP function. The exact cause can be determined by interrogating the ADSPIS register. Note that HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of the interrupt status bits in ADSPIS register.
30:0	0h RO	**Reserved**

5.2.266 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC0LLPL) - Offset 810h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 810h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.267 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC0LLPU) - Offset 814h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 814h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.268 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC0LDPL) - Offset 818h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 818h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.269 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC0LDPU) - Offset 81Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 81Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.270 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC1LLPL) - Offset 820h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 820h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.271 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC1LLPU) - Offset 824h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 824h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.272 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC1LDPL) - Offset 828h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 828h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.273 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC1LDPU) - Offset 82Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 82Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.274 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC2LLPL) - Offset 830h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 830h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.275 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC2LLPU) - Offset 834h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 834h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.276 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC2LDPL) - Offset 838h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 838h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.277 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC2LDPU) - Offset 83Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 83Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.278 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC3LLPL) - Offset 840h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 840h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.279 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC3LLPU) - Offset 844h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 844h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.280 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC3LDPL) - Offset 848h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 848h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.281 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC3LDPU) - Offset 84Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 84Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.282 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC4LLPL) - Offset 850h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 850h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.283 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC4LLPU) - Offset 854h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 854h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.284 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC4LDPL) - Offset 858h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 858h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.285 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC4LDPU) - Offset 85Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 85Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.286 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC5LLPL) - Offset 860h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 860h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.287 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC5LLPU) - Offset 864h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 864h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.288 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC5LDPL) - Offset 868h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 868h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.289 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC5LDPU) - Offset 86Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 86Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.290 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC6LLPL) - Offset 870h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 870h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.291 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC6LLPU) - Offset 874h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 874h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.292 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC6LDPL) - Offset 878h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 878h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.293 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC6LDPU) - Offset 87Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 87Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.294 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC0LLPL) - Offset 880h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 880h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.295 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC0LLPU) - Offset 884h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 884h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.296 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC0LDPL) - Offset 888h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 888h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.297 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC0LDPU) - Offset 88Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 88Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.298 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC1LLPL) - Offset 890h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 890h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.299 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC1LLPU) - Offset 894h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 894h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.300 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC1LDPL) - Offset 898h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 898h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.301 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC1LDPU) - Offset 89Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 89Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.302 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC2LLPL) - Offset 8A0h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.303 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC2LLPU) - Offset 8A4h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.304 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC2LDPL) - Offset 8A8h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.305 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC2LDPU) - Offset 8ACh

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.306 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC3LLPL) - Offset 8B0h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.307 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC3LLPU) - Offset 8B4h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.308 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC3LDPL) - Offset 8B8h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.309 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC3LDPU) - Offset 8BCh

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.310 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC4LLPL) - Offset 8C0h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.311 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC4LLPU) - Offset 8C4h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.312 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC4LDPL) - Offset 8C8h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.313 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC4LDPU) - Offset 8CCh

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.314 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC5LLPL) - Offset 8D0h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.315 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC5LLPU) - Offset 8D4h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.316 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC5LDPL) - Offset 8D8h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.317 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC5LDPU) - Offset 8DCh

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.318 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC6LLPL) - Offset 8E0h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.319 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC6LLPU) - Offset 8E4h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.320 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC6LDPL) - Offset 8E8h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.321 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC6LDPU) - Offset 8ECh

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.322 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC7LLPL) - Offset 8F0h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8F0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.323 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC7LLPU) - Offset 8F4h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8F4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1).Once RUN bit is set, the register will become read only until SRST occurs.

5.2.324 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC7LDPL) - Offset 8F8h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.325 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC7LDPU) - Offset 8FCh

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 8FCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.326 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC8LLPL) - Offset 900h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 900h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.327 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC8LLPU) - Offset 904h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 904h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.328 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC8LDPL) - Offset 908h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 908h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.329 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC8LDPU) - Offset 90Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 90Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.330 Input/Output Processing Pipe's Link Connection x Control (IPPLC0CTL) - Offset 910h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 910h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.331 Input/Output Processing Pipe's Link Connection x Format (IPPLC0FMT) - Offset 914h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 914h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.332 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC0LLPL) - Offset 918h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 918h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.333 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC0LLPU) - Offset 91Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 91Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.334 Input/Output Processing Pipe's Link Connection x Control (IPPLC1CTL) - Offset 920h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 920h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.335 Input/Output Processing Pipe's Link Connection x Format (IPPLC1FMT) - Offset 924h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 924h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.336 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC1LLPL) - Offset 928h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 928h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.337 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC1LLPU) - Offset 92Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 92Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.338 Input/Output Processing Pipe's Link Connection x Control (IPPLC2CTL) - Offset 930h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 930h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.339 Input/Output Processing Pipe's Link Connection x Format (IPPLC2FMT) - Offset 934h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 934h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.340 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC2LLPL) - Offset 938h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 938h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.341 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC2LLPU) - Offset 93Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 93Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.342 Input/Output Processing Pipe's Link Connection x Control (IPPLC3CTL) - Offset 940h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 940h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.343 Input/Output Processing Pipe's Link Connection x Format (IPPLC3FMT) - Offset 944h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 944h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.344 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC3LLPL) - Offset 948h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 948h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.345 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC3LLPU) - Offset 94Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 94Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.346 Input/Output Processing Pipe's Link Connection x Control (IPPLC4CTL) - Offset 950h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 950h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.347 Input/Output Processing Pipe's Link Connection x Format (IPPLC4FMT) - Offset 954h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 954h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.348 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC4LLPL) - Offset 958h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 958h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.349 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC4LLPU) - Offset 95Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 95Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.350 Input/Output Processing Pipe's Link Connection x Control (IPPLC5CTL) - Offset 960h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 960h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.351 Input/Output Processing Pipe's Link Connection x Format (IPPLC5FMT) - Offset 964h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 964h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.352 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC5LLPL) - Offset 968h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 968h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.353 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC5LLPU) - Offset 96Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 96Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.354 Input/Output Processing Pipe's Link Connection x Control (IPPLC6CTL) - Offset 970h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 970h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.355 Input/Output Processing Pipe's Link Connection x Format (IPPLC6FMT) - Offset 974h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 974h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.356 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC6LLPL) - Offset 978h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 978h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.357 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC6LLPU) - Offset 97Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 97Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.358 Input/Output Processing Pipe's Link Connection x Control (OPPLC0CTL) - Offset 980h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 980h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.359 Input/Output Processing Pipe's Link Connection x Format (OPPLC0FMT) - Offset 984h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 984h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.360 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC0LLPL) - Offset 988h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 988h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.361 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC0LLPU) - Offset 98Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 98Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.362 Input/Output Processing Pipe's Link Connection x Control (OPPLC1CTL) - Offset 990h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 990h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.363 Input/Output Processing Pipe's Link Connection x Format (OPPLC1FMT) - Offset 994h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 994h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.364 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC1LLPL) - Offset 998h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 998h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.365 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC1LLPU) - Offset 99Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 99Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.366 Input/Output Processing Pipe's Link Connection x Control (OPPLC2CTL) - Offset 9A0h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 9A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.367 Input/Output Processing Pipe's Link Connection x Format (OPPLC2FMT) - Offset 9A4h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 9A4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.368 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC2LLPL) - Offset 9A8h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 9A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.369 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC2LLPU) - Offset 9ACh

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 9ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.370 Input/Output Processing Pipe's Link Connection x Control (OPPLC3CTL) - Offset 9B0h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 9B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.371 Input/Output Processing Pipe's Link Connection x Format (OPPLC3FMT) - Offset 9B4h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 9B4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.372 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC3LLPL) - Offset 9B8h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 9B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.373 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC3LLPU) - Offset 9BCh

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 9BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.374 Input/Output Processing Pipe's Link Connection x Control (OPPLC4CTL) - Offset 9C0h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 9C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.375 Input/Output Processing Pipe's Link Connection x Format (OPPLC4FMT) - Offset 9C4h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 9C4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.376 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC4LLPL) - Offset 9C8h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 9C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.377 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC4LLPU) - Offset 9CCh

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 9CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.378 Input/Output Processing Pipe's Link Connection x Control (OPPLC5CTL) - Offset 9D0h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 9D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.379 Input/Output Processing Pipe's Link Connection x Format (OPPLC5FMT) - Offset 9D4h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 9D4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.380 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC5LLPL) - Offset 9D8h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 9D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.381 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC5LLPU) - Offset 9DCh

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 9DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.382 Input/Output Processing Pipe's Link Connection x Control (OPPLC6CTL) - Offset 9E0h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 9E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.383 Input/Output Processing Pipe's Link Connection x Format (OPPLC6FMT) - Offset 9E4h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 9E4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.384 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC6LLPL) - Offset 9E8h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 9E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.385 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC6LLPU) - Offset 9ECh

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 9ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.386 Input/Output Processing Pipe's Link Connection x Control (OPPLC7CTL) - Offset 9F0h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 9F0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.387 Input/Output Processing Pipe's Link Connection x Format (OPPLC7FMT) - Offset 9F4h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 9F4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.388 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC7LLPL) - Offset 9F8h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 9F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.389 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC7LLPU) - Offset 9FCh

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 9FCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.390 Input/Output Processing Pipe's Link Connection x Control (OPPLC8CTL) - Offset A00h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + A00h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.391 Input/Output Processing Pipe's Link Connection x Format (OPPLC8FMT) - Offset A04h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + A04h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.392 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC8LLPL) - Offset A08h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + A08h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.393 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC8LLPU) - Offset A0Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + A0Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.394 Multiple Links Capability Header (MLCH) - Offset C00h

This register declares the multiple links capability structure.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + C00h	00020800h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW/L	**Capability Version (VER):** This field is an Intel HD Audio Specification defined version number that indicates the version of the capability structure present. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
27:16	002h RW/L	**Capability Identifier (ID):** This field is an Intel HD Audio Specification defined ID number that indicates the nature and format of the capability. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
15:0	0800h RW/L	**Next Capability Pointer (PTR):** This field contains the offset to the next capability structure or 000h if no other item sexist in the linked list of capabilities. Point to Processing Pipe capability. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD

5.2.395 Multiple Links Capability Declaration (MLCD) - Offset C04h

This register identifies the general multiple links associated capabilities.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + C04h	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	1h RO	**Link Count (LCOUNT):** Indicates the number of links. Up to 15 links can be supported. A '0' indicates 1 link, and '1110' indicates 15 links. ***Note***: '1111' is reserved. Note that this Link Count is the cumulative total number of links where the links can be heterogeneous. This field is hard coded to parameter LNKC-1.

5.2.396 Link x Capabilities (LCAP0) - Offset C40h

This register identifies the specific link associated capabilities

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + C40h	00000007h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW/L	**Audio Link Type (ALT):** Indicates which Link Type this link belongs to. 0001-1111 = Reserved 0000 = Intel HD Audio Link Reset value is hard coded to parameter LCAPALT[x*4+3:x*4]. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
27:26	0h RO	**Reserved**
25:24	0h RW/L	**Number of Serial Data Out Signals (NSDO):** 00b indicates that the Intel HD Audio controller supports one Serial Data Output signal. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
23:6	0h RO	**Reserved**
5	0h RW/L	**192 MHz Supported (S192):** Indicates 192 MHz clock is supported. Reset value is hard coded to parameter DEFLCAPS192[x]. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
4	0h RW/L	**96 MHz Supported (S96):** Indicates 96 MHz clock is supported. Reset value is hard coded to parameter DEFLCAPS96[x]. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
3	0h RW/L	**48 MHz Supported (S48):** Indicates 48 MHz clock is supported. Reset value is hard coded to parameter DEFLCAPS48[x]. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD

Bit Range	Default & Access	Field Name (ID): Description
2	1h RW/L	**24 MHz Supported (S24):** Indicates 24 MHz clock is supported. Reset value is hard coded to parameter DEFLCAPS24[x]. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
1	1h RW/L	**12 MHz Supported (S12):** Indicates 12 MHz clock is supported. Reset value is hard coded to parameter DEFLCAPS12[x]. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
0	1h RW/L	**6 MHz Supported (S6):** Indicates 6 MHz clock is supported. Reset value is hard coded to parameter DEFLCAPS6[x]. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD

5.2.397 Link x Control (LCTL0) - Offset C44h

Link x Control

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + C44h	00010002h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO/V	**Current Power Active (CPA):** This value changes to the value set by SPA when the power of the link has reached that state. Software sets SPA, then monitors CPA to know when the link has changed state.
22:17	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
16	1h RW	**Set Power Active (SPA):** Software sets this bit to '1' to turn the link on (provided CRSTB = 1), and clears it to '0'when it wishes to turn the link off. When CPA matches the value of this bit, the achieved power state has been reached. Software is expected to wait for CPA to match SPA before it can program SPA again. Any deviation may result in undefined behavior.
15:4	0h RO	**Reserved**
3:0	2h RW	**Set Clock Frequency (SCF):** Indicates the frequency that software wishes the link to run at. Changing this value to a value not supported by Link Capabilities shall result in indeterminate results. The possible encodings are: Encoding Frequency 0000 6 MHz 0001 12 MHz 0010 24 MHz 0011 48 MHz 0100 96 MHz 0101 Reserved for 192 MHz 0110-1111 Reserved

5.2.398 Link x Output Stream ID Mapping Valid (LOSIDV0) - Offset C48h

This register maps the output stream connection for specific link.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + C48h	0000FFFEh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	1h RW	**Output Stream ID of 15 is Valid for this Link (L1OSIDV15):** This link will claim / forward output cycles with Stream ID = 1111b.
14	1h RW	**Output Stream ID of 14 is Valid for this Link (L1OSIDV14):** This link will claim / forward output cycles with Stream ID = 1110b.
13	1h RW	**Output Stream ID of 13 is Valid for this Link (L1OSIDV13):** This link will claim / forward output cycles with Stream ID = 1101b.
12	1h RW	**Output Stream ID of 12 is Valid for this Link (L1OSIDV12):** This link will claim / forward output cycles with Stream ID = 1100b.
11	1h RW	**Output Stream ID of 11 is Valid for this Link (L1OSIDV11):** This link will claim / forward output cycles with Stream ID = 1011b.
10	1h RW	**Output Stream ID of 10 is Valid for this Link (L1OSIDV10):** This link will claim / forward output cycles with Stream ID = 1010b.
9	1h RW	**Output Stream ID of 9 is Valid for this Link (L1OSIDV9):** This link will claim / forward output cycles with Stream ID = 1001b.

Bit Range	Default & Access	Field Name (ID): Description
8	1h RW	**Output Stream ID of 8 is Valid for this Link (L1OSIDV8):** This link will claim / forward output cycles with Stream ID = 1000b.
7	1h RW	**Output Stream ID of 7 is Valid for this Link (L1OSIDV7):** This link will claim / forward output cycles with Stream ID = 0111b.
6	1h RW	**Output Stream ID of 6 is Valid for this Link (L1OSIDV6):** This link will claim / forward output cycles with Stream ID = 0110b.
5	1h RW	**Output Stream ID of 5 is Valid for this Link (L1OSIDV5):** This link will claim / forward output cycles with Stream ID = 0101b.
4	1h RW	**Output Stream ID of 4 is Valid for this Link (L1OSIDV4):** This link will claim / forward output cycles with Stream ID = 0100b.
3	1h RW	**Output Stream ID of 3 is Valid for this Link (L1OSIDV3):** This link will claim / forward output cycles with Stream ID = 0011b.
2	1h RW	**Output Stream ID of 2 is Valid for this Link (L1OSIDV2):** This link will claim / forward output cycles with Stream ID = 0010b.
1	1h RW	**Output Stream ID of 1 is Valid for this Link (L1OSIDV1):** This link will claim / forward output cycles with Stream ID = 0001b.
0	0h RO	**Reserved**

5.2.399 Link x SDI Identifier (LSDIID0) - Offset C4Ch

Link x SDI Identifier

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + C4Ch	00000003h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14	0h RO	**SDI 14 (SDIID14):** This link uses SDI 14. This bit is hard coded per parameter LSDIID14 assignment.
13	0h RO	**SDI 13 (SDIID13):** This link uses SDI 13. This bit is hard coded per parameter LSDIID13 assignment.
12	0h RO	**SDI 12 (SDIID12):** This link uses SDI 12. This bit is hard coded per parameter LSDIID12 assignment.
11	0h RO	**SDI 11 (SDIID11):** This link uses SDI 11. This bit is hard coded per parameter LSDIID11 assignment.
10	0h RO	**SDI 10 (SDIID10):** This link uses SDI 10. This bit is hard coded per parameter LSDIID10 assignment.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**SDI 9 (SDIID9):** This link uses SDI 9. This bit is hard coded per parameter LSDIID9 assignment.
8	0h RO	**SDI 8 (SDIID8):** This link uses SDI 8. This bit is hard coded per parameter LSDIID8 assignment.
7	0h RO	**SDI 7 (SDIID7):** This link uses SDI 7. This bit is hard coded per parameter LSDIID7 assignment.
6	0h RO	**SDI 6 (SDIID6):** This link uses SDI 6. This bit is hard coded per parameter LSDIID6 assignment.
5	0h RO	**SDI 5 (SDIID5):** This link uses SDI 5. This bit is hard coded per parameter LSDIID5 assignment.
4	0h RO	**SDI 4 (SDIID4):** This link uses SDI 4. This bit is hard coded per parameter LSDIID4 assignment.
3	0h RO	**SDI 3 (SDIID3):** This link uses SDI 3. This bit is hard coded per parameter LSDIID3 assignment.
2	0h RO	**SDI 2 (SDIID2):** This link uses SDI 2. This bit is hard coded per parameter LSDIID2 assignment.
1	1h RO	**SDI 1 (SDIID1):** This link uses SDI 1. This bit is hard coded per parameter LSDIID1 assignment.
0	1h RO	**SDI 0 (SDIID0):** This link uses SDI 0. This bit is hard coded per parameter LSDIID0 assignment.

5.2.400 Link x Per Stream Output Overhead (LPSOO0) - Offset C50h

This register reports the output stream overhead for specific link.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + C50h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO/V	**Per Stream Output Overhead (PSOO):** Indicates the SDO Output Overhead on a per stream basis. This does not include bandwidth used for command and control. This measurement is in byte quantities per 48 kHz frame. Software calculates available link bandwidth in bytes with the following formula: (2 * LOUTPAY) - (NumOfStreams * LPSOO).

5.2.401 Link x Per Stream Input Overhead (LPSIO0) - Offset C52h

This register reports the input stream overhead for specific link.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + C52h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO/V	**Per Stream Input Overhead (PSIO):** Indicates the SDI Input Overhead on a per stream basis. This does not include bandwidth used for response. This measurement is in byte quantities per 48 kHz frame. Software calculates available link bandwidth in bytes with the following formula: (2 * LINPAY) - (NumOfStreams * LPSIO).

5.2.402 Link x Wall Frame Counter (LWALFC0) - Offset C58h

This register reports the wall frame counter for specific link.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + C58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	000000h RO/V	**Frame Number (FN):** 23 bit counter that is incremented when CIF rolls over from 499 to 0. This counter will roll over to zero with a period of approximately 174 seconds.
8:0	000h RO/V	**Clock in Frame (CIF):** 9 bit counter that is incremented on each link BCLK period and rolls over from 499 to 0. This counter will roll over to zero with a period of 48 KHz HD Audio frame. With the introduction of multiple link segments for the Intel HD Audio controller, and the capability of running each link segment at different clock speed, the BCLK definition is fixed at 24 MHz equivalent rate always, independent of the physical link clock speed.

5.2.403 Link x Output Payload Capability (LOUTPAY6M0) - Offset C60h

Link x Output Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + C60h	000Dh

Bit Range	Default & Access	Field Name (ID): Description
15:0	000Dh RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.404 Link x Output Payload Capability (LOUTPAY12M0) - Offset C62h

Link x Output Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + C62h	001Ch

Bit Range	Default & Access	Field Name (ID): Description
15:0	001Ch RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.405 Link x Output Payload Capability (LOUTPAY24M0) - Offset C64h

Link x Output Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + C64h	003Ch

Bit Range	Default & Access	Field Name (ID): Description
15:0	003Ch RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.406 Link x Output Payload Capability (LOUTPAY48M0) - Offset C66h

Link x Output Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + C66h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.407 Link x Output Payload Capability (LOUTPAY96M0) - Offset C68h

Link x Output Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + C68h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.408 Link x Output Payload Capability (LOUTPAY192M0) - Offset C6Ah

Link x Output Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + C6Ah	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.409 Link x Input Payload Capability (LINPAY6M0) - Offset C70h

Link x Input Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + C70h	0005h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0005h RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.410 Link x Input Payload Capability (LINPAY12M0) - Offset C72h

Link x Input Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + C72h	000Dh

Bit Range	Default & Access	Field Name (ID): Description
15:0	000Dh RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.411 Link x Input Payload Capability (LINPAY24M0) - Offset C74h

Link x Input Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + C74h	001Dh

Bit Range	Default & Access	Field Name (ID): Description
15:0	001Dh RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.412 Link x Input Payload Capability (LINPAY48M0) - Offset C76h

Link x Input Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + C76h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.413 Link x Input Payload Capability (LINPAY96M0) - Offset C78h

Link x Input Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + C78h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.414 Link x Input Payload Capability (LINPAY192M0) - Offset C7Ah

Link x Input Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + C7Ah	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.415 Link x Capabilities (LCAP1) - Offset C80h

This register identifies the specific link associated capabilities

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + C80h	0000001Fh

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW/L	**Audio Link Type (ALT):** Indicates which Link Type this link belongs to. 0001-1111 = Reserved 0000 = Intel HD Audio Link Reset value is hard coded to parameter LCAPALT[x*4+3:x*4]. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
27:26	0h RO	**Reserved**
25:24	0h RW/L	**Number of Serial Data Out Signals (NSDO):** 00b indicates that the Intel HD Audio controller supports one Serial Data Output signal. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
23:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/L	**192 MHz Supported (S192):** Indicates 192 MHz clock is supported. Reset value is hard coded to parameter DEFLCAPS192[x]. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
4	1h RW/L	**96 MHz Supported (S96):** Indicates 96 MHz clock is supported. Reset value is hard coded to parameter DEFLCAPS96[x]. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
3	1h RW/L	**48 MHz Supported (S48):** Indicates 48 MHz clock is supported. Reset value is hard coded to parameter DEFLCAPS48[x]. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
2	1h RW/L	**24 MHz Supported (S24):** Indicates 24 MHz clock is supported. Reset value is hard coded to parameter DEFLCAPS24[x]. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
1	1h RW/L	**12 MHz Supported (S12):** Indicates 12 MHz clock is supported. Reset value is hard coded to parameter DEFLCAPS12[x]. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
0	1h RW/L	**6 MHz Supported (S6):** Indicates 6 MHz clock is supported. Reset value is hard coded to parameter DEFLCAPS6[x]. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD

5.2.416 Link x Control (LCTL1) - Offset C84h

Link x Control

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + C84h	00010004h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO/V	**Current Power Active (CPA):** This value changes to the value set by SPA when the power of the link has reached that state. Software sets SPA, then monitors CPA to know when the link has changed state.
22:17	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
16	1h RW	**Set Power Active (SPA):** Software sets this bit to '1' to turn the link on (provided CRSTB = 1), and clears it to '0'when it wishes to turn the link off. When CPA matches the value of this bit, the achieved power state has been reached. Software is expected to wait for CPA to match SPA before the program SPA again. Any deviation may result in undefined behavior.
15:4	0h RO	**Reserved**
3:0	4h RW	**Set Clock Frequency (SCF):** Indicates the frequency that software wishes the link to run at. Changing this value to a value not supported by Link Capabilities shall result in indeterminate results. The possible encodings are: Encoding Frequency 0000 6 MHz 0001 12 MHz 0010 24 MHz 0011 48 MHz 0100 96 MHz 0101 Reserved for 192 MHz 0110-1111 Reserved

5.2.417 Link x Output Stream ID Mapping Valid (LOSIDV1) - Offset C88h

This register maps the output stream connection for specific link.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + C88h	0000FFFEh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	1h RW	**Output Stream ID of 15 is Valid for this Link (L1OSIDV15):** This link will claim / forward output cycles with Stream ID = 1111b.
14	1h RW	**Output Stream ID of 14 is Valid for this Link (L1OSIDV14):** This link will claim / forward output cycles with Stream ID = 1110b.
13	1h RW	**Output Stream ID of 13 is Valid for this Link (L1OSIDV13):** This link will claim / forward output cycles with Stream ID = 1101b.
12	1h RW	**Output Stream ID of 12 is Valid for this Link (L1OSIDV12):** This link will claim / forward output cycles with Stream ID = 1100b.
11	1h RW	**Output Stream ID of 11 is Valid for this Link (L1OSIDV11):** This link will claim / forward output cycles with Stream ID = 1011b.
10	1h RW	**Output Stream ID of 10 is Valid for this Link (L1OSIDV10):** This link will claim / forward output cycles with Stream ID = 1010b.
9	1h RW	**Output Stream ID of 9 is Valid for this Link (L1OSIDV9):** This link will claim / forward output cycles with Stream ID = 1001b.

Bit Range	Default & Access	Field Name (ID): Description
8	1h RW	**Output Stream ID of 8 is Valid for this Link (L1OSIDV8):** This link will claim / forward output cycles with Stream ID = 1000b.
7	1h RW	**Output Stream ID of 7 is Valid for this Link (L1OSIDV7):** This link will claim / forward output cycles with Stream ID = 0111b.
6	1h RW	**Output Stream ID of 6 is Valid for this Link (L1OSIDV6):** This link will claim / forward output cycles with Stream ID = 0110b.
5	1h RW	**Output Stream ID of 5 is Valid for this Link (L1OSIDV5):** This link will claim / forward output cycles with Stream ID = 0101b.
4	1h RW	**Output Stream ID of 4 is Valid for this Link (L1OSIDV4):** This link will claim / forward output cycles with Stream ID = 0100b.
3	1h RW	**Output Stream ID of 3 is Valid for this Link (L1OSIDV3):** This link will claim / forward output cycles with Stream ID = 0011b.
2	1h RW	**Output Stream ID of 2 is Valid for this Link (L1OSIDV2):** This link will claim / forward output cycles with Stream ID = 0010b.
1	1h RW	**Output Stream ID of 1 is Valid for this Link (L1OSIDV1):** This link will claim / forward output cycles with Stream ID = 0001b.
0	0h RO	**Reserved**

5.2.418 Link x SDI Identifier (LSDIID1) - Offset C8Ch

Link x SDI identifier

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + C8Ch	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14	0h RO	**SDI 14 (SDIID14):** This link uses SDI 14. This bit is hard coded per parameter LSDIID14 assignment.
13	0h RO	**SDI 13 (SDIID13):** This link uses SDI 13. This bit is hard coded per parameter LSDIID13 assignment.
12	0h RO	**SDI 12 (SDIID12):** This link uses SDI 12. This bit is hard coded per parameter LSDIID12 assignment.
11	0h RO	**SDI 11 (SDIID11):** This link uses SDI 11. This bit is hard coded per parameter LSDIID11 assignment.
10	0h RO	**SDI 10 (SDIID10):** This link uses SDI 10. This bit is hard coded per parameter LSDIID10 assignment.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**SDI 9 (SDIID9):** This link uses SDI 9. This bit is hard coded per parameter LSDIID9 assignment.
8	0h RO	**SDI 8 (SDIID8):** This link uses SDI 8. This bit is hard coded per parameter LSDIID8 assignment.
7	0h RO	**SDI 7 (SDIID7):** This link uses SDI 7. This bit is hard coded per parameter LSDIID7 assignment.
6	0h RO	**SDI 6 (SDIID6):** This link uses SDI 6. This bit is hard coded per parameter LSDIID6 assignment.
5	0h RO	**SDI 5 (SDIID5):** This link uses SDI 5. This bit is hard coded per parameter LSDIID5 assignment.
4	0h RO	**SDI 4 (SDIID4):** This link uses SDI 4. This bit is hard coded per parameter LSDIID4 assignment.
3	0h RO	**SDI 3 (SDIID3):** This link uses SDI 3. This bit is hard coded per parameter LSDIID3 assignment.
2	1h RO	**SDI 2 (SDIID2):** This link uses SDI 2. This bit is hard coded per parameter LSDIID2 assignment.
1	0h RO	**SDI 1 (SDIID1):** This link uses SDI 1. This bit is hard coded per parameter LSDIID1 assignment.
0	0h RO	**SDI 0 (SDIID0):** This link uses SDI 0. This bit is hard coded per parameter LSDIID0 assignment.

5.2.419 Link x Per Stream Output Overhead (LPSOO1) - Offset C90h

This register reports the output stream overhead for specific link.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + C90h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO/V	**Per Stream Output Overhead (PSOO):** Indicates the SDO Output Overhead on a per stream basis. This does not include bandwidth used for command and control. This measurement is in byte quantities per 48 kHz frame. Software calculates available link bandwidth in bytes with the following formula: (2 * LOUTPAY) - (NumOfStreams * LPSOO).

5.2.420 Link x Per Stream Input Overhead (LPSIO1) - Offset C92h

This register reports the input stream overhead for specific link.

Type	Size	Offset	Default
MMIO	8 bit	HDA BAR + C92h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO/V	**Per Stream Input Overhead (PSIO):** Indicates the SDI Input Overhead on a per stream basis. This does not include bandwidth used for response. This measurement is in byte quantities per 48 kHz frame. Software calculates available link bandwidth in bytes with the following formula: (2 * LINPAY) - (NumOfStreams * LPSIO).

5.2.421 Link x Wall Frame Counter (LWALFC1) - Offset C98h

This register reports the wall frame counter for specific link.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + C98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	000000h RO/V	**Frame Number (FN):** 23 bit counter that is incremented when CIF rolls over from 499 to 0. This counter will roll over to zero with a period of approximately 174 seconds.
8:0	000h RO/V	**Clock in Frame (CIF):** 9 bit counter that is incremented on each link BCLK period and rolls over from 499 to 0. This counter will roll over to zero with a period of 48 KHz HD Audio frame. With the introduction of multiple link segments for the Intel HD Audio controller, and the capability of running each link segment at different clock speed, the BCLK definition is fixed at 24 MHz equivalent rate always, independent of the physical link clock speed.

5.2.422 Link x Output Payload Capability (LOUTPAY6M1) - Offset CA0h

Link x Output Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + CA0h	0003h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0003h RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.423 Link x Output Payload Capability (LOUTPAY12M1) - Offset CA2h

Link x Output Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + CA2h	000Bh

Bit Range	Default & Access	Field Name (ID): Description
15:0	000Bh RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.424 Link x Output Payload Capability (LOUTPAY24M1) - Offset CA4h

Link x Output Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + CA4h	001Ah

Bit Range	Default & Access	Field Name (ID): Description
15:0	001Ah RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.425 Link x Output Payload Capability (LOUTPAY48M1) - Offset CA6h

Link x Output Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + CA6h	0038h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0038h RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.426 Link x Output Payload Capability (LOUTPAY96M1) - Offset CA8h

Link x Output Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + CA8h	0074h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0074h RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.427 Link x Output Payload Capability (LOUTPAY192M1) - Offset CAAh

Link x Output Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + CAAh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nettoutput bandwidth before deciding whether to switch frequency.

5.2.428 Link x Input Payload Capability (LINPAY6M1) - Offset CB0h

Link x Input Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + CB0h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.429 Link x Input Payload Capability (LINPAY12M1) - Offset CB2h

Link x Input Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + CB2h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.430 Link x Input Payload Capability (LINPAY24M1) - Offset CB4h

Link x Input Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + CB4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.431 Link x Input Payload Capability (LINPAY48M1) - Offset CB6h

Link x Input Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + CB6h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.432 Link x Input Payload Capability (LINPAY96M1) - Offset CB8h

Link x Input Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + CB8h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.433 Link x Input Payload Capability (LINPAY192M1) - Offset CBAh

Link x Input Payload Capability

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + CBAh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Offset Frequency Encoding Frequency 40h+(40h*x) + 20h[15:0] 6 MHz 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz 40h+(40h*x) + 22h[15:0] 12 MHz 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz 40h+(40h*x) + 24h[15:0] 24 MHz 40h+(40h*x) + 26h[15:0] Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential nett output bandwidth before deciding whether to switch frequency.

5.2.434 DMA Resume Capability Header (DRSMCH) - Offset 1F00h

This register resides in Primary well (always on), or resides in Primary well (gated-controller) with state retention, and reset by platform reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1F00h	00050700h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW/L	**Capability Version (VER):** This field is an Intel HD Audio Specification defined version number that indicates the version of the capability structure present. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
27:16	005h RW/L	**Capability Identifier (ID):** This field is an Intel HD Audio Specification defined ID number that indicates the nature and format of the capability. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD
15:0	0700h RW/L	**Next Capability Pointer (PTR):** This field contains the offset to the next capability structure or 000h if no other items exist in the linked list of capabilities. Point to SW position based FIFO capability. Locked when FNCFG.BCLD = 1. **Locked by:** SBPR.FNCFG.BCLD

5.2.435 DMA Resume Control (DRSMCTL) - Offset 1F04h

The number of RSM bits in this register is depending on the total number of streams DMA implemented,

represented as x in the register table. The x value is determined by the parameter equation: HSTISC + HSTOSC.

For SPT implementation, x = 16.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1F04h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/1S/V	**RSM:** This field is an Intel HD Audio Specification defined version number that indicates the version of the capability structure present. Locked when FNCFG.BCLD = 1.

5.2.436 DMA Position in Buffer Resume (ISD0DPIBR) - Offset 1F08h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1F08h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.437 DMA Position in Buffer Resume (ISD1DPIBR) - Offset 1F10h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1F10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.438 DMA Position in Buffer Resume (ISD2DPIBR) - Offset 1F18h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1F18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.439 DMA Position in Buffer Resume (ISD3DPIBR) - Offset 1F20h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1F20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.440 DMA Position in Buffer Resume (ISD4DPIBR) - Offset 1F28h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1F28h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.441 DMA Position in Buffer Resume (ISD5DPIBR) - Offset 1F30h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1F30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.442 DMA Position in Buffer Resume (ISD6DPIBR) - Offset 1F38h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1F38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.443 DMA Position in Buffer Resume (OSD0DPIBR) - Offset 1F40h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1F40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.444 DMA Position in Buffer Resume (OSD1DPIBR) - Offset 1F48h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1F48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.445 DMA Position in Buffer Resume (OSD2DPIBR) - Offset 1F50h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1F50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.446 DMA Position in Buffer Resume (OSD3DPIBR) - Offset 1F58h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1F58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.447 DMA Position in Buffer Resume (OSD4DPIBR) - Offset 1F60h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1F60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.448 DMA Position in Buffer Resume (OSD5DPIBR) - Offset 1F68h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1F68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.449 DMA Position in Buffer Resume (OSD6DPIBR) - Offset 1F70h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1F70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.450 DMA Position in Buffer Resume (OSD7DPIBR) - Offset 1F78h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1F78h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.451 DMA Position in Buffer Resume (OSD8DPIBR) - Offset 1F80h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1F80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.452 DMA Position in Buffer Resume (ISD7DPIBR) - Offset 1F88h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1F88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.453 DMA Position in Buffer Resume (ISD8DPIBR) - Offset 1F90h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1F90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.454 DMA Position in Buffer Resume (ISD9DPIBR) - Offset 1F98h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1F98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.455 DMA Position in Buffer Resume (ISD10DPIBR) - Offset 1FA0h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1FA0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.456 DMA Position in Buffer Resume (ISD11DPIBR) - Offset 1FA8h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1FA8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.457 DMA Position in Buffer Resume (ISD12DPIBR) - Offset 1FB0h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1FB0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.458 DMA Position in Buffer Resume (ISD13DPIBR) - Offset 1FB8h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1FB8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.459 DMA Position in Buffer Resume (ISD14DPIBR) - Offset 1FC0h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1FC0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.460 DMA Position in Buffer Resume (OSD9DPIBR) - Offset 1FC8h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1FC8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.461 DMA Position in Buffer Resume (OSD10DPIBR) - Offset 1FD0h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1FD0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.462 DMA Position in Buffer Resume (OSD11DPIBR) - Offset 1FD8h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1FD8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.463 DMA Position in Buffer Resume (OSD12DPIBR) - Offset 1FE0h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1FE0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.464 DMA Position in Buffer Resume (OSD13DPIBR) - Offset 1FE8h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1FE8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.465 DMA Position in Buffer Resume (OSD14DPIBR) - Offset 1FF0h

This register specifies the DPIB resume position.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 1FF0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

5.2.466 Wall Clock Alias (WLCLKA) - Offset 2030h

This register is shadowed from the WALCLK register. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 2030h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Wall Clock Counter Alias (WALCLK):** This is an alias of the WALCK register. 32 bit counter that is incremented on each link BCLK period and rolls over from FFFF_FFFFh to0000_0000h. This counter will roll over to zero with a period of approximately 179 seconds. This counter is enabled while the BCLK bit is set to 1. Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset. With the introduction of multiple link segments for the Intel HD Audio controller, and the capability of running each link segment at different clock speed, the BCLK definition for this counter is fixed at 24 MHz equivalent rate always, independent of the physical link clock speed, and reports the link 0 wall clock value.

5.2.467 Input Stream Descriptor 0 Link Position in Buffer Alias (ISD0LPIBA) - Offset 2084h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 2084h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.468 Input Stream Descriptor 0 Link Position in Buffer Alias (ISD1LPIBA) - Offset 20A4h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 20A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.469 Input Stream Descriptor 0 Link Position in Buffer Alias (ISD2LPIBA) - Offset 20C4h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 20C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.470 Input Stream Descriptor 0 Link Position in Buffer Alias (ISD3LPIBA) - Offset 20E4h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 20E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.471 Input Stream Descriptor 0 Link Position in Buffer Alias (ISD4LPIBA) - Offset 2104h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 2104h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.472 Input Stream Descriptor 0 Link Position in Buffer Alias (ISD5LPIBA) - Offset 2124h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 2124h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.473 Input Stream Descriptor 0 Link Position in Buffer Alias (ISD6LPIBA) - Offset 2144h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 2144h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.474 Input Stream Descriptor 0 Link Position in Buffer Alias (OSD0LPIBA) - Offset 2164h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 2164h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.475 Input Stream Descriptor 0 Link Position in Buffer Alias (OSD1LPIBA) - Offset 2184h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 2184h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.476 Input Stream Descriptor 0 Link Position in Buffer Alias (OSD2LPIBA) - Offset 21A4h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 21A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.477 Input Stream Descriptor 0 Link Position in Buffer Alias (OSD3LPIBA) - Offset 21C4h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 21C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.478 Input Stream Descriptor 0 Link Position in Buffer Alias (OSD4LPIBA) - Offset 21E4h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 21E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.479 Input Stream Descriptor 0 Link Position in Buffer Alias (OSD5LPIBA) - Offset 2204h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 2204h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.480 Input Stream Descriptor 0 Link Position in Buffer Alias (OSD6LPIBA) - Offset 2224h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 2224h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.481 Input Stream Descriptor 0 Link Position in Buffer Alias (OSD7LPIBA) - Offset 2244h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 2244h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.482 Input Stream Descriptor 0 Link Position in Buffer Alias (OSD8LPIBA) - Offset 2264h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 2264h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.483 Input Stream Descriptor 0 Link Position in Buffer Alias (ISD7LPIBA) - Offset 2284h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 2284h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.484 Input Stream Descriptor 0 Link Position in Buffer Alias (ISD8LPIBA) - Offset 22A4h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 22A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.485 Input Stream Descriptor 0 Link Position in Buffer Alias (ISD9LPIBA) - Offset 22C4h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 22C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.486 Input Stream Descriptor 0 Link Position in Buffer Alias (ISD10LPIBA) - Offset 22E4h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 22E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.487 Input Stream Descriptor 0 Link Position in Buffer Alias (ISD11LPIBA) - Offset 2304h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 2304h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.488 Input Stream Descriptor 0 Link Position in Buffer Alias (ISD12LPIBA) - Offset 2324h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 2324h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.489 Input Stream Descriptor 0 Link Position in Buffer Alias (ISD13LPIBA) - Offset 2344h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 2344h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.490 Input Stream Descriptor 0 Link Position in Buffer Alias (ISD14LPIBA) - Offset 2364h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 2364h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.491 Input Stream Descriptor 0 Link Position in Buffer Alias (OSD9LPIBA) - Offset 2384h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 2384h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.492 Input Stream Descriptor 0 Link Position in Buffer Alias (OSD10LPIBA) - Offset 23A4h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 23A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.493 Input Stream Descriptor 0 Link Position in Buffer Alias (OSD11LPIBA) - Offset 23C4h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 23C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.494 Input Stream Descriptor 0 Link Position in Buffer Alias (OSD12LPIBA) - Offset 23E4h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 23E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.495 Input Stream Descriptor 0 Link Position in Buffer Alias (OSD13LPIBA) - Offset 2404h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 2404h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.496 Input Stream Descriptor 0 Link Position in Buffer Alias (OSD14LPIBA) - Offset 2424h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Refer to the corresponding section for details of the register.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 2424h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

5.2.497 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC7LLPL) - Offset 4A10h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.498 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC7LLPU) - Offset 4A14h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.499 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC7LDPL) - Offset 4A18h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.500 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC7LDPU) - Offset 4A1Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.501 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC8LLPL) - Offset 4A20h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.502 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC8LLPU) - Offset 4A24h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A24h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.503 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC8LDPL) - Offset 4A28h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A28h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.504 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC8LDPU) - Offset 4A2Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.505 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC9LLPL) - Offset 4A30h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.506 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC9LLPU) - Offset 4A34h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.507 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC9LDPL) - Offset 4A38h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.508 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC9LDPU) - Offset 4A3Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.509 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC10LLPL) - Offset 4A40h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.510 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC10LLPU) - Offset 4A44h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A44h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.511 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC10LDPL) - Offset 4A48h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.512 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC10LDPU) - Offset 4A4Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A4Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.513 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC11LLPL) - Offset 4A50h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.514 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC11LLPU) - Offset 4A54h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A54h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.515 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC11LDPL) - Offset 4A58h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.516 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC11LDPU) - Offset 4A5Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A5Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.517 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC12LLPL) - Offset 4A60h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.518 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC12LLPU) - Offset 4A64h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.519 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC12LDPL) - Offset 4A68h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.520 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC12LDPU) - Offset 4A6Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A6Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.521 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC13LLPL) - Offset 4A70h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.522 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC13LLPU) - Offset 4A74h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A74h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.523 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC13LDPL) - Offset 4A78h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A78h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.524 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC13LDPU) - Offset 4A7Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A7Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.525 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC14LLPL) - Offset 4A80h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.526 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC14LLPU) - Offset 4A84h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.527 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC14LDPL) - Offset 4A88h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.528 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC14LDPU) - Offset 4A8Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A8Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.529 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC9LLPL) - Offset 4A90h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.530 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC9LLPU) - Offset 4A94h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.531 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC9LDPL) - Offset 4A98h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.532 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC9LDPU) - Offset 4A9Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4A9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.533 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC10LLPL) - Offset 4AA0h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4AA0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.534 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC10LLPU) - Offset 4AA4h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4AA4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.535 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC10LDPL) - Offset 4AA8h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4AA8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.536 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC10LDPU) - Offset 4AACh

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4AACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.537 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC11LLPL) - Offset 4AB0h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4AB0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.538 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC11LLPU) - Offset 4AB4h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4AB4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.539 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC11LDPL) - Offset 4AB8h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4AB8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.540 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC11LDPU) - Offset 4ABCh

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4ABCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.541 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC12LLPL) - Offset 4AC0h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4AC0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.542 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC12LLPU) - Offset 4AC4h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4AC4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.543 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC12LDPL) - Offset 4AC8h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4AC8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.544 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC12LDPU) - Offset 4ACCh

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4ACCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.545 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC13LLPL) - Offset 4AD0h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4AD0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.546 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC13LLPU) - Offset 4AD4h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4AD4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.547 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC13LDPL) - Offset 4AD8h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4AD8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.548 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC13LDPU) - Offset 4ADCh

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4ADCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.549 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC14LLPL) - Offset 4AE0h

This register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe.

This register provides the status of the processing pipe operation.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4AE0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.550 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC14LLPU) - Offset 4AE4h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4AE4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.551 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC14LDPL) - Offset 4AE8h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4AE8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.552 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC14LDPU) - Offset 4AECh

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4AECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.553 Input/Output Processing Pipe's Link Connection x Control (IPPLC7CTL) - Offset 4AF0h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4AF0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when t he DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.554 Input/Output Processing Pipe's Link Connection x Format (IPPLC7FMT) - Offset 4AF4h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 4AF4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.555 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC7LLPL) - Offset 4AF8h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4AF8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.556 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC7LLPU) - Offset 4AFCh

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4AFCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.557 Input/Output Processing Pipe's Link Connection x Control (IPPLC8CTL) - Offset 4B00h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B00h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.558 Input/Output Processing Pipe's Link Connection x Format (IPPLC8FMT) - Offset 4B04h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 4B04h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.559 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC8LLPL) - Offset 4B08h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B08h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.560 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC8LLPU) - Offset 4B0Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B0Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.561 Input/Output Processing Pipe's Link Connection x Control (IPPLC9CTL) - Offset 4B10h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.562 Input/Output Processing Pipe's Link Connection x Format (IPPLC9FMT) - Offset 4B14h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 4B14h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.563 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC9LLPL) - Offset 4B18h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.564 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC9LLPU) - Offset 4B1Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.565 Input/Output Processing Pipe's Link Connection x Control (IPPLC10CTL) - Offset 4B20h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.566 Input/Output Processing Pipe's Link Connection x Format (IPPLC10FMT) - Offset 4B24h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 4B24h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.567 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC10LLPL) - Offset 4B28h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B28h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.568 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC10LLPU) - Offset 4B2Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.569 Input/Output Processing Pipe's Link Connection x Control (IPPLC11CTL) - Offset 4B30h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.570 Input/Output Processing Pipe's Link Connection x Format (IPPLC11FMT) - Offset 4B34h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 4B34h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.571 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC11LLPL) - Offset 4B38h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.572 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC11LLPU) - Offset 4B3Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.573 Input/Output Processing Pipe's Link Connection x Control (IPPLC12CTL) - Offset 4B40h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.574 Input/Output Processing Pipe's Link Connection x Format (IPPLC12FMT) - Offset 4B44h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 4B44h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.575 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC12LLPL) - Offset 4B48h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.576 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC12LLPU) - Offset 4B4Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B4Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.577 Input/Output Processing Pipe's Link Connection x Control (IPPLC13CTL) - Offset 4B50h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.578 Input/Output Processing Pipe's Link Connection x Format (IPPLC13FMT) - Offset 4B54h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 4B54h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.579 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC13LLPL) - Offset 4B58h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.580 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC13LLPU) - Offset 4B5Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B5Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.581 Input/Output Processing Pipe's Link Connection x Control (IPPLC14CTL) - Offset 4B60h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.582 Input/Output Processing Pipe's Link Connection x Format (IPPLC14FMT) - Offset 4B64h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 4B64h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.583 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC14LLPL) - Offset 4B68h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.584 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC14LLPU) - Offset 4B6Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B6Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.585 Input/Output Processing Pipe's Link Connection x Control (OPPLC9CTL) - Offset 4B70h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.586 Input/Output Processing Pipe's Link Connection x Format (OPPLC9FMT) - Offset 4B74h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 4B74h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.587 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC9LLPL) - Offset 4B78h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B78h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.588 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC9LLPU) - Offset 4B7Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B7Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.589 Input/Output Processing Pipe's Link Connection x Control (OPPLC10CTL) - Offset 4B80h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.590 Input/Output Processing Pipe's Link Connection x Format (OPPLC10FMT) - Offset 4B84h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 4B84h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.591 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC10LLPL) - Offset 4B88h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.592 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC10LLPU) - Offset 4B8Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B8Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.593 Input/Output Processing Pipe's Link Connection x Control (OPPLC11CTL) - Offset 4B90h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.594 Input/Output Processing Pipe's Link Connection x Format (OPPLC11FMT) - Offset 4B94h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 4B94h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.595 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC11LLPL) - Offset 4B98h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.596 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC11LLPU) - Offset 4B9Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4B9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.597 Input/Output Processing Pipe's Link Connection x Control (OPPLC12CTL) - Offset 4BA0h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4BA0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.598 Input/Output Processing Pipe's Link Connection x Format (OPPLC12FMT) - Offset 4BA4h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 4BA4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.599 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC12LLPL) - Offset 4BA8h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4BA8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.600 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC12LLPU) - Offset 4BACh

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4BACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.601 Input/Output Processing Pipe's Link Connection x Control (OPPLC13CTL) - Offset 4BB0h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4BB0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.602 Input/Output Processing Pipe's Link Connection x Format (OPPLC13FMT) - Offset 4BB4h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 4BB4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.603 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC13LLPL) - Offset 4BB8h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4BB8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.604 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC13LLPU) - Offset 4BBCh

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4BBCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.605 Input/Output Processing Pipe's Link Connection x Control (OPPLC14CTL) - Offset 4BC0h

SRST bit is not affected by stream reset.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4BC0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	**Reserved**
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.606 Input/Output Processing Pipe's Link Connection x Format (OPPLC14FMT) - Offset 4BC4h

This register specifies the audio format on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	16 bit	HDA BAR + 4BC4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.607 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC14LLPL) - Offset 4BC8h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4BC8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.608 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC14LLPU) - Offset 4BCCh

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

Type	Size	Offset	Default
MMIO	32 bit	HDA BAR + 4BCCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become Referread only until SRST occurs.

5.3 cAVS PCR Registers Summary

Table 5-3. Summary of cAVS PCR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
530h	4	Function Configuration (FNCFG)	0000002Ah

5.3.1 Function Configuration (FNCFG) - Offset 530h

This register is for configuring the Intel HD Audio subsystem behavior as a device function in SOC.

If FUSVAL.ADSPD = 1, HW should treat ADSPD bit = 1.

If FUSVAL.CGD = 1, HW should treat CGD bit = 1.

Type	Size	Offset	Default
MMIO	32 bit	FDD70000h + 530h	0000002Ah

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	1h RW	**Power Gating Disable (PGDIS):** When cleared, it allows power gating to take place per their associated enable and idle conditions. When set, it globally disables all power gating.
4	0h RW/O/L	**BIOS Configuration Lock Down (BCLD):** BIOS Configuration Lock Down (BCLD): When set, it indicates BIOS configuration is done and ready for operations. It also locks down related RW/L bits. **Locked by:** FNCFG.BCLD
3	1h RW	**Clock Gating Disable (CGD):** Clock Gating Disabled (CGD): When cleared, it allows local / dynamic clock gating and trunk clock gating to take place per their associated enable and idle conditions. When set, it globally disables all clock gating.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/L	**Audio DSP Disable (ADSPD):** Audio DSP Disable (ADSPD): When set, the Audio DSP is disabled and all register access associated with Audio DSP are treated as unsupported request, and return UR response if it is non-posted cycle. This bit does not affect cycles from IOSF Sideband Interface. Locked when FNCFG.BCLD = 1. **Locked by:** FNCFG.BCLD
1	1h RW/L	**HD Audio Subsystem as PCI Device (HDASPCID):** HD Audio Subsystem as PCI Device (HDASPCID): When this bit is set to 1, the Intel HD Audio subsystem will appear as a PCI device to SW. When this bit is 0, the Intel HD Audio subsystem will appear as a PCI-Express device to SW. Locked when FNCFG.BCLD = 1. **Locked by:** FNCFG.BCLD
0	0h RW/L	**HD Audio Subsystem Disable (HDASD):** HD Audio Subsystem Disable (HDASD): When set, the Intel HD Audio subsystem (including Audio DSP) is disabled and all register access are treated as unsupported request, and return UR response if it is non-posted cycle. This bit does not affect cycles from IOSF Sideband Interface. Locked when FNCFG.BCLD = 1. **Locked by:** FNCFG.BCLD

6 System Management Bus (SMBus) Controller

6.1 SMBus Configuration Registers Summary

This chapter documents the registers in Bus: 0, Device 31, Function 4.

Table 6-1. Summary of Bus: 0, Device: 31, Function: 4 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	Vendor ID (VID)	8086h
2h	2	Device ID (DID)	4B23h
4h	2	Command Register (CMD)	0000h
6h	2	Device Status (DS)	0280h
8h	1	Revision ID (RID)	00h
9h	1	Programming Interface (PI)	00h
Ah	1	Sub Class Code (SCC)	05h
Bh	1	Base Class Code (BCC)	0Ch
10h	4	SMBus Memory Base Address_31_0 (SMBMBAR_31_0)	00000004h
14h	4	SMBus Memory Base Address_63_32 (SMBMBAR_63_32)	00000000h
20h	4	SMB Base Address (SBA)	00000001h
2Ch	2	Subsystem Vendor Identifiers (SVID)	0000h
2Eh	2	Subsystem Identifiers (SID)	0000h
3Ch	1	Interrupt Line (INTLN)	00h
3Dh	1	Interrupt Pin (INTPN)	01h
40h	1	Host Configuration (HCFG)	00h
50h	4	TCO Base Address (TCOBASE)	00000001h
54h	4	TCO Control (TCOCTL)	00000000h
90h	4	SAI IOSF Primary Access Control Policy (SAIPRIAC0)	01210000h
94h	4	SAI IOSF Primary Access Control Policy (SAIPRIAC1)	00000C00h
98h	4	SAI IOSF Primary Read/Write Policy (SAIPRIRW0)	0120001Fh
9Ch	4	SAI IOSF Primary Read/Write Policy (SAIPRIRW1)	00000E00h
F0h	4	Unsupported Request Error Status (URES)	00000000h
F4h	4	Unsupported Request Error Control (UREC)	00000000h
F8h	4	Manufacturer's ID (MANID)	08000F80h

6.1.1 Vendor ID (VID) - Offset 0h

Vendor ID

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:4] + 0h	8086h

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**Vendor ID (VID):** Value indicates Intel as the vendor

6.1.2 Device ID (DID) - Offset 2h

Device ID

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:4] + 2h	4B23h

Bit Range	Default & Access	Field Name (ID): Description
15:0	4B23h RO/V	**Device ID (DID):** Indicates the device number assigned by the SIG.

6.1.3 Command Register (CMD) - Offset 4h

Command Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:4] + 4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable (INTD):** 1 = Disables SMBus to assert its PIRQB# signal. Defaults to 0.
9	0h RO	**Fast Back to Back Enable (FBE):** Reserved
8	0h RW	**SERR# Enable (SERRE):** 1 = Enables SERR# generation
7	0h RO	**Wait Cycle Control (WCC):** Reserved
6	0h RW	**Parity Error Response (PER):** 1 = Sets Detected Parity Error bit when parity error is detected
5	0h RO	**VGA Palette Snoop (VGAPS):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**Postable Memory Write Enable (PMWE):** Reserved
3	0h RO	**Special Cycle Enable (SCE):** Reserved
2	0h RO	**Bus Master Enable (BME):** Reserved
1	0h RW	**Memory Space Enable (MSE):** 1= Enables memory mapped configuration space.
0	0h RW	**I/O Space Enable (IOSE):** 1= enables access to the SM Bus I/O space registers as defined by the Base Address Register.

6.1.4 Device Status (DS) - Offset 6h

Device Status

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:4] + 6h	0280h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**Detected Parity Error (DPE):** Detected Parity Error
14	0h RW/1C	**Signaled System Error (SSE):** Signaled System Error
13	0h RO	**Received Master Abort (RMA):** Reserved
12	0h RO	**Received Target Abort (RTA):** Reserved
11	0h RW/1C	**Signaled Target-Abort Status (STA):** Reserved
10:9	1h RO	**DEVSEL# Timing Status (DEVT):** This 2-bit field defines the timing for DEVSEL# assertion. These read only bits indicate the Intel PCH's DEVSEL# timing when performing a positive decode. Note: Intel PCH generates DEVSEL# with medium time. Note: It is not clear if a PCI master can write to SMBus controller.
8	0h RO	**Data Parity Error Detected (DPED):** Reserved
7	1h RO	**Fast Back-to-Back Capable (FBC):** Reserved
6	0h RO	**User Definable Features (UDF):** Reserved
5	0h RO	**66 MHz Capable (C_66M):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**Capabilities List Indicator (CLI):** Hardwired to 0 because there are no capability list structures in this function.
3	0h RO	**Interrupt Status (INTS):** This bit indicates that an interrupt is pending. It is independent from the state of the Interrupt Enable bit in the command register.
2:0	0h RO	**Reserved**

6.1.5 Revision ID (RID) - Offset 8h

Revision ID

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:31, F:4] + 8h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Revision ID (RID):** The value reported in this register depends on the global revision ID for the PCH.

6.1.6 Programming Interface (PI) - Offset 9h

Programming Interface

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:31, F:4] + 9h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Programming Interface (PI):** No programming interface defined.

6.1.7 Sub Class Code (SCC) - Offset Ah

Sub Class Code

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:31, F:4] + Ah	05h

Bit Range	Default & Access	Field Name (ID): Description
7:0	05h RO	**Sub Class Code (SCC):** A value of 05h indicates that this device is a SM Bus serial controller.

6.1.8 Base Class Code (BCC) - Offset Bh

Base Class Code

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:31, F:4] + Bh	0Ch

Bit Range	Default & Access	Field Name (ID): Description
7:0	0Ch RO	**Base Class Code (BCC):** A value of 0Ch indicates that this device is a serial controller.

6.1.9 SMBus Memory Base Address_31_0 (SMBMBAR_31_0) - Offset 10h

SMBus Memory Base Address_31_0

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:4] + 10h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RW	**Base Address (BA):** Provides the 32 byte system memory base address for the Intel PCH SMB logic.
7:4	0h RO	**HARDWIRED_0:** Hardwired to 0.
3	0h RO	**PREF:** Hardwired to 0. Indicated that SMBMBAR is not pre- fetch-able
2:1	2h RO	**Address Range (ADDRNG):** Indicates that this SMBMBAR can be located anywhere in 64 bit address space
0	0h RO	**Memory Space Indicator (MSI):** Indicates that the SMB logic is memory mapped.

6.1.10 SMBus Memory Base Address_63_32 (SMBMBAR_63_32) - Offset 14h

SMBus Memory Base Address_63_32

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:4] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address (BA):** Bits 63-32 of SMBus Memory Base Address

6.1.11 SMB Base Address (SBA) - Offset 20h

SMB Base Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:4] + 20h	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:5	000h RW	**Base Address (BA):** Provides the 32 byte t system I/O base address for the SMB logic.
4:1	0h RO	**Reserved**
0	1h RO	**IO Space Indicator (IOSI):** This read-only bit always is 1, indicating that the SMB logic is I/O mapped.

6.1.12 Subsystem Vendor Identifiers (SVID) - Offset 2Ch

Subsystem Vendor ID

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:4] + 2Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/O	**Subsystem Vendor ID (SVID):** BIOS sets the value in this register to identify the Subsystem Vendor ID. The SMBus SVID register, in combination with the SMBus Subsystem ID register, enables the operating system to distinguish each subsystem from the others. Note: The software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

6.1.13 Subsystem Identifiers (SID) - Offset 2Eh

Subsystem ID

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:31, F:4] + 2Eh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/O	**Subsystem ID (SID):** BIOS can write to this register to identify the Subsystem ID. The SID register, in combination with the SVID, enable the operating system to distinguish each subsystem from other(s). Note: The software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

6.1.14 Interrupt Line (INTLN) - Offset 3Ch

Interrupt Line

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:31, F:4] + 3Ch	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Interrupt Line (INTLN):** This data is not used by the hardware. It is to communicate to software the interrupt line that the interrupt pin is connected to PIRQB#.

6.1.15 Interrupt Pin (INTPN) - Offset 3Dh

Interrupt Pin

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:31, F:4] + 3Dh	01h

Bit Range	Default & Access	Field Name (ID): Description
7:0	01h RW/O	**Interrupt Pin (INTPN):** This defines the interrupt pin to be used by the SMBus controller. Bits: Pins 0h: No Interrupt 1h: INTA# 2h: INTB# 3h: INTC# 4h: INTD# 5h-Fh: Reserved

6.1.16 Host Configuration (HCFG) - Offset 40h

Host Configuration

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:31, F:4] + 40h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Reserved**
4	0h RW/1L	**SPD Write Disable (SPDWD):** This bit must be set to '1' to disable writes to SPD which are on Host SMB address ranges A0h - AEh. The SMBus range is unwriteable until next platform reset. HW Default is '0.' **Note:** This bit is RW O and will be reset on PLTRST# reset. This should be set by BIOS memory reference code to '1'. SW can only program this bit when both HCTL(6) = 0 (START) and HSTS(0) = 0 (HBSY), else it may result in an undefined behavior. [Noted in HSTS.HBSY that states "No SMB registers should be accessed while HSTS.HBSY bit is set, the same will apply to SPD write disable. 3 RW 0 SSRESET: Soft SMBUS Reset: When this bit is 1,
3	0h RW	**SSRESET:** Soft SMBUS Reset: When this bit is 1, the SMBus state machine and logic in PCH is reset. The HW will reset this bit to 0 when reset operation is completed.
2	0h RW	**I2CEN:** When this bit is 1, the Intel PCH is enabled to communicate with I2C devices. This will change the formatting of some commands. When this bit is 0, behavior is for SMBus.
1	0h RW	**SSEN:** When this bit is set, any source of an SMB interrupt will instead be routed to generate an SMI#.
0	0h RW	**HSTEN:** When set, the SMB Host Controller interface is enabled to execute commands. The HST_INT_EN bit needs to be enabled in order for the SMB Host Controller to interrupt or SMI#. Additionally, the SMB Host Controller will not respond to any new requests until all interrupt requests have been cleared.

6.1.17 TCO Base Address (TCOBASE) - Offset 50h

TCO Base Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:4] + 50h	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:5	000h RW/L	**TCO Base Address (TCOBA):** When set to 1, this bit locks down the TCO Base Address Register (TCOBASE) at offset 50h. The Base Address Field becomes read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a platform reset. **Locked by:** TCOCTL.TCO_BASE_LOCK
4:1	0h RO	**Reserved**
0	1h RO	**I/O Space (IOS):** Indicates an I/O Space

6.1.18 TCO Control (TCOCTL) - Offset 54h

TCO Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:4] + 54h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**TCO Base Enable (TCO_BASE_EN):** When set, decode of the I/O range pointed to by the TCO base register is enabled.
7:1	0h RO	**Reserved**
0	0h RW/O	**TCO Base Lock (TCO_BASE_LOCK):** When set to 1, this bit locks down the TCO Base Address Register (TCOBASE) at offset 50h. The Base Address Field becomes read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a platform reset.

6.1.19 SAI IOSF Primary Access Control Policy (SAIPRIAC0) - Offset 90h

SAI IOSF Primary Access Control Policy

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:4] + 90h	01210000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	01210000h RW	**SAI IOSF Primary Access Control Policy (SAIPRIAC0):** Bit wise register where each bit represent the 6-bit SAI Index that mapped to a particular 8-bit SAI value or values. A value 1in this register bit means that a IOSF Primary cycle with SAI value that matches the mapped 8-bit SAI value or values has the write access to the SAIPRIAC and SAIPRIRW register. A value 0in this register bit means that a IOSF Primary Cycle with SAI value that does not match the mapped 8-bit SAI value or values has no write access to the SAIPRIAC and SAIPRIRW register. IOSF Primary Cycle to the SAIPRIAC and SAIPRIRW registers always has read access disregard of the value of this register.

6.1.20 SAI IOSF Primary Access Control Policy (SAIPRIAC1) - Offset 94h

SAI IOSF Primary Access Control Policy

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:4] + 94h	00000C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000C00h RW	**SAI IOSF Primary Access Control Policy (SAIPRIAC1):** Bit wise register where each bit represent the 6-bit SAI Index that mapped to a particular 8-bit SAI value or values. A value 1in this register bit means that a IOSF Primary cycle with SAI value that matches the mapped 8-bit SAI value or values has the write access to the SAIPRIAC and SAIPRIRW register. A value 0in this register bit means that a IOSF Primary Cycle with SAI value that does not match the mapped 8-bit SAI value or values has no write access to the SAIPRIAC and SAIPRIRW register. IOSF Primary Cycle to the SAIPRIAC and SAIPRIRW registers always has read access disregard of the value of this register.

6.1.21 SAI IOSF Primary Read/Write Policy (SAIPRIRW0) - Offset 98h

SAI IOSF Primary Read/Write Policy

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:4] + 98h	0120001Fh

Bit Range	Default & Access	Field Name (ID): Description
31:0	0120001Fh RW	**SAI IOSF Primary Read/Write Policy (SAIPRIRW0):** Bit wise register where each bit represent the 6-bit SAI Index that mapped to a particular 8-bit SAI value or values. A value 1 in this register bit means that an IOSF Primary Cycle with SAI value that matches the mapped 8-bit SAI value or values has both the read and write access to the IOSF Primary register space (CFG/MMIO/IO). A value 0iin this register bit means that an IOSF Primary Cycle with SAI value that does not match the mapped 8-bit SAI value or values. So, there is no read and write access to the IOSF Primary register space (CFG/MMIO/IO).

6.1.22 SAI IOSF Primary Read/Write Policy (SAIPRIRW1) - Offset 9Ch

SAI IOSF Primary Read/Write Policy

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:4] + 9Ch	00000E00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000E00h RW	**SAI IOSF Primary Read/Write Policy (SAIPRIRW1):** Bit wise register where each bit represent the 6-bit SAI Index that mapped to a particular 8-bit SAI value or values. A value 1 in this register bit means that an IOSF Primary Cycle with SAI value that matches the mapped 8-bit SAI value or values has both the read and write access to the IOSF Primary register space (CFG/MMIO/IO). A value 0in this register bit means that an IOSF Primary Cycle with SAI value that does not match the mapped 8-bit SAI value or values. So, there is no read and write access to the IOSF Primary register space (CFG/MMIO/IO).

6.1.23 Unsupported Request Error Status (URES) - Offset F0h

This register denotes the status for the unsupported request on IOSF Primary I/F

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:4] + F0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**Unsupported Request Detected (URD):** Set to 1 by hardware upon detecting an Unsupported Request on IOSF Primary interface that is not considered Advisory Non-Fatal. Cleared to 0 by SW. URD bit is only set based on IOSF primary bus interface activity. It is not set based on IOSF sideband bus interface activity.

6.1.24 Unsupported Request Error Control (UREC) - Offset F4h

This register denotes the control for the unsupported request on IOSF Primary I/F

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:4] + F4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**Unsupported Request Reporting Enable (URRE):** If set to 1 by software, it allows reporting of an Unsupported Request as a system error.

6.1.25 Manufacturer's ID (MANID) - Offset F8h

This reflects the value of the Manufacturers ID which provides information on the details of the chip revision.

Implementation Note: A single Manufacturers ID is implemented based on information in the Fuse block and distributed to the devices via a message.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:4] + F8h	08000F80h

Bit Range	Default & Access	Field Name (ID): Description
31:0	08000F80h RO/P	**Manufacturers ID Field (MANID)**: Manufacturer ID: Default value comes from straps

6.2 SMBus Memory Mapped Registers Summary

Table 6-2. Summary of SMBus Memory Mapped Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	1	Host Status Register Address (HSTS)	00h
2h	1	Host Control Register (HCTL)	00h
3h	1	Host Command Register (HCMD)	00h
4h	1	Transmit Slave Address Register (TSA)	00h
5h	1	Data 0 Register (HD0)	00h
6h	1	Data 1 Register (HD1)	00h
7h	1	Host Block Data (HBD)	00h
8h	1	Packet Error Check Data Register (PEC)	00h
9h	1	Receive Slave Address Register (RSA)	44h
Ah	2	Slave Data Register (SD)	0000h
Ch	1	Auxiliary Status (AUXS)	00h
Dh	1	Auxiliary Control (AUXC)	00h
Eh	1	SMLINK_PIN_CTL Register (SMLC)	04h
Fh	1	SMBUS_PIN_CTL Register (SMBC)	04h
10h	1	Slave Status Register (SSTS)	00h
11h	1	Slave Command Register (SCMD)	00h
14h	1	Notify Device Address Register (NDA)	00h
16h	1	Notify Data Low Byte Register (NDLB)	00h
17h	1	Notify Data High Byte Register (NDHB)	00h

6.2.1 Host Status Register Address (HSTS) - Offset 0h

All status bits are set by hardware and cleared by the software writing a one to the particular bit position. Writing a zero to any bit position has no affect.

Type	Size	Offset	Default
MMIO	8 bit	SMBMBAR + 0h	00h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/1C	**BDS:** This bit will be set to 1 when the host controller has received a byte (for Block Read commands) or if it has completed transmission of a byte (for Block Write commands) when the 32-byte buffer is not being used. Note that this bit will be set, even on the last byte of the transfer. Software clears the bit by writing a 1 to the bit position. This bit is not set when transmission is due to the D110 interface heartbeat. This bit has no meaning for block transfers when the 32- byte buffer is enabled. Note: When the last byte of a block message is received, the host controller will set this bit. However, it will not immediately set the INTR bit (bit 1 in this register). When the interrupt handler clears the BYTE_DONE_STS bit, the message is considered complete, and the host controller will then set the INTR bit (and generate another interrupt). Thus, for a block message of n bytes, the Intel PCH will generate n+1 interrupts. The interrupt handler needs to be implemented to handle these cases.
6	0h RW/1C	**In Use Status (IUS):** After a full PCI reset, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the host controller. This bit has no other effect on the hardware, and is only used as semaphore among various independent software threads that may need to use the Intel PCHs SMBus logic.
5	0h RW/1C	**SMSTS:** Intel PCH sets this bit to a 1 to indicates source of the interrupt or SMI# was the SMBAlert# signal. Software resets this bit by writing a 1 to this location. This bit should also be cleared by RSMRST# (but not PLTRST#).
4	0h RW/1C	**FAIL:** When set, this indicates that the source of the interrupt or SMI# was a failed bus transaction. This is set in response to the KILL bit being set to terminate the host transaction.
3	0h RW/1C	**Bus Error (BERR):** When set, this indicates the source of the interrupt or SMI# was a transaction collision.
2	0h RW/1C	**Device Error (DERR):** When set, this indicates that the source of the interrupt or SMI# was due one of the following: Illegal Command Field Unclaimed Cycle (host initiated) Host Device Time-out Error. CRC Error
1	0h RW/1C	**INTR:** When set, this indicates that the source of the interrupt or SMI# was the successful completion of its last command.
0	0h RW/1C	**Host Busy (HBSY):** A 1 indicates that the Intel PCH is running a command from the host interface. No SMB registers should be accessed while this bit is set. Exception: The BLOCK DATA REGISTER can be accessed when this bit is set ONLY when the SMB_CMD bits (in Host control register) are programmed for Block command or I2C Read command. This is necessary in order to check the DONE_STS bit.

6.2.2 Host Control Register (HCTL) - Offset 2h

Note: A read to this register will clear the pointer in the 32-byte buffer.

Type	Size	Offset	Default
MMIO	8 bit	SMBMBAR + 2h	00h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**PEC_EN:** When set to 1, this bit causes the host controller to perform the SMBus transaction with the Packet Error Checking phase appended. For writes, the value of the PEC byte is transferred from the PEC Register. For reads, the PEC byte is loaded in to the PEC Register. When this bit is cleared to 0, the SMBus host controller does not perform the transaction with the PEC phase appended. This bit must be written prior to the write in which the START bit is set.
6	0h RW	**START:** This write-only bit is used to initiate the command described in the SMB_CMD field. All registers should be setup prior to writing a 1 to this bit position. This bit always reads zero. The HOST_BUSY bit in the Host Status register (offset 00h) can be used to identify when the Intel PCH has finished the command.
5	0h RW	**LAST_BYTE:** Used for I2C Read commands as an indication that the next byte will be the last one to be received for that block. The algorithm and usage model for this bit will be as follows (assume a message of n bytes): A. When the software sees the BYTE_DONE_STS bit set (bit 7 in the SMBus Host Status Register) for each of bytes 1 through n-2 of the message, the software should then read the Block Data Byte Register to get the byte that was just received. B. After reading each of bytes 1 to n-2 of the message, the software will then clear the BYTE_DONE_STS bit. C. After receiving byte n-1 of the message, the software will then set the LAST BYTE bit. The software will then clear the BYTE_DONE_STS bit. D. The Intel PCH will then receive the last byte of the message (byte n). However, the Intel PCH state machine will see the LAST BYTE bit set, and instead of sending an ACK after receiving the last byte, it will instead send a NAK. E. After receiving the last byte (byte n), the software will still clear the BYTE_DONE_STS bit. However, the LAST_BYTE bit will be irrelevant at that point. Note: This bit may be set when the TCO timer causes the SECOND_TO_STS bit to be set. See the TCO2_STS Register in Volume 1, bit 1 for more details on that bit. The SMBus device driver should clear the LAST_BYTE bit (if it is set) before starting any new command. Note: In addition to I2C Read Commands, the LAST_BYTE bit will also cause Block Read/Write cycles to stop prematurely (at the end of the next byte).

Bit Range	Default & Access	Field Name (ID): Description
4:2	0h RW	**SMB_CMD:** As shown by the bit encoding below, indicates which command the Intel PCH is to perform. If enabled, the Intel PCH will generate an interrupt or SMI# when the command has completed. If the value is for a non-supported or reserved command, the Intel PCH will set the device error (DEV_ERR) status bit and generate an interrupt when the START bit is set. The Intel PCH will perform no command, and will not operate until DEV_ERR is cleared. Val - Command Description: 000 - Quick: The slave address and read/write value (bit 0) are stored in the tx slave address register. 001 - Byte: This command uses the transmit slave address and command registers. Bit 0 of the slave address register determines if this is a read or write command. 010 - Byte Data: This command uses the transmit slave address, command, and DATA0 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, the DATA0 register will contain the read data. 011 - Word Data: This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, after the command completes the DATA0 and DATA1 registers will contain the read data. 100 - Process Call: This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. After the command completes, the DATA0 and DATA1 registers will contain the read data. 101 - Block: This command uses the transmit slave address, command, and DATA0 registers, and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block reads, the count is received and stored in the DATA0 register. Bit 0 of the slave address register selects if this is a read or write command. For writes, data is retrieved from the first n (where n is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. 110 - I2C Read: This command uses the transmit slave address, command, DATA0, DATA1 registers, and the Block Data Byte register. The read data is stored in the Block Data Byte register. The Intel PCH will continue reading data until the NAK is received. 111 - Block-Process: This command uses the transmit slave address, command, DATA0 and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block read, the count is received and stored in the DATA0 register. Bit 0 of the slave address register always indicate a write command. For writes, data is retrieved from the first m (where m is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. Note: E32B bit in the Auxiliary Control Register must be set for this command to work.
1	0h RW	**KILL:** When set, kills the current host transaction taking place, sets the FAILED status bit, and asserts the interrupt (or SMI#) selected by the SMB_INTRSEL field. This bit, once set, must be cleared to allow the SMB Host Controller to function normally.
0	0h RW	**INTREN:** Enable the generation of an interrupt or SMI# upon the completion of the command.

6.2.3 Host Command Register (HCMD) - Offset 3h

Host Command Register

Type	Size	Offset	Default
MMIO	8 bit	SMBMBAR + 3h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Host Command Register (HCMD):** This eight bit field is transmitted by the host controller in the command field of the SMB protocol during the execution of any command.

6.2.4 Transmit Slave Address Register (TSA) - Offset 4h

This register is transmitted by the host controller in the slave address field of the SMB protocol. This is the address of the target.

Type	Size	Offset	Default
MMIO	8 bit	SMBMBAR + 4h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:1	00h RW	**ADDR:** 7-bit address of the targeted slave. Note: Writes to TSA values of A0h - AEh are blocked depending on the setting of the SPD write disable bit in HCFG - Host Configuration.
0	0h RW	**RW:** Direction of the host transfer. 1 = read, 0 = write

6.2.5 Data 0 Register (HD0) - Offset 5h

Data 0 Register

Type	Size	Offset	Default
MMIO	8 bit	SMBMBAR + 5h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**DATA0_COUNT:** This field contains the eight bit data sent in the DATA0 field of the SMB protocol. For block write commands, this register reflects the number of bytes to transfer. This register should be programmed to a value between 1 and 32 for block counts. A count of 0 or a count above 32 will result in unpredictable behavior. The host controller does not check or log illegal block counts.

6.2.6 Data 1 Register (HD1) - Offset 6h

Data 1 Register

Type	Size	Offset	Default
MMIO	8 bit	SMBMBAR + 6h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**DATA1:** This eight bit register is transmitted in the DATA1 field of the SMB protocol during the execution of any command.

6.2.7 Host Block Data (HBD) - Offset 7h

Host Block Data

Type	Size	Offset	Default
MMIO	8 bit	SMBMBAR + 7h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Block Data (BDTA):** This is either a register, or a pointer into a 32- byte block array, depending upon whether the E32B bit is set in the Auxiliary Control register. When the E32B bit is cleared, this is a register containing a byte of data to be sent on a block write or read from on a block read, just as it behaved on the INTEL PCH. When the E32B bit is set, reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array, which is reset to 0 by reading the HCTL register (offset 02h). The index pointer then increments automatically upon each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0. When the E2B bit is set, for writes, software will write up to 32-bytes to this register as part of the setup for the command. After the Host Controller has sent the Address, Command, and Byte Count fields, it will send the bytes in the SRAM pointed to by this register. When the E2B bit is cleared for writes, software will place a single byte in this register. After the host controller has sent the address, command, and byte count fields, it will send the byte in this register. If there is more data to send, software will write the next series of bytes to the SRAM pointed to by this register and clear the DONE_STS bit. The controller will then send the next byte. During the time between the last byte being transmitted to the next byte being transmitted, the controller will insert wait-states on the interface. When the E2B bit is set for reads, after receiving the byte count into the Data0 register, the first series of data bytes go into the SRAM pointed to by this register. If the byte count has been exhausted or the 32-byte SRAM has been filled, the controller will generate an SMI# or interrupt (depending on configuration) and set the DONE_STS bit. Software will then read the data. During the time between when the last byte is read from the SRAM to when the DONE_STS bit is cleared, the controller will insert wait states on the interface.

6.2.8 Packet Error Check Data Register (PEC) - Offset 8h

Note: This register may reside in either the core well or the suspend well. To simplify the implementation, this register will be in the suspend well with the suspend well version of PCI reset (URST33B).

This register contains the 8-bit CRC value that is used as the Packet Error Check on SMBus. For writes, this register is written by software prior to running the command. For reads, this register is read by software after the read command is completed on SMBus.

Type	Size	Offset	Default
MMIO	8 bit	SMBMBAR + 8h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**PEC_DATA:** This 8-bit register is written with the SMBus PEC data prior to a write transaction. For read transactions, the PEC data is loaded from the SMBus into this register and is then read by software. Software must ensure that the INUSE_STS bit is properly maintained to avoid having this field over-written by a write transaction following a read transaction.

6.2.9 Receive Slave Address Register (RSA) - Offset 9h

Receive Slave Address Register

Type	Size	Offset	Default
MMIO	8 bit	SMBMBAR + 9h	44h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:0	44h RW	**SA_6_0:** This field is the slave address that the Intel PCH decodes for read and write cycles. The default is not 0 so that it can respond even before the CPU comes up (or if the CPU is dead). This register is reset by RSMRST#, but not by PLTRST#.

6.2.10 Slave Data Register (SD) - Offset Ah

Slave Data Register

Type	Size	Offset	Default
MMIO	16 bit	SMBMBAR + Ah	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**SD_15_0:** This field is the 16-bit data value written by the external SMBus master. The CPU can then read the value from this register. This register is reset by RSMRST#, but not by PLTRST#. SLAVE_DATA[7:0] corresponds to the Data Message Byte 0 at Slave Write Register 4 in the table. SLAVE_[15:8] corresponds to the Data Message Byte 1 at Slave Write Register 5 in the table.

6.2.11 Auxiliary Status (AUXS) - Offset Ch

All bits in this register are in the core well.

Type	Size	Offset	Default
MMIO	8 bit	SMBMBAR + Ch	00h

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Reserved**
4	0h RO/V	**SMT3EN:** Register value determines if SMT3 is enabled and connected on SMLink1. Disabled means the device is not connected to the pins 0: Disable 1: Enable
3	0h RO/V	**SMT2EN:** Register value determines if SMT2 is enabled and connected on SMLink0. Disabled means the device is not connected to the pins 0: Disable 1: Enable
2	0h RO/V	**SMT1EN:** Register value determines if SMT1 is enabled and connected on SMBus. Disabled means the device is not connected to the pins 0: Disables 1: Enable
1	0h RO	**Reserved**
0	0h RW/1C	**CRC Error (CRCE):** This bit is set if a received message contained a CRC error. When this bit is set, the DERR bit of the host status register will also be set. This bit will be set by the controller if a software abort occurs in the middle of the CRC portion of the cycle or an abort happens after Intel PCH has received the final data bit transmitted by external slave.

6.2.12 Auxiliary Control (AUXC) - Offset Dh

All bits in this register are in the resume well.

Type	Size	Offset	Default
MMIO	8 bit	SMBMBAR + Dh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW	**Enable 32-byte Buffer (E32B):** When set, the Host Block Data register is a pointer into a 32-byte buffer, as opposed to a single register. This enables the block commands to transfer or receive up to 32-bytes before the Intel PCH generates an interrupt.
0	0h RW	**Automatically Append CRC (AAC):** When set, the Intel PCH will automatically append the CRC. This bit must not be changed during SM Bus transactions, or undetermined behavior will result. It should be programmed only once during the lifetime of the function.

6.2.13 SMLINK_PIN_CTL Register (SMLC) - Offset Eh

Note: This register is in the resume well and is reset by RSMRST#

Type	Size	Offset	Default
MMIO	8 bit	SMBMBAR + Eh	04h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved**
2	1h RW	**SMLINK_CLK_CTL:** 0 = Intel PCH will drive the SMLINK[0] pin low, independent of what the other SMLINK logic would otherwise indicate for the SMLINK(0) pin. 1 = The SMLINK[0] pin is Not overdriven low. The other SMLINK logic controls the state of the pin.
1	0h RO/V	**SMLINK1_CUR_STS:** This bit has a default value that is dependent on an external signal level. This returns the value on the SMLINK[1] pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.
0	0h RO/V	**SMLINK0_CUR_STS:** This bit has a default value that is dependent on an external signal level. This returns the value on the SMLINK[0] pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.

6.2.14 SMBUS_PIN_CTL Register (SMBC) - Offset Fh

Note: This register is in the resume well and is reset by RSMRST#

Type	Size	Offset	Default
MMIO	8 bit	SMBMBAR + Fh	04h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved**
2	1h RW	**SMBCLK_CTL:** 0 = Intel PCH will drive the SMBCLK pin low, independent of what the other SMB logic would otherwise indicate for the SMBCLK pin. 1 = The SMBCLK pin is Not overdriven low. The other SMBus logic controls the state of the pin.
1	0h RO/V	**SMBDATA_CUR_STS:** This bit has a default value that is dependent on an external signal level. This returns the value on the SMBDATA pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.
0	0h RO/V	**SMBCLK_CUR_STS:** This bit has a default value that is dependent on an external signal level. This returns the value on the SMBCLK pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.

6.2.15 Slave Status Register (SSTS) - Offset 10h

All bits in this register are implemented in the 64 kHz clock domain. Therefore, software must poll the register until a write takes effect before assuming that a write has completed internally.

Type	Size	Offset	Default
MMIO	8 bit	SMBMBAR + 10h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	**Reserved**
0	0h RW/1C	**HNS:** The Intel PCH sets this bit to a 1 when it has completely received a successful Host Notify Command on the SMBus pins. Software reads this bit to determine that the source of the interrupt or SMI# was the reception of the Host Notify Command. Software clears this bit after reading any information needed from the Notify address and data registers by writing a 1 to this bit. Note that the Intel PCH will allow the Notify Address and Data registers to be over-written once this bit has been cleared. When this bit is 1, the Intel PCH will NACK the first byte (host address) of any new Host Notify commands on the SMBus. Writing a 0 to this bit has no effect.

6.2.16 Slave Command Register (SCMD) - Offset 11h

All bits in this register are implemented in the 64 kHz clock domain. Therefore, software must poll the register until a write takes effect before assuming that a write has completed internally. Also, software must confirm the prior written value before writing to the register again.

Type	Size	Offset	Default
MMIO	8 bit	SMBMBAR + 11h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved**
2	0h RW	**SMB_D:** Software sets this bit to 1 to block the generation of the interrupt or SMI# due to the SMBALERT# source. This bit is logically inverted and ANDed with the SMBALERT_STS bit. The resulting signal is distributed to the SMI# and/or interrupt generation logic. This bit does not effect the wake logic.
1	0h RW	**HNW:** Software sets this bit to 1 to enable the reception of a Host Notify command as a wake event. When enabled this event is ORed in with the other SMBus wake events and is reflected in the SMB_WAK_STS bit of the General Purpose Event 0 Status register.
0	0h RW	**HNI:** Software sets this bit to 1 to enable the generation of interrupt or SMI# when HOST_NOTIFY_STS is 1. This enable does not affect the setting of the HOST_NOTIFY_STS bit. When the interrupt is generated, either PIRQB or SMI# is generated, depending on the value of the SMB_SMI_EN bit (D31, F3, Off40h, B1). If the HOST_NOTIFY_STS bit is set when this bit is written to a 1, then the interrupt (or SMI#) will be generated. The interrupt (or SMI#) is logically generated by ANDing the STS and INTREN bits.

6.2.17 Notify Device Address Register (NDA) - Offset 14h

Notify Device Address Register

Type	Size	Offset	Default
MMIO	8 bit	SMBMBAR + 14h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:1	00h RO/V	**DEV_ADDR:** This field contains the 7-bit device address received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.
0	0h RO	**Reserved**

6.2.18 Notify Data Low Byte Register (NDLB) - Offset 16h

Notify Data Low Byte Register

Type	Size	Offset	Default
MMIO	8 bit	SMBMBAR + 16h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**DLB:** This field contains the first (low) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.

6.2.19 Notify Data High Byte Register (NDHB) - Offset 17h

Notify Data High Byte Register

Type	Size	Offset	Default
MMIO	8 bit	SMBMBAR + 17h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**DHB:** This field contains the second (high) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.

6.3 SMBus PCR Registers Summary

Table 6-3. Summary of SMBus PCR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	TCO Configuration (TCOCFG)	00000000h
Ch	4	General Control (GC)	00000000h
10h	4	Power Control Enable (PCE)	00000009h

6.3.1 TCO Configuration (TCOCFG) - Offset 0h

TCO Configuration

Type	Size	Offset	Default
MMIO	32 bit	FDC60000h + 0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**TCO IRQ Enable (IE):** When set, TCO IRQ is enabled, as selected by the TCO_IRQ_SEL field. When cleared, TCO IRQ is disabled.
6:3	0h RO	**Reserved**
2:0	0h RW	**TCO IRQ Select (IRQSEL):** Specifies on which IRQ the TCO will internally appear. If not using the APIC, the TCO interrupt must be routed to IRQ9-11, and that interrupt is not sharable with the SERIRQ stream, but is shareable with other PCI interrupts. If using the APIC, the TCO interrupt can also be mapped to IRQ20-23, and can be shared with other interrupt. Bits TCO Map 000 IRQ9 (maps to 8259 and APIC) 001 IRQ10 (maps to 8259 and APIC) 010 IRQ11 (maps to 8259 and APIC) 011 Reserved 100 IRQ20 (maps to APIC) 101 IRQ21 (maps to APIC) 110 IRQ22 (maps to APIC) 111 IRQ23 (maps to APIC) When setting the these bits, the IE bit should be cleared to prevent glitching. When the interrupt is mapped to APIC interrupts 9, 10 or 11, the APIC should be programmed for active-high reception. When the interrupt is mapped to APIC interrupts 20 through 23, the APIC should be programmed for active-low reception.

6.3.2 General Control (GC) - Offset Ch

General Control

Type	Size	Offset	Default
MMIO	32 bit	FDC60000h + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**SMB Slave Support (SMBSLV):** "0" : SMB controller as slave is supported "1" : SMB controller as slave is not supported Note: This bit has no other effect on the hardware, and is only used as semaphore and exposed into the BIOS menu for use by customer that has SMBus controller usage model as Slave, i.e. TCO Slave. This shall be enabled in BIOS menu to also prevent Platform from entering S0i3.4.
7:3	0h RO	**Reserved**
2	0h RW	**SMB Static Clock Gating Enable (SMBSCGE):** "0" : SMB cluster static clock gating is disabled "1" : SMB cluster static clock gating is enabled Note: Setting this bit will also clock gate all the TCO logic functionality.
1	0h RO	**Reserved**
0	0h RW	**Function Disable (FD):** When set to one, this disables the PCI configuration register space for the SMBus device.

6.3.3 Power Control Enable (PCE) - Offset 10h

Power Control Enable

Type	Size	Offset	Default
MMIO	32 bit	FDC60000h + 10h	00000009h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW	**Hardware Autonomous Enable (HAE):** When set, SMB will automatically engage power gating when it has reached its idle condition.
4	0h RO	**Reserved**
3	1h RO	**Sleep Enable (SE):** When this bit is clear, the SMB will never asset Sleep to the retention flops. If set, then SMB may assert sleep during power gating.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**D3-Hot Enable (D3HE):** No support for D3 Hot power gating.
1	0h RO	**I3 Enable (I3E):** No support for S0i3 power gating.
0	1h RW	**PMC Request Enable (PMCRE):** When set to 1, the SMB will engage power gating if it is idle and the pmc_smb_sw_pg_req_b signal is asserted.

7 Serial Peripheral Interface (SPI) Controller

7.1 SPI Configuration Registers Summary

This chapter documents the registers in Bus: 0, Device 31, Function 5.

Table 7-1. Summary of Bus: 0, Device: 31, Function: 5 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID and Vendor ID (BIOS_SPI_DID_VID)	4B248086h
4h	4	Status and Command (BIOS_SPI_STS_CMD)	00000400h
8h	4	Revision ID and Class Code (BIOS_SPI_CC_RID)	0C800000h
Ch	4	BIST, Header Type, Latency Timer, Cache Line Size (BIOS_SPI_BIST_HTYPE_LT_CLS)	00000000h
10h	4	SPI BAR0 MMIO (BIOS_SPI_BAR0)	00000000h
2Ch	4	Subsystem and Vendor ID (BIOS_SPI_SID_SVID)	00000000h
D0h	4	SPI Unsupported Request Status (BIOS_SPI_UR_STS_CTL)	00000000h
D8h	4	BIOS Decode Enable (BIOS_SPI_BDE)	0000FFCFh
DCh	4	BIOS Control (BIOS_SPI_BC)	00000028h
F8h	4	Manufacturer's ID (BIOS_SPI_MANID)	00000F00h

7.1.1 Device ID and Vendor ID (BIOS_SPI_DID_VID) - Offset 0h

Device ID and Vendor ID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:5] + 0h	4B248086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4B24h RO/V	**Device Identification (DID):** Identifier for the SPI Flash Controller in Host Root Space. The upper 9-bits of this field can be overridden by the SetID Value IOSF-SB Message. The value of the lower 7 bits is parameterized to allow different SOCs to configure the SPI IP.
15:0	8086h RO	**Vendor Identification (VID):** This field identifies the manufacturer of the device. Valid vendor identifiers are allocated by the PCI SIG to ensure uniqueness. 0x8086 indicates Intel

7.1.2 Status and Command (BIOS_SPI_STS_CMD) - Offset 4h

This is a standard PCI configuration register. See the PCI spec for bit descriptions.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:5] + 4h	00000400h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Detected Parity Error (DPE):** See the PCI spec.
30	0h RW/1C/V	**Signaled System Error (SSE):** See the PCI spec.
29	0h RO	**Received Master Abort (RMA):** See the PCI spec.
28	0h RO	**Received Target Abort (RTA):** See the PCI spec.
27	0h RW/1C/V	**Signaled Target Abort (STA):** See the PCI spec.
26:25	0h RO	**Devsel Timing (DEVT):** See the PCI spec.
24	0h RO	**Master Data Parity Error (MDPE):** See the PCI spec.
23	0h RO	**Fast Back to Back Capable (FBTBC):** Has no meaning on the internal backbone.
22	0h RO	**Reserved**
21	0h RO	**66 Mhz Capable (MCAP):** Not 66 MHz capable device. Has no meaning on the internal backbone.
20	0h RO	**Capabilities List (CAPL):** See the PCI spec.
19	0h RO	**Interrupt Status (INTS):** See the PCI spec.
18:11	0h RO	**Reserved**
10	1h RO	**Interrupt Disable (INTD):** See the PCI spec.
9	0h RO	**Fast Back to Back Enable (FBTBEN):** See the PCI spec.
8	0h RW	**System Error Enable (SERREN):** See the PCI spec.
7	0h RO	**Reserved**
6	0h RW	**Parity Error Response (PERRR):** See the PCI spec.
5	0h RO	**VGA Palette Snoop (VGAPS):** See the PCI spec.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**Memory Write and Invalidate Enable (MWRIEN):** See the PCI spec.
3	0h RO	**Special Cycles (SPCYC):** See the PCI spec.
2	0h RW	**Bus Master Enable (BME):** See the PCI spec.
1	0h RW	**Memory Space Enable (MSE):** Memory Space Enable may default False because the BIOS boot fetch decoding is hardcoded and does not rely on a BAR in configuration space.
0	0h RO	**IO Space Enable (IOSE):** See the PCI spec.

7.1.3 Revision ID and Class Code (BIOS_SPI_CC_RID) - Offset 8h

Revision ID and Class Code.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:5] + 8h	0C800000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0Ch RO	**Base Class Code (BCC):** Base Class Code
23:16	80h RO	**Sub-Class Code (SCC):** Sub-Class Code
15:8	00h RO	**Programming Interface (PI):** Programming Interface
7:0	00h RO/V	**Revision ID (RID):** Indicates the part revision. This will reset to 0 but will overridden by the SetID IOSF-SB message during the power-up sequence.

7.1.4 BIST, Header Type, Latency Timer, Cache Line Size (BIOS_SPI_BIST_HTYPE_LT_CLS) - Offset Ch

BIST, Header Type, Latency Timer, Cache Line Size.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:5] + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**Multi-function Device (MFD):** See the PCI spec.
22:16	00h RO	**Header Type (HTYPE):** See the PCI spec.
15:8	00h RO	**Latency Timer (LT):** See the PCI spec.
7:0	00h RO	**Cache Line Size (CLSZ):** See the PCI spec.

7.1.5 SPI BAR0 MMIO (BIOS_SPI_BAR0) - Offset 10h

Base Address for BAR0 - MMIO Registers.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:5] + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Memory BAR (MEMBAR):** Software programs this register with the base address of the device's memory region. The Host/BIOS MMIO registers in the flash controller are offset from this BAR.
11:4	00h RO	**Memory Size (MEMSIZE):** Hardwired to 0 to indicate 4KB of memory space.
3	0h RO	**PREFETCH:** A device can mark a range as prefetchable if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables.
2:1	0h RO	**TYP:** Hardwired to 0 to indicate that Base register is 32 bits wide and mapping can be done anywhere in the 32-bit Memory Space.
0	0h RO	**Memory Space Indicator (MEMSPACE):** Hardwired to 0 to identify a Memory BAR.

7.1.6 Subsystem and Vendor ID (BIOS_SPI_SID_SVID) - Offset 2Ch

Subsystem and Vendor ID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:5] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SSID):** Subsystem ID
15:0	0000h RW/O	**Subsystem Vendor ID (SSVID):** Subsystem Vendor ID

7.1.7 SPI Unsupported Request Status (BIOS_SPI_UR_STS_CTL) - Offset D0h

See the IOSF Specification for required behavior.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:5] + D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW/1C/V	**Unsupported Request Detected (URD):** Set to 1 by hardware upon detecting an Unsupported Request that is not considered an Advisory Non-Fatal error. Cleared to 0 when software writes a 1 to this register.
0	0h RW	**Unsupported Request Reporting Enabled (URRE):** If set to 1 by software, the flash controller generates a DoSERR sideband message when the URD bit transitions from 0 to 1.

7.1.8 BIOS Decode Enable (BIOS_SPI_BDE) - Offset D8h

This register only effects BIOS decode if BIOS is resident on SPI.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:5] + D8h	0000FFCFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**BDE Lock Enable (BLE):** When this bit is set, the RW bits of this BDE register are locked down. Once set, this bit can only be cleared by PLTRST#. **Locked by:** BIOS_SPI_BDE.BLE
30:16	0h RO	**Reserved**
15	1h RO	**F8-FF Enable (EF8):** Enables decoding of 512K of the following BIOS ranges: FFF80000h - FFFFFFFFh FFB80000h - FFBFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
14	1h RW/L	**F0-F8 Enable (EF0):** Enables decoding of 512K of the following BIOS ranges: FFF00000h - FFF7FFFFh FFB00000h - FFB7FFFFh **Locked by:** BIOS_SPI_BDE.BLE
13	1h RW/L	**E8-EF Enable (EE8):** Enables decoding of 512K of the following BIOS ranges: FFE80000h - FFEFFFFFh FFA80000h - FFAFFFFFh **Locked by:** BIOS_SPI_BDE.BLE
12	1h RW/L	**E0-E8 Enable (EE0):** Enables decoding of 512K of the following BIOS ranges: FFE00000h - FFE7FFFFh FFA00000h - FFA7FFFFh **Locked by:** BIOS_SPI_BDE.BLE
11	1h RW/L	**D8-DF Enable (ED8):** Enables decoding of 512K of the following BIOS ranges: FFD80000h - FFDFFFFFh FF980000h - FF9FFFFFh **Locked by:** BIOS_SPI_BDE.BLE
10	1h RW/L	**D0-D7 Enable (ED0):** Enables decoding of 512K of the following BIOS ranges: FFD00000h - FFD7FFFFh FF900000h - FF97FFFFh **Locked by:** BIOS_SPI_BDE.BLE
9	1h RW/L	**C8-CF Enable (EC8):** Enables decoding of 512K of the following BIOS ranges: FFC80000h - FFCFFFFFh FF880000h - FF8FFFFFh **Locked by:** BIOS_SPI_BDE.BLE
8	1h RW/L	**C0-C7 Enable (EC0):** Enables decoding of 512K of the following BIOS ranges: FFC00000h - FFC7FFFFh FF800000h - FF87FFFFh **Locked by:** BIOS_SPI_BDE.BLE
7	1h RW/L	**Legacy F Segment Enable (LFE):** This enables the decoding of the legacy 64KB range at F0000h - FFFFFh. Note that decode for the BIOS legacy F segment is enabled by the LFE bit only. It is not affected by the GEN_PMCON_1.iA64_EN bit. **Locked by:** BIOS_SPI_BDE.BLE
6	1h RW/L	**Legacy E Segment Enable (LEE):** This enables the decoding of the legacy 64KB range at E0000h - EFFFFh. Note that decode for the BIOS legacy E segment is enabled by the LEE bit only. It is not affected by the GEN_PMCON_1.iA64_EN bit. **Locked by:** BIOS_SPI_BDE.BLE
5:4	0h RO	**Reserved**
3	1h RW/L	**70-7F Enable (E70):** Enables decoding of 1MB of the following BIOS ranges: FF700000h - FF7FFFFFh FF300000h - FF3FFFFFh **Locked by:** BIOS_SPI_BDE.BLE

Bit Range	Default & Access	Field Name (ID): Description
2	1h RW/L	**60-6F Enable (E60):** Enables decoding of 1MB of the following BIOS ranges: FF600000h - FF6FFFFFh FF200000h - FF2FFFFFh **Locked by:** BIOS_SPI_BDE.BLE
1	1h RW/L	**50-5F Enable (E50):** Enables decoding of 1MB of the following BIOS ranges: FF500000h - FF5FFFFFh FF100000h - FF1FFFFFh **Locked by:** BIOS_SPI_BDE.BLE
0	1h RW/L	**40-4F Enable (E40):** Enables decoding of 1MB of the following BIOS ranges: FF400000h - FF4FFFFFh FF000000h - FF0FFFFFh **Locked by:** BIOS_SPI_BDE.BLE

7.1.9 BIOS Control (BIOS_SPI_BC) - Offset DCh

This register collects bits that were previously distributed in various IPs and input to the SPI controller via discrete wires.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:5] + DCh	00000028h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW/L	**Extended BIOS Range Lock (EXT_BIOS_LOCK):** When set, prevents EXT_BIOS_EN and EXT_BIOS_LIMIT_OFFSET from being changed. This bit can only be written from 0 to 1 once. This field is only used when the extended BIOS direct read range decoding is supported. (SPI_EXT_BIOS_BAR1_EN=1). **Locked by:** BIOS_SPI_BC.EXT_BIOS_LOCK
27	0h RW/L	**Extended BIOS Range Enable (EXT_BIOS_EN):** When set, enables the extended BIOS range decoding on SPI BAR1.This field is only used when the extended BIOS direct read range decoding is supported. (SPI_EXT_BIOS_BAR1_EN=1). **Locked by:** BIOS_SPI_BC.EXT_BIOS_LOCK
26:12	0000h RW/L	**Extended BIOS Range Limit Offset (EXT_BIOS_LIMIT_OFFSET):** This field defines the offset of the extended BIOS range upper limit from the upper limit of the BIOS region in the flash. This field is only used when the extended BIOS direct read range decoding is supported. (SPI_EXT_BIOS_BAR1_EN=1). **Locked by:** BIOS_SPI_BC.EXT_BIOS_LOCK
11	0h RW/L	**Async SMI Enable for BIOS Write Protection (ASE_BWP):** When set to '1', the flash controller will generate an SMI when it blocks a BIOS write or erase. The value in this field can be written by software as long as the BIOS Interface Lock-Down (BILD) is not set. **Locked by:** BIOS_SPI_BC.BILD

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO/V	**Asynchronous SMI Status (SPI_ASYNC_SS):** Status indication that the SPI Flash Controller has asserted an asynchronous SMI. Hardware clears the bit when it sends the De-assert SMI message. 0: default state 1: SPI flash controller asserted Asynchronous SMI
9	0h RW/L	**OS Function Hide (OSFH):** This bit controls read access over IOSF Primary to SPI's Device ID, Vendor ID PCI Configuration register. This bit does not affect access to any other PCI Configuration registers. This bit is locked with BILD. Trusted BIOS must set this bit prior to starting the OS. 0: DeviceID, VendorID can be read 1: reads to Device ID, Vendor ID return a UR **Note:** This bit is still implemented as a RW/L bit, but is no longer used by the hardware to return UR as specified above. **Locked by:** BIOS_SPI_BC.BILD
8	0h RW/1C/V	**Synchronous SMI Status (SPI_SYNC_SS):** Status indication that the SPI Flash Controller has asserted a synchronous SMI. Hardware clears the bit when it sends the De-assert Synchronous SMI message. 0: default state 1: SPI flash controller asserted Synchronous SMI
7	0h RW/L	**BIOS Interface Lock-Down (BILD):** When set, prevents BBS and ASE_BWP from being changed. This bit can only be written from 0 to 1 once. **Locked by:** BIOS_SPI_BC.BILD
6	0h RW/V/L	**Boot BIOS Strap (BBS):** This field determines the destination of accesses to the BIOS memory range. 0 SPI 1 Reserved When SPI is selected, the range that is decoded is further qualified by the BIOS Decode Enable (BDE) register. The initial value of this bit is determined by the BBS pinstrap. The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down (BILD) is not set. **Locked by:** BIOS_SPI_BC.BILD
5	1h RW/L	**Enable InSMM.STS (EISS):** When this bit is set, the BIOS region is not writable until the CPU is in SMM mode. SPI receives this indication either via the InSMM.STS bit discrete wire input or via SAI. If this bit [5] is set, then WPD must be a '1' and the CPU must be in SMM mode in order to write to BIOS regions of SPI Flash. If this bit [5] is clear, then SMM mode is a don't care. This bit is locked by LE (bit 1 of this register). **Locked by:** BIOS_SPI_BC.LE
4	0h RO/V	**Top Swap Status (TSS):** This bit provides a read-only path to view the state of the Top Swap bit.

Bit Range	Default & Access	Field Name (ID): Description
3:2	2h RW	**SPI Read Configuration (SRC):** These bits are located in PCI Configuration space to allow them to be set early in the boot flow. This 2-bit field controls two policies related to BIOS reads on the SPI interface: Bit 3 - Prefetch Enable Bit 2 - Cache Disable Settings are summarized below: Bits 3:2 -- Description 00 **No prefetching, but caching enabled.** Direct Memory reads load the read buffer cache with 'valid' data, allowing repeated reads to the same range to complete quickly 01 **No prefetching and no caching.** One-to-one correspondence of host BIOS reads to SPI cycles. This value can be used to invalidate the cache. 10 **Prefetching and Caching enabled.** This mode is used for long sequences of short reads to consecutive addresses (i.e. shadowing) 11 **Illegal.** Caching must be enabled when Prefetching is enabled. This eliminates the need for a complex prefetch-flushing mechanism
1	0h RW/L	**Lock Enable (LE):** When set, setting the WPD bit will cause a synchronous SMI. When cleared, setting the WPD bit will not cause SMI. Once set, this bit can only be cleared by a PLTRST#. When this bit is set, EISS - bit [5] of this register is locked down. **Locked by:** BIOS_SPI_BC.LE
0	0h RW	**Write Protect Disable (WPD):** When set, access to the BIOS space is enabled for both read and write cycles to BIOS. When cleared, only read cycles are permitted to the SPI flash. When this bit is written from a '0' to a '1' and the LE bit is also set, a synchronous SMI is generated. This ensures that only SMM code can update BIOS.

7.1.10 Manufacturer's ID (BIOS_SPI_MANID) - Offset F8h

This register is assigned during the boot flow using the SetID message based on values found in the fuse block. All fields except MID will be reset by hardware to zero and set only by the SetID Value message.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:5] + F8h	00000F00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000F00h RO/P	**Manufacturers ID Field (MANID)**:Manufacturer ID: Default value comes from straps.

7.2 SPI Memory Mapped Registers Summary

Table 7-2. Summary of SPI Memory Mapped Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	BIOS Flash Primary Region (BIOS_BFPREG)	00000000h
4h	4	Hardware Sequencing Flash Status and Control (BIOS_HSFSTS_CTL)	00002000h
8h	4	Flash Address (BIOS_FADDR)	00000000h
Ch	4	Discrete Lock Bits (BIOS_DLOCK)	00000000h
10h	4	Flash Data (BIOS_FDATA0)	00000000h
14h	4	Flash Data (BIOS_FDATA1)	00000000h
18h	4	Flash Data (BIOS_FDATA2)	00000000h
1Ch	4	Flash Data (BIOS_FDATA3)	00000000h
20h	4	Flash Data (BIOS_FDATA4)	00000000h
24h	4	Flash Data (BIOS_FDATA5)	00000000h
28h	4	Flash Data (BIOS_FDATA6)	00000000h
2Ch	4	Flash Data (BIOS_FDATA7)	00000000h
30h	4	Flash Data (BIOS_FDATA8)	00000000h
34h	4	Flash Data (BIOS_FDATA9)	00000000h
38h	4	Flash Data (BIOS_FDATA10)	00000000h
3Ch	4	Flash Data (BIOS_FDATA11)	00000000h
40h	4	Flash Data (BIOS_FDATA12)	00000000h
44h	4	Flash Data (BIOS_FDATA13)	00000000h
48h	4	Flash Data (BIOS_FDATA14)	00000000h
4Ch	4	Flash Data (BIOS_FDATA15)	00000000h
50h	4	Flash Region Access Permissions (BIOS_FRACC)	000042C2h
54h	4	Flash Region (BIOS_FREG0)	00000000h
58h	4	Flash Region (BIOS_FREG1)	00000000h
5Ch	4	Flash Region (BIOS_FREG2)	00000000h
60h	4	Flash Region (BIOS_FREG3)	00000000h
64h	4	Flash Region (BIOS_FREG4)	00000000h
68h	4	Flash Region (BIOS_FREG5)	00000000h
6Ch	4	Flash Region (BIOS_FREG6)	00000000h
70h	4	Flash Region (BIOS_FREG7)	00000000h
74h	4	Flash Region (BIOS_FREG8)	00000000h
78h	4	Flash Region (BIOS_FREG9)	00000000h
7Ch	4	Flash Region (BIOS_FREG10)	00000000h
80h	4	Flash Region (BIOS_FREG11)	00000000h
84h	4	Flash Protected Range (BIOS_FPR0)	00000000h
88h	4	Flash Protected Range (BIOS_FPR1)	00000000h
8Ch	4	Flash Protected Range (BIOS_FPR2)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
90h	4	Flash Protected Range (BIOS_FPR3)	00000000h
94h	4	Flash Protected Range (BIOS_FPR4)	00000000h
98h	4	Global Protected Range 0 (BIOS_GPR0)	00000000h
A0h	4	Software Sequencing Flash Status and Control (BIOS_SSFSTS_CTL)	06000000h
A4h	4	Prefix Opcode and Opcode Type Configuration (BIOS_PREOP_OPTYPE)	00000000h
A8h	4	Opcode Menu0 Configuration (BIOS_OPMENU0)	00000000h
ACh	4	Opcode Menu1 Configuration (BIOS_OPMENU1)	00000000h
B0h	4	Secondary Flash Region Access Permissions (BIOS_SFRACC)	00000000h
B4h	4	Flash Descriptor Observability Control (BIOS_FDOC)	00000000h
B8h	4	Flash Descriptor Observability Data (BIOS_FDOD)	00000000h
C0h	4	Additional Flash Control (BIOS_AFC)	00000000h
C4h	4	Vendor Specific Component Capabilities for Component 0 (BIOS_SFDP0_VSCC0)	00002000h
C8h	4	Vendor Specific Component Capabilities for Component 1 (BIOS_SFDP1_VSCC1)	00002000h
CCh	4	Parameter Table Index (BIOS_PTINX)	00000000h
D0h	4	Parameter Table Data (BIOS_PTDATA)	00000000h
D4h	4	SPI Bus Requester Status (BIOS_SBRS)	00000000h
E0h	4	Flash Region (BIOS_FREG12)	00000000h
E4h	4	Flash Region (BIOS_FREG13)	00000000h
E8h	4	Flash Region (BIOS_FREG14)	00000000h
ECh	4	Flash Region (BIOS_FREG15)	00000000h
118h	4	BIOS Master Read Access Permissions (BIOS_BM_RAP)	000000C2h
11Ch	4	BIOS Master Write Access Permissions (BIOS_BM_WAP)	00000042h
184h	4	CSXE Flash Protected Range (BIOS_CSXE_PR0)	00000000h
188h	4	CSXE Flash Protected Range (BIOS_CSXE_PR1)	00000000h
18Ch	4	CSXE Flash Protected Range (BIOS_CSXE_PR2)	00000000h
190h	4	CSXE Flash Protected Range (BIOS_CSXE_PR3)	00000000h
194h	4	CSXE Flash Protected Range (BIOS_CSXE_PR4)	00000000h
198h	4	Write Protected Range 0 (BIOS_CSXE_WPR0)	00000000h

7.2.1 BIOS Flash Primary Region (BIOS_BFPREG) - Offset 0h

BIOS Flash Primary Region.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Shadowed BIOS Region Select (SBRS):** This bit reflects the CSXEFCTRL.BRS bit under the CSME SPI CSME root space configuration register.
30:16	0000h RO/V	**BIOS Flash Primary Region Limit (PRL):** This specifies address bits 26:12 for the Primary Region Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Limit, or the Flash Descriptor.FLREG6.Region Limit depending on the BFPREG.SBRS bit.
15	0h RO	**Reserved**
14:0	0000h RO/V	**BIOS Flash Primary Region Base (PRB):** This specifies address bits 26:12 for the Primary Region Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base, or the Flash Descriptor.FLREG6.Region Base depending on the BFPREG.SBRS bit.

7.2.2 Hardware Sequencing Flash Status and Control (BIOS_HSFSTS_CTL) - Offset 4h

Several hardware sequenced operations are not supported in slave-attach flash mode.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 4h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Flash SPI SMI# Enable (FSMIE):** When set to 1, the SPI asserts an SMI# request whenever the Flash Cycle Done bit is 1.
30	0h RO	**Reserved**
29:24	00h RW	**Flash Data Byte Count (FDBC):** This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The contents of this register are 0s based with 0b representing 1 byte and 3Fh representing 64 bytes. The number of bytes transferred is the value of this field plus 1. This field is ignored for the Block Erase command.
23:22	0h RO	**Reserved**
21	0h RW	**Write Enable Type (WET):** 0: Use 06h as the write enable instruction 1: Use 50h as the write enable instruction Note: No supported flash devices require the 50h opcode to enable a non-volatile status register write. This bit is no longer required.

Bit Range	Default & Access	Field Name (ID): Description
20:17	0h RW	**Flash Cycle (FCYCLE):** This field defines the Flash SPI cycle type generated to the FLASH when the FGO bit is set as defined below: 0h: Read (1 up to 64 bytes by setting FDBC) 1h: Reserved 2h: Write (1 up to 64 bytes by setting FDBC) 3h: 4k Block Erase 4h: 64k Sector erase 5h: Read SFDP 6h: Read JEDEC ID 7h: write status 8h: read status 9h: Reserved Ah: Reserved Bh: Reserved Ch: Reserved Dh: Reserved Eh: Reserved Fh: Reserved Flash controller hardware automatically inserts a write enable opcode prior to Write and erase operations. Hardware automatically polls for device not-busy using read status after write and erase operations. If the device does not support 64k erase size (or if it doesn't support SFDP) then only 4k is allowed. See Program Register Access section for opcode values. Note: If reserved '1' is programmed to this field, flash controller will handle it as if it is 0 (Read) (Preserves legacy behavior.) Other reserved operations, set the FCERR bit and do not issue a cycle on the SPI bus.
16	0h RW/1S/V	**Flash Cycle Go (FGO):** A write to this register with a '1' in this bit initiates a request to the Flash SPI Arbiter to start a cycle. This register is cleared by hardware when the cycle is granted by the SPI arbiter to run the cycle on the SPI bus. When the cycle is complete, the FDONE bit is set. Software is forbidden to write to any register in the HSFLCTL register between the FGO bit getting set and the FDONE bit being cleared. Any attempt to violate this rule will be ignored by hardware. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write. This bit remains set until the transaction is granted by the SPI Controller's internal arbiter.
15	0h RW/L	**Flash Configuration Lock-Down (FLOCKDN):** When set to 1, those Flash Program Registers that are locked down by this FLOCKDN bit cannot be written. Once set to 1, this bit can only be cleared by a hardware reset. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN
14	0h RO/V	**Flash Descriptor Valid (FDV):** This bit is set to a 1 if the Flash Controller read the correct Flash Descriptor Signature. If the Flash Descriptor Valid bit is not 1, software cannot use the Hardware Sequencing registers, but must use the software sequencing registers. Any attempt to use the Hardware Sequencing registers will result in the FCERR bit being set.
13	1h RO/V	**Flash Descriptor Override Pin-Strap Status (FDOPSS):** This register indicates whether the flash controller is overriding descriptor permissions due to the Pin-Strap. Note: the register value is the inversion of the level sampled on the external pinstrap. 1: No override 0: The Flash Descriptor Override strap is set

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/L	**PRR3 PRR4 Lock-Down (PRR34_LOCKDN):** When set to 1, the BIOS PRR3 and PRR4 registers cannot be written. Once set to 1, this bit can only be cleared by a hardware reset. See also the BIOS PR3 and BIOS PR4 register descriptions. **Locked by:** BIOS_HSFSTS_CTL.PRR34_LOCKDN
11	0h RW/L	**Write Status Disable (WRSDIS):** 0: Write status operation may be issued using Hardware Sequencing. 1: Write status is not allowed as a Hardware Sequencing operation. The flash controller will block the operation and set the FCERR bit when software sets the 'go' bit. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN
10:9	0h RO	**Reserved**
8	0h RW/1C/V	**SAF Ctype error (H_SAF_CE):** Hardware sets this bit to 1 when a transaction is returned from the eSPI controller with Ctype error.
7	0h RO/V	**SAF Mode Active (H_SAF_MODE_ACTIVE):** 0: indicates flash is attached directly to the PCH via the SPI bus 1: indicates flash is attached to the EC/BMC and is accessed via tunneled eSPI commands
6	0h RW/1C/V	**SAF link Error (H_SAF_LE):** Hardware sets this bit to 1 when a transaction is returned from the eSPI channel with link error.
5	0h RO/V	**SPI Cycle In Progress (H_SCIP):** Hardware sets this bit when software sets the Flash Cycle Go (FGO) bit in the Hardware Sequencing Flash Control register. This bit remains set until the cycle completes on the SPI interface or the transaction is prevented due to any protection policy violation (descriptor, address range, protected region, etc). Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0.
4	0h RW/1C/V	**SAF Data length Error (H_SAF_DLE):** Hardware sets this bit to 1 when a transaction is returned from the eSPI channel with an incorrect data length.
3	0h RW/1C/V	**SAF Error (H_SAF_ERROR):** Hardware sets this bit to 1 when a transaction is requested that is not supported by slave-attached flash, e.g. read status.
2	0h RW/1C/V	**Access Error Log (H_AEL):** Hardware sets this bit to a 1 when an attempt was made to access the BIOS region using the direct access method or an access to the BIOS Program Registers that violated the security restrictions. This bit is simply a log of an access security violation. This bit is cleared by software writing a '1'.
1	0h RW/1C/V	**Flash Cycle Error (FCERR):** Hardware sets this bit to 1 when a program register access is blocked to the FLASH due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or until a partition reset occurs. Software must clear this bit before setting the FLASH Cycle GO bit in this register.
0	0h RW/1C/V	**Flash Cycle Done (FDONE):** The PCH sets this bit to 1 when the SPI Cycle completes after software previously set the FGO bit. This bit remains asserted until cleared by software writing a 1 or partition reset. Software must make sure this bit is cleared prior to enabling the SPI SMI assertion for a new programmed access.

7.2.3 Flash Address (BIOS_FADDR) - Offset 8h

Flash Address.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:0	0000000h RW	**Flash Linear Address (FLA):** The FLA is the starting byte linear address of a SPI Read or Write cycle or an address within a Block for the Block Erase command. The Flash Linear Address must fall within a region for which this master has access permissions. Hardware must convert the FLA into a Flash Physical Address (FPA) before running this cycle on the SPI bus.

7.2.4 Discrete Lock Bits (BIOS_DLOCK) - Offset Ch

Lockable BIOS registers may be locked by either the global FLOCKDN bit or by the individual DLOCK.* bit. Each lockable bit in this register is locked either by itself or by the FLOCKDN bit.

<product specific = *"SPT-LP Astep"*>

Note: Implementation of this registers required in SPT-H, but optional in SPT-LP. This register is not functional in SPT-LP A-step silicon.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW/L	**SSEQ Lock-Down (SSEQLOCKDN):** BIOS Software Sequencing registers are locked when the logical OR of this bit and FLOCKDN is true. The affected registers are SSFSTS_CTL.SCF, PREOP_OPTYPE, OPMENU0, and OPMENU1.Once set to 1 this register is only cleared by host partition reset. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SSEQLOCKDN
15:13	0h RO	**Reserved**
12	0h RW/L	**PR4 Lock-Down (PR4LOCKDN):** BIOS PR4 register is locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by BIOS partition reset. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR4LOCKDN

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/L	**PR3 Lock-Down (PR3LOCKDN):** BIOS PR3 register is locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by BIOS partition reset. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR3LOCKDN
10	0h RW/L	**PR2 Lock-Down (PR2LOCKDN):** BIOS PR2 register is locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by BIOS partition reset. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR2LOCKDN
9	0h RW/L	**PR1 Lock-Down (PR1LOCKDN):** BIOS PR1 register is locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by BIOS partition reset. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR1LOCKDN
8	0h RW/L	**PR0 Lock-Down (PR0LOCKDN):** BIOS PR0 register is locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by BIOS partition reset. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR0LOCKDN
7:4	0h RO	**Reserved**
3	0h RW/L	**SBMRAG Lock-Down (SBMRAGLOCKDN):** BIOS SFRACC.BMRAG register bits are locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by host partition reset. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SBMRAGLOCKDN
2	0h RW/L	**SBMWAG Lock-Down (SBMWAGLOCKDN):** BIOS SFRACC.BMWAG register bits are locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by host partition reset. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SBMWAGLOCKDN
1	0h RW/L	**BMRAG Lock-Down (BMRAGLOCKDN):** BIOS FRACC.BMRAG register bits are locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by host partition reset. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.BMRAGLOCKDN
0	0h RW/L	**BMWAG Lock-Down (BMWAGLOCKDN):** BIOS FRACC.BMWAG register bits are locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by host partition reset. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.BMWAGLOCKDN

7.2.5 Flash Data (BIOS_FDATA0) - Offset 10h

Flash Data.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Flash Data (FD):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13- ... 8-23-22- ... 16-31 ... 24. Bit 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. The registers are shifted in order, starting from register 0. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

7.2.6 Flash Data (BIOS_FDATA1) - Offset 14h

Flash Data.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Flash Data (FD):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13- ... 8-23-22- ... 16-31 ... 24. Bit 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. The registers are shifted in order, starting from register 0. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

7.2.7 Flash Data (BIOS_FDATA2) - Offset 18h

Flash Data.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Flash Data (FD):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13- ... 8-23-22- ... 16-31 ... 24. Bit 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. The registers are shifted in order, starting from register 0. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

7.2.8 Flash Data (BIOS_FDATA3) - Offset 1Ch

Flash Data.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Flash Data (FD):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13- ... 8-23-22- ... 16-31 ... 24. Bit 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. The registers are shifted in order, starting from register 0. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

7.2.9 Flash Data (BIOS_FDATA4) - Offset 20h

Flash Data.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Flash Data (FD):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13- ... 8-23-22- ... 16-31 ... 24. Bit 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. The registers are shifted in order, starting from register 0. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

7.2.10 Flash Data (BIOS_FDATA5) - Offset 24h

Flash Data.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 24h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Flash Data (FD):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13- ... 8-23-22- ... 16-31 ... 24. Bit 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. The registers are shifted in order, starting from register 0. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

7.2.11 Flash Data (BIOS_FDATA6) - Offset 28h

Flash Data.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 28h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Flash Data (FD):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13- ... 8-23-22- ... 16-31 ... 24. Bit 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. The registers are shifted in order, starting from register 0. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

7.2.12 Flash Data (BIOS_FDATA7) - Offset 2Ch

Flash Data.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Flash Data (FD):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13- ... 8-23-22- ... 16-31 ... 24. Bit 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. The registers are shifted in order, starting from register 0. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

7.2.13 Flash Data (BIOS_FDATA8) - Offset 30h

Flash Data.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Flash Data (FD):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13- ... 8-23-22- ... 16-31 ... 24. Bit 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. The registers are shifted in order, starting from register 0. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

7.2.14 Flash Data (BIOS_FDATA9) - Offset 34h

Flash Data.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Flash Data (FD):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13- ... 8-23-22- ... 16-31 ... 24. Bit 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. The registers are shifted in order, starting from register 0. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

7.2.15 Flash Data (BIOS_FDATA10) - Offset 38h

Flash Data.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Flash Data (FD):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13- ... 8-23-22- ... 16-31 ... 24. Bit 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. The registers are shifted in order, starting from register 0. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

7.2.16 Flash Data (BIOS_FDATA11) - Offset 3Ch

Flash Data.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Flash Data (FD):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13- ... 8-23-22- ... 16-31 ... 24. Bits 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. The registers are shifted in order, starting from register 0. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

7.2.17 Flash Data (BIOS_FDATA12) - Offset 40h

Flash Data.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Flash Data (FD):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13- ... 8-23-22- ... 16-31 ... 24. Bit 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. The registers are shifted in order, starting from register 0. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

7.2.18 Flash Data (BIOS_FDATA13) - Offset 44h

Flash Data.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 44h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Flash Data (FD):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13- ... 8-23-22- ... 16-31 ... 24. Bits 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. The registers are shifted in order, starting from register 0. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

7.2.19 Flash Data (BIOS_FDATA14) - Offset 48h

Flash Data.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Flash Data (FD):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13- ... 8-23-22- ... 16-31 ... 24. Bits 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. The registers are shifted in order, starting from register 0. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

7.2.20 Flash Data (BIOS_FDATA15) - Offset 4Ch

Flash Data.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 4Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Flash Data (FD):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13- ... 8-23-22- ... 16-31 ... 24. Bits 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. The registers are shifted in order, starting from register 0. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

7.2.21 Flash Region Access Permissions (BIOS_FRACC) - Offset 50h

Flash Region Access Permissions.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 50h	000042C2h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW/L	**BIOS Master Write Access Grant (BMWAG):** Each bit [31:24] corresponds to Master[7:0]. BIOS can grant one or more masters write access to the BIOS region 1 overriding the permissions in the Flash Descriptor. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.BMWAGLOCKDN
23:16	00h RW/L	**BIOS Master Read Access Grant (BMRAG):** Each bit [23:16] corresponds to Master[7:0]. BIOS can grant one or more masters read access to the BIOS region 1 overriding the read permissions in the Flash Descriptor. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.BMRAGLOCKDN
15:8	42h RO/V	**BIOS Region Write Access (BRWA):** Each bit [15:8] corresponds to Regions [7:0]. If the bit is set, this master can erase and write that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Master 1.Master Region Write Access OR a particular master has granted BIOS write permissions in their Master Write Access Grant register OR the Flash Descriptor Security Override strap is set.
7:0	C2h RO/V	**BIOS Region Read Access (BRRA):** Each bit [7:0] corresponds to Regions [7:0]. If the bit is set, this master can read that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Master 1.Master Region Read Access OR a particular master has granted BIOS read permissions in their Master Read Access Grant register OR the Flash Descriptor Security Override strap is set.

7.2.22 Flash Region (BIOS_FREG0) - Offset 54h

Flash Region.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 54h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:16	0000h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Limit.
15	0h RO	**Reserved**
14:0	0000h RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Base.

7.2.23 Flash Region (BIOS_FREG1) - Offset 58h

Flash Region.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:16	0000h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Limit.
15	0h RO	**Reserved**
14:0	0000h RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Base.

7.2.24 Flash Region (BIOS_FREG2) - Offset 5Ch

Flash Region.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 5Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:16	0000h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Limit.
15	0h RO	**Reserved**
14:0	0000h RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Base.

7.2.25 Flash Region (BIOS_FREG3) - Offset 60h

Flash Region.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:16	0000h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Limit.
15	0h RO	**Reserved**
14:0	0000h RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Base.

7.2.26 Flash Region (BIOS_FREG4) - Offset 64h

Flash Region.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:16	0000h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Limit.
15	0h RO	**Reserved**
14:0	0000h RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Base.

7.2.27 Flash Region (BIOS_FREG5) - Offset 68h

Flash Region.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:16	0000h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Limit.
15	0h RO	**Reserved**
14:0	0000h RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Base.

7.2.28 Flash Region (BIOS_FREG6) - Offset 6Ch

Flash Region.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 6Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:16	0000h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Limit.
15	0h RO	**Reserved**
14:0	0000h RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Base.

7.2.29 Flash Region (BIOS_FREG7) - Offset 70h

Flash Region.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:16	0000h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Limit.
15	0h RO	**Reserved**
14:0	0000h RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Base.

7.2.30 Flash Region (BIOS_FREG8) - Offset 74h

Flash Region.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 74h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:16	0000h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Limit.
15	0h RO	**Reserved**
14:0	0000h RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Base.

7.2.31 Flash Region (BIOS_FREG9) - Offset 78h

Flash Region.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 78h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:16	0000h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Limit.
15	0h RO	**Reserved**
14:0	0000h RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Base.

7.2.32 Flash Region (BIOS_FREG10) - Offset 7Ch

Flash Region.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 7Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:16	0000h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Limit.
15	0h RO	**Reserved**
14:0	0000h RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Base.

7.2.33 Flash Region (BIOS_FREG11) - Offset 80h

Flash Region.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:16	0000h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Limit.
15	0h RO	**Reserved**
14:0	0000h RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Base.

7.2.34 Flash Protected Range (BIOS_FPR0) - Offset 84h

This register cannot be written when the FLOCKDN bit is set to 1.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR0LOCKDN
30:16	0000h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR0LOCKDN
15	0h RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR0LOCKDN
14:0	0000h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR0LOCKDN

7.2.35 Flash Protected Range (BIOS_FPR1) - Offset 88h

This register cannot be written when the FLOCKDN bit is set to 1.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR1LOCKDN
30:16	0000h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR1LOCKDN
15	0h RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR1LOCKDN
14:0	0000h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR1LOCKDN

7.2.36 Flash Protected Range (BIOS_FPR2) - Offset 8Ch

This register cannot be written when the FLOCKDN bit is set to 1.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 8Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR2LOCKDN
30:16	0000h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR2LOCKDN
15	0h RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR2LOCKDN
14:0	0000h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR2LOCKDN

7.2.37 Flash Protected Range (BIOS_FPR3) - Offset 90h

This register cannot be written when the FLOCKDN bit is set to 1.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR3LOCKDN

Bit Range	Default & Access	Field Name (ID): Description
30:16	0000h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR3LOCKDN
15	0h RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR3LOCKDN
14:0	0000h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR3LOCKDN

7.2.38 Flash Protected Range (BIOS_FPR4) - Offset 94h

This register cannot be written when the FLOCKDN bit is set to 1.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR4LOCKDN
30:16	0000h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR4LOCKDN
15	0h RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR4LOCKDN
14:0	0000h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.PR4LOCKDN

7.2.39 Global Protected Range 0 (BIOS_GPR0) - Offset 98h

This register is initialized via softstraps. This protected range applies globally to all masters / flash requesters. If SPT users do not want a register that applies across all masters then the enable bits must be set false. Since this register is a descriptor-based protection, it is disabled (both enable bits are treated as false) when the Flash Descriptor Security Override pinstrap is asserted.

Note: Since this register is a RO view of the softstraps the underlying values are only reset when softstraps are reset.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0000h RO/V	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range. Note: If either Write or Read protection is enabled, then Limit must be configured greater than or equal to Base.
15	0h RO/V	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0000h RO/V	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range. Note: If either Write or Read protection is enabled, then Limit must be configured greater than or equal to Base.

7.2.40 Software Sequencing Flash Status and Control (BIOS_SSFSTS_CTL) - Offset A0h

The Software Sequencing control and status registers are intended to be used only as a back-up mode to the hardware sequencing control and status registers.**When HSSEN = 0 the SCGO bit must become read-only.** It is an implementation decision whether to make all register bits RO when HSSEN=0. Software sequencing is not supported in slave-attach flash mode.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + A0h	06000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:24	6h RW/L	**SPI Cycle Frequency (SCF):** 000: source clock is not divided 001: divide source clock by 2 010: divide source clock by 2.5 (not recommended) 011: divide source clock by 3 100: divide source clock by 4 101: divide source clock by 5 110: divide source clock by 7 All others: Reserved This register sets frequency to use for all SPI Software Sequencing cycles (write, erase, fast read, read status, etc) except for the Read cycle which always runs at divide by 7. This register is locked when the SPI Configuration Lock-Down (FLOCKDN) bit is set. Note: Fast Reset Testmode overrides the value programmed into this register. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SSEQLOCKDN
23	0h RW	**SPI SMI Enable (SME):** When set to 1, the SPI sends an assert SMI when the Cycle Done Status bit changes to a 1.
22	0h RW	**Data Cycle (DS):** When set to 1, there is data that corresponds to this transaction. When 0, no data is delivered for this cycle, and the DBC and data fields themselves are do not care.
21:16	00h RW	**Data Byte Count (DBC):** This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The valid settings (in decimal) are any value from 0 to 63. The number of bytes transferred is the value of this field plus 1. Note that when this field is 00_0000b, then there is 1 byte to transfer and that 11_1111b means there are 64 bytes to transfer.
15	0h RO	**Reserved**
14:12	0h RW	**Cycle Opcode Pointer (COP):** This field selects one of the programmed opcodes in the Opcode Menu to be used as the SPI Command/Opcode. In the case of an Atomic Cycle Sequence, this determines the second command.
11	0h RW	**Sequence Prefix Opcode Pointer (SPOP):** This field selects one of the two programmed prefix opcodes for use when performing an Atomic Cycle Sequence. A value of 0 points to the opcode in the least significant byte of the Prefix Opcodes register. By making this programmable, the PCH supports flash devices that have different opcodes for enabling writes to the data space vs. status register.
10	0h RW	**Atomic Cycle Sequence (ACS):** When set to 1 along with the SCGO assertion, the PCH will execute a sequence of commands on the SPI interface without allowing another master to arbitrate and interleave cycles. The sequence is composed of: - Atomic Sequence Prefix Command (8-bit opcode only) - Primary Command specified below by software (can include address and data) - Polling the Flash Status Register (opcode 05h) until bit 0 becomes 0b. The SPI Cycle in Progress bit remains set and the Cycle Done Status bit remains unset until the Busy bit in the Flash Status Register returns 0.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/1S/V	**SPI Cycle Go (SCGO):** This bit always returns 0 on reads. A write to this register with a '1' in this bit starts the SPI cycle defined by the other bits of this register. The SPI Cycle in Progress (SCIP) bit gets set by this action. Hardware must ignore writes to this bit while the Cycle In Progress bit is set. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write. This bit remains set until the transaction is granted by the SPI Controller's internal arbiter.
8	0h RO	**Reserved**
7	0h RO/V	**Fast Read Supported (FAST_READ_SUPPORT):** This bit reflects the value of the Fast Read Support bit in the Flash Descriptor Component Section.
6	0h RO/V	**Dual Output Fast Read Supported (DUAL_FAST_READ_SUPPORT):** This bit reflects the value of the Dual Output Fast Read Support bit in the Flash Descriptor Component Section.
5	0h RW/1C/V	**SAF Error (S_SAF_ERROR):** Hardware sets this bit to 1 when a transaction is targeted to slave-attached flash regardless of the opcode.
4	0h RO/V	**Access Error Log (AEL):** This bit reflects the value of the Hardware Sequencing Status.AEL register.
3	0h RW/1C/V	**Flash Cycle Error (FCERR):** Hardware sets this bit to 1 when a programmed access is blocked from running on the SPI interface due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or partition reset.
2	0h RW/1C/V	**Cycle Done Status (CYCLE_DONE_STS):** The PCH sets this bit to 1 when the SPI Cycle completes (i.e., SCIP bit is 0) after software sets the GO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access.
1	0h RO	**Reserved**
0	0h RO/V	**SPI Cycle In Progress (SCIP):** Hardware sets this bit when software sets the SPI Cycle Go bit in the Command register. This bit remains set until the cycle completes on the SPI interface or the transaction is prevented due to any protection policy violation (descriptor, address range, protected region, etc). Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0.

7.2.41 Prefix Opcode and Opcode Type Configuration (BIOS_PREOP_OPTYPE) - Offset A4h

This register is not writable when the Flash Configuration Lock-Down (FLOCKDN) bit is set. Entries in this register correspond to the entries in the Opcode Menu Configuration register. Note that the definition below only provides write protection for opcodes that have addresses associated with them. Therefore, any erase or write opcodes that do not use an address should be avoided (for example, 'Chip Erase' and 'Auto-Address Increment Byte Program').

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW/L	**Opcode Type 7 (OPCODE_TYPE7):** See the description for OPCODE_TYPE0. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SSEQLOCKDN
29:28	0h RW/L	**Opcode Type 6 (OPCODE_TYPE6):** See the description for OPCODE_TYPE0. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SSEQLOCKDN
27:26	0h RW/L	**Opcode Type 5 (OPCODE_TYPE5):** See the description for OPCODE_TYPE0. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SSEQLOCKDN
25:24	0h RW/L	**Opcode Type 4 (OPCODE_TYPE4):** See the description for OPCODE_TYPE0. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SSEQLOCKDN
23:22	0h RW/L	**Opcode Type 3 (OPCODE_TYPE3):** See the description for OPCODE_TYPE0. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SSEQLOCKDN
21:20	0h RW/L	**Opcode Type 2 (OPCODE_TYPE2):** See the description for OPCODE_TYPE0. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SSEQLOCKDN
19:18	0h RW/L	**Opcode Type 1 (OPCODE_TYPE1):** See the description for OPCODE_TYPE0. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SSEQLOCKDN
17:16	0h RW/L	**Opcode Type 0 (OPCODE_TYPE0):** This field specifies information about the corresponding Opcode 0. This information allows the hardware to 1) know whether to use the address field and 2) provide BIOS and Shared Flash protection capabilities. The hardware implementation also uses the read vs. write information for modifying the behavior of the SPI interface logic. The encoding of the two bits is: 00: No Address associated with this Opcode and Read Cycle type 01: No Address associated with this Opcode and Write Cycle type 10: Address required; Read cycle type 11: Address required; Write cycle type **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SSEQLOCKDN
15:8	00h RW/L	**Prefix Opcode 1 (PREFIX_OPCODE1):** Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SSEQLOCKDN
7:0	00h RW/L	**Prefix Opcode 0 (PREFIX_OPCODE0):** Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SSEQLOCKDN

7.2.42 Opcode Menu0 Configuration (BIOS_OPMENU0) - Offset A8h

This register is not writable when the SPI Configuration Lock-Down bit (FLOCKDN) is set.

Eight entries are available in this register to give a sufficient set of commands for communicating with the flash device, while also restricting what malicious software can do. This keeps the hardware flexible enough to operate with a wide variety of SPI devices.

It is recommended to avoid programming Write Enable opcodes in this menu. Malicious software could then perform writes and erases to the SPI flash without using the atomic cycle mechanism. This could cause functional failures in a shared flash environment. Write Enable opcodes should only be programmed in the Prefix Opcodes.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW/L	**Allowable Opcode 3 (OPCODE3):** See the description for OPCODE0. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SSEQLOCKDN
23:16	00h RW/L	**Allowable Opcode 2 (OPCODE2):** See the description for OPCODE0. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SSEQLOCKDN
15:8	00h RW/L	**Allowable Opcode 1 (OPCODE1):** See the description for OPCODE0. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SSEQLOCKDN
7:0	00h RW/L	**Allowable Opcode 0 (OPCODE0):** Software programs an SPI opcode into this field for use when initiating SPI commands through the Control Register. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SSEQLOCKDN

7.2.43 Opcode Menu1 Configuration (BIOS_OPMENU1) - Offset ACh

See description for the 'OPMENU0 -- Opcode Menu0 Configuration'.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW/L	**Allowable Opcode 7 (OPCODE7):** See the description for OPCODE0. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SSEQLOCKDN
23:16	00h RW/L	**Allowable Opcode 6 (OPCODE6):** See the description for OPCODE0. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SSEQLOCKDN
15:8	00h RW/L	**Allowable Opcode 5 (OPCODE5):** See the description for OPCODE0. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SSEQLOCKDN
7:0	00h RW/L	**Allowable Opcode 4 (OPCODE4):** See the description for OPCODE0. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SSEQLOCKDN

7.2.44 Secondary Flash Region Access Permissions (BIOS_SFRACC) - Offset B0h

Secondary Flash Region Access Permissions

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW/L	**Secondary BIOS Master Write Access Grant (SECONDARYBIOS_MWAG):** Each bit [31:29] corresponds to Master[7:0]. BIOS can grant one or more masters write access to the Secondary BIOS region 6 overriding the permissions in the Flash Descriptor. Bits for unassigned masters are reserved. The contents of this register are locked by the FLOCKDN bit. See section 'DLOCK -- Discrete Lock Bits' or a description of how this register is locked. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SBMWAGLOCKDN
23:16	00h RW/L	**Secondary BIOS Master Read Access Grant (SECONDARYBIOS_MRAG):** Each bit [28:16] corresponds to Master[7:0]. BIOS can grant one or more masters read access to the Secondary BIOS region 6 overriding the read permissions in the Flash Descriptor. Bits for unassigned masters are reserved. The contents of this register are locked by the FLOCKDN bit. See section 'DLOCK -- Discrete Lock Bits' or a description of how this register is locked. **Locked by:** BIOS_HSFSTS_CTL.FLOCKDN, BIOS_DLOCK.SBMRAGLOCKDN
15:0	0h RO	**Reserved**

7.2.45 Flash Descriptor Observability Control (BIOS_FDOC) - Offset B4h

This is a test mode only register that can be used to observe the contents of the Flash Descriptor that is stored internally in the PCH Flash Controller. The CPU Complex soft straps are not observable in PCH as these are forwarded to the CPU Complex and not stored.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14:12	0h RW	**Flash Descriptor Section Select (FDSS):** Selects which section within the loaded Flash Descriptor to observe. 000: Flash Signature and Descriptor Map 001: Component 010: Region 011: Master 100: PCH Soft Straps Other: Reserved
11:2	000h RW	**Flash Descriptor Section Index (FDSI):** Selects the DW offset within the Flash Descriptor Section to observe.
1:0	0h RO	**Reserved**

7.2.46 Flash Descriptor Observability Data (BIOS_FDOD) - Offset B8h

Flash Descriptor Observability Data.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Flash Descriptor Section Data (FDSD):** Returns the DW of data to observe as selected in the Flash Descriptor Observability Control.

7.2.47 Additional Flash Control (BIOS_AFC) - Offset C0h

Additional Flash Control.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/V/P	**Stop Prefetch on Flush Pending (SPFP):** When set to '1', the progress of a pre-fetch will be ended if subsequence access from the master of the same Root Space is detected to be a cache-miss and read cache will be flushed. When set to '0', the prefetch will be allowed to complete prior to flushing. This register is only reset on an Early boot reset of both the Host and the CSME partitions. Hardware loads this bit from the PCH soft strap SPI_SPFP when the strap completion is received from the strap pull message.

7.2.48 Vendor Specific Component Capabilities for Component 0 (BIOS_SFDP0_VSCC0) - Offset C4h

Support for non-SFDP capable flash devices is deprecated.

Hardware uses the data it loads from the flash device's SFDP tables. Hardware copies some SFDP data to the SFDP_VSCCn registers for the convenience of BIOS/FW, but does not directly use the data in those registers.

Hardware locks the SFDP_VSCCn registers after copying SFDP data into them and setting the CPPTV bit.

Firmware requirements:

The QER bits are not used by the hardware. The QER bits are used by software/ firmware to ensure the QE bit is not changed while doing status register write.

The QER field in SFDP_VSCC is only valid if the flash device contains a rev 1.5 or higher SFDP table. Firmware must use PTINX/PTDATA to read the Parameter Table Header to determine the SFDP revision.

If the SFDP revision is < 1.5 then firmware must use some other means to determine QER, e.g. the Flash Upper Map VSCC tables.

The fields in this register pertain to cycles targeting addresses within Component 0. The lockable bits in this register are locked when either CPPTV is set to '1' by hardware or when VCL is '1'.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + C4h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Component Property Parameter Table Valid (CPPTV):** This bit is set to a 1 if the Flash Controller detects a valid SFDP Component Property Parameter Table in Component 0. Note: If this bit is set software must not overwrite bits that were initialized by hardware via SFDP discovery.
30	0h RW/L	**Vendor Component Lock (VCL):** 0: The lock bit is not set. 1: The Vendor Component Lock bit is set. This register locks itself when set. **Locked by:** BIOS_SFDP0_VSCC0.VCL
29	0h RW/V/L	**64k Erase Valid (EO_64K_VALID):** 0: The EO_64k opcode is not valid. 1: The EO_64k opcode is valid. **Locked by:** BIOS_SFDP0_VSCC0.VCL
28	0h RW/V/L	**4k Erase Valid (EO_4K_VALID):** 0: The EO_4k opcode is not valid. 1: The EO_4k opcode is valid. **Locked by:** BIOS_SFDP0_VSCC0.VCL
27	0h RW/L	**RPMC Supported (RPMC_SUPPORTED):** 0: The device does not support RPMC. 1: The device supports RPMC. **Locked by:** BIOS_SFDP0_VSCC0.VCL
26	0h RW/V/L	**Deep Powerdown Supported (DEEP_PWRDN_SUPPORTED):** 0: The device does not support Deep Powerdown. 1: The device supports Deep Powerdown. **Locked by:** BIOS_SFDP0_VSCC0.VCL
25	0h RW/V/L	**Suspend/Resume Supported (SUSPEND_RESUME_SUPPORTED):** 1: The device does not support Suspend/Resume. 0: The device supports Suspend/Resume. **Locked by:** BIOS_SFDP0_VSCC0.VCL
24	0h RW/V/L	**Soft Reset Supported (SOFT_RST_SUPPORTED):** 0: The device does not support Soft Reset. 1: The device supports Soft Reset. **Locked by:** BIOS_SFDP0_VSCC0.VCL
23:16	00h RW/V/L	**64k Erase Opcode (EO_64K):** This register is programmed with the Flash 64k sector erase instruction opcode for component 0. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit. **Locked by:** BIOS_SFDP0_VSCC0.VCL
15:8	20h RW/V/L	**4k Erase Opcode (EO_4K):** This register is programmed with the Flash 4k subsector erase instruction opcode for component 0. Software must program this register if the SFDP table for this component does not show 4 kByte erase capability. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit. **Locked by:** BIOS_SFDP0_VSCC0.VCL

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RW/V/L	**Quad Enable Requirements (QER):** This field is defined by the JEDEC JESD216A standard for SFDP, reference 2. Information is copied here for reference. The JEDEC standard shall take precedence in the event of a discrepancy. This field describes whether the device contains a Quad Enable (QE) bit used to enable 1-1-4 and 1-4-4 quad read or quad program operations. If QE exists, this field also identifies the bit location and method to set/clear the bit. In this specification, status register 1 refers to the first data byte transferred on a Read Status (05h) or Write Status (01h) command. Status register 2 refers to the byte read using instruction 35h. Status register 2 is the second byte transferred in a Write Status (01h) command. Bits are numbered from 7 to 0, where bit 7 is transferred first on the wire. Note: Industry naming and definitions of these status registers may differ. The user will typically perform a read-modify-write sequence of operations to maintain the state of all other writable status register bits. For example read both status registers, set/clear QE, Write Status with both data bytes. 000b: Device does not have a QE bit. Device detects 1-1-4 and 1-4-4 reads based on instruction. DQ3/HOLD# functions as hold during instruction phase. 001b: QE is bit 1 of status register 2. It is set via Write Status with two data bytes where bit 1 of the second byte is one. It is cleared via Write Status with two data bytes where bit 1 of the second byte is zero. Writing only one byte to the status register has the side-effect of clearing status register 2, including the QE bit. The 100b code is used if writing one byte to the status register does not modify status register 2. 010b: QE is bit 6 of status register 1. It is set via Write Status with one data byte where bit 6 is one. It is cleared via Write Status with one data byte where bit 6 is zero. 011b: QE is bit 7 of status register 2. It is set via Write status register 2 instruction 3Eh with one data byte where bit 7 is one. It is cleared via Write status register 2 instruction 3Eh with one data byte where bit 7 is zero. The status register 2 is read using instruction 3Fh. 100b: QE is bit 1 of status register 2. It is set via Write Status with two data bytes where bit 1 of the second byte is one. It is cleared via Write Status with two data bytes where bit 1 of the second byte is zero. In contrast to the 001b code, writing one byte to the status register does not modify status register 2. 101b: QE is bit 1 of the status register 2. Status register 1 is read using Read Status instruction 05h. Status register 2 is read using instruction 35h. QE is set via Write Status instruction 01h with two data bytes where bit 1 of the second byte is one. It is cleared via Write Status with two data bytes where bit 1 of the second byte is zero. Other: Reserved. This register is locked by the Vendor Component Lock (VCL) bit. The flash controller hardware does not use this field. NOTE: This field is only valid for SFDP revision 1.5 and above. Firmware must check the revision prior to acting on the contents of this register. **Locked by:** BIOS_SFDP0_VSCC0.VCL
4	0h RW/V/L	**Write Enable on Write Status (WEWS):** 0: 50h is the opcode to enable a status register write. 1: 06h is the opcode to enable a status register write. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit. Note: Hardware ignores the state of this bit and only issues 06h as a write enable. **Locked by:** BIOS_SFDP0_VSCC0.VCL

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/V/L	**Write Status Required (WSR):** 0: No requirement to write to the Write Status Register prior to a write. 1: A write is required to the Write Status Register prior to write and erase to remove any protection. This is required for SST components. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit. Note: Hardware ignores the state of this bit and behaves as if WSR=0. Flash devices that contain a 1 in this field are no longer supported by the flash controller. **Locked by:** BIOS_SFDP0_VSCC0.VCL
2	0h RW/V/L	**Write Granularity (WG):** 0: Reserved. 1: 64 Byte. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit. Note: Hardware ignores the state of this bit. **Locked by:** BIOS_SFDP0_VSCC0.VCL
1:0	0h RO	**Reserved**

7.2.49 Vendor Specific Component Capabilities for Component 1 (BIOS_SFDP1_VSCC1) - Offset C8h

The fields in this register pertain to cycles targeting addresses outside of Component 0. The lockable bits in this register are locked when either CPPTV is set to '1' by hardware or when VCL is '1'.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + C8h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Component Property Parameter Table Valid (CPPTV):** This bit is set to a 1 if the Flash Controller detects a valid SFDP Component Property Parameter Table in Component 1. Note: If this bit is set software must not overwrite bits that were initialized by hardware via SFDP discovery.
30	0h RO	**Reserved**
29	0h RW/V/L	**64k Erase Valid (EO_64K_VALID):** 0: The EO_64k opcode is not valid. 1: The EO_64k opcode is valid. **Locked by:** BIOS_SFDP0_VSCC0.VCL
28	0h RW/V/L	**4k Erase Valid (EO_4K_VALID):** 0 The EO_4k opcode is not valid. 1 The EO_4k opcode is valid. **Locked by:** BIOS_SFDP0_VSCC0.VCL
27	0h RW/L	**RPMC Supported (RPMC_SUPPORTED):** 0: The device does not support RPMC. 1: The device supports RPMC. **Locked by:** BIOS_SFDP0_VSCC0.VCL

Bit Range	Default & Access	Field Name (ID): Description
26	0h RW/V/L	**Deep Powerdown Supported (DEEP_PWRDN_SUPPORTED):** 0: The device does not support Deep Powerdown. 1: The device supports Deep Powerdown. **Locked by:** BIOS_SFDP0_VSCC0.VCL
25	0h RW/V/L	**Suspend/Resume Supported (SUSPEND_RESUME_SUPPORTED):** 1: The device does not support Suspend/Resume. 0: The device supports Suspend/Resume. **Locked by:** BIOS_SFDP0_VSCC0.VCL
24	0h RW/V/L	**Soft Reset Supported (SOFT_RST_SUPPORTED):** 0: The device does not support Soft Reset. 1: The device supports Soft Reset. **Locked by:** BIOS_SFDP0_VSCC0.VCL
23:16	00h RW/V/L	**64k Erase Opcode (EO_64K):** This register is programmed with the Flash 64k sector erase instruction opcode for component 1. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit. **Locked by:** BIOS_SFDP0_VSCC0.VCL
15:8	20h RW/V/L	**4k Erase Opcode (EO_4K):** This register is programmed with the Flash 4k subsector erase instruction opcode for component 1. Software must program this register if the SFDP table for this component does not show 4 kByte erase capability. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit. **Locked by:** BIOS_SFDP0_VSCC0.VCL
7:5	0h RW/V/L	**Quad Enable Requirements (QER):** See description in SFDP0_VSCC0.QER. **Locked by:** BIOS_SFDP0_VSCC0.VCL
4	0h RW/V/L	**Write Enable on Write Status (WEWS):** See description in SFDP0_VSCC0.WEWS. **Locked by:** BIOS_SFDP0_VSCC0.VCL
3	0h RW/V/L	**Write Status Required (WSR):** See description in SFDP0_VSCC0.WSR. **Locked by:** BIOS_SFDP0_VSCC0.VCL
2	0h RW/V/L	**Write Granularity (WG):** See description in SFDP0_VSCC0.WG. **Locked by:** BIOS_SFDP0_VSCC0.VCL
1:0	0h RO	**Reserved**

7.2.50 Parameter Table Index (BIOS_PTINX) - Offset CCh

Observability Control for Component Property Tables.

Note: The PTINX and PTDATA registers do not have any meaning in slave-attach flash mode because the SPI controller does not perform SFDP discovery.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:14	0h RW	**Supported Parameter Table (SPT):** Selects which supported parameter table to observe. 00: Component 0 Property Parameter Table. 01: Component 1 Property Parameter Table. 10 - 11: Reserved.
13:12	0h RW	**Header or Data (HORD):** Select parameter table header DW vs Data DW. 00: SFDP Header. 01: Parameter Table Header. 10: Data. 11: Reserved.
11:2	000h RW	**Parameter Table DW Index (PTDWI):** Selects the DW offset within the parameter table to observe. The returned data is undefined if the index is programmed to a value greater than the size of the header or table.
1:0	0h RO	**Reserved**

7.2.51 Parameter Table Data (BIOS_PTDATA) - Offset D0h

Parameter Table Data

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Parameter Table DW Data (PTDWD):** Returns the DW of data to observe as selected in the Parameter Table Index register. Note: The returned value of reserved fields in the SFDP header or table must be ignored by software. The flash controller may return either 0 or 1 for these fields.

7.2.52 SPI Bus Requester Status (BIOS_SBRS) - Offset D4h

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**TPM Access Ongoing (TPM_ACC_ONG):** Indicates that a TPM access is in progress.
30	0h RO/V	**eSPI Access Ongoing (ESPI_ACC_ONG):** This bit is only defined if eSPI and SPI are sharing the SPI bus.
29	0h RO/V	**Touch Access Ongoing (TOUCH_ACC_ONG):** Indicates that a Touch access is in progress.
28	0h RO/V	**CSME accessing the Huffman Decompression (CSME_ACC_HWD):** Indicates that CSME has a HW Decompression cycle in progress.
27:18	0h RO	**Reserved**
17:15	0h RO/V	**Master 5 Status (M5STATUS):** See description under M1STATUS.
14:12	0h RO/V	**Master 6 Status (M6STATUS):** See description under M1STATUS.
11:9	0h RO/V	**Master 4 Status (M4STATUS):** See description under M1STATUS.
8:6	0h RO/V	**Master 3 Status (M3STATUS):** See description under M1STATUS.
5:3	0h RO/V	**Master 2 Status (M2STATUS):** See description under M1STATUS.
2:0	0h RO/V	**Master 1 Status (M1STATUS):** Indicates whether this master has an outstanding transaction enqueued or in flight and the transaction type. 0xx: No transaction. 100: Flash read transaction. 101: Flash write transaction. 110: Flash erase transaction. 111: Flash RPMC transaction.

7.2.53 Flash Region (BIOS_FREG12) - Offset E0h

Flash Region.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
30:16	0000h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Limit.
15	0h RO	**Reserved**
14:0	0000h RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Base.

7.2.54 Flash Region (BIOS_FREG13) - Offset E4h

Flash Region.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:16	0000h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Limit.
15	0h RO	**Reserved**
14:0	0000h RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Base.

7.2.55 Flash Region (BIOS_FREG14) - Offset E8h

Flash Region.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
30:16	0000h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Limit.
15	0h RO	**Reserved**
14:0	0000h RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Base.

7.2.56 Flash Region (BIOS_FREG15) - Offset ECh

Flash Region.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:16	0000h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Limit.
15	0h RO	**Reserved**
14:0	0000h RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREGX.Region Base.

7.2.57 BIOS Master Read Access Permissions (BIOS_BM_RAP) - Offset 118h

BIOS Master Read Access Permissions.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 118h	000000C2h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	00C2h RO/V	**BIOS Master Read Access Permissions (BMRAP):** Each bit [15:0] corresponds to Regions [15:0]. If the bit is set, this master can read that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Master 1.Master Region Read Access OR a particular master has granted BIOS read permissions in their Master Read Access Grant register OR the Flash Descriptor Security Override strap is set. BIOS has read access to its own Region 1, 6 and 7 by default. Thus, the reset default of this field will be read as *"C2h"*.

7.2.58 BIOS Master Write Access Permissions (BIOS_BM_WAP) - Offset 11Ch

BIOS Master Write Access Permissions.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 11Ch	00000042h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0042h RO/V	**BIOS Master Write Access Permissions (BMWAP):** Each bit [15:0] corresponds to Regions [15:0]. If the bit is set, this master can erase and write that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Master 1.Master Region Write Access OR a particular master has granted BIOS write permissions in their Master Write Access Grant register OR the Flash Descriptor Security Override strap is set. BIOS has write access to its own Region 1 and 6 by default. Thus, the reset default of this field will be read as *"42h"*.

7.2.59 CSXE Flash Protected Range (BIOS_CSXE_PR0) - Offset 184h

These are not physical registers in the memory space. These addresses provide the host with a read-only view of the values stored in the CSxE Protected Range registers.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 184h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Write Protection Enable (WPE):** Write Protection Enable: When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0000h RO/V	**Protected Range Limit (PRL):** Protected Range Limit: This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0h RO/V	**Read Protection Enable (RPE):** Read Protection Enable: When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0000h RO/V	**Protected Range Base (PRB):** Protected Range Base: This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

7.2.60 CSXE Flash Protected Range (BIOS_CSXE_PR1) - Offset 188h

These are not physical registers in the memory space. These addresses provide the host with a read-only view of the values stored in the CSxE Protected Range registers.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 188h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Write Protection Enable (WPE):** Write Protection Enable: When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0000h RO/V	**Protected Range Limit (PRL):** Protected Range Limit: This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0h RO/V	**Read Protection Enable (RPE):** Read Protection Enable: When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0000h RO/V	**Protected Range Base (PRB):** Protected Range Base: This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

7.2.61 CSXE Flash Protected Range (BIOS_CSXE_PR2) - Offset 18Ch

These are not physical registers in the memory space. These addresses provide the host with a read-only view of the values stored in the CSxE Protected Range registers.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 18Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Write Protection Enable (WPE):** Write Protection Enable: When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0000h RO/V	**Protected Range Limit (PRL):** Protected Range Limit: This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0h RO/V	**Read Protection Enable (RPE):** Read Protection Enable: When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0000h RO/V	**Protected Range Base (PRB):** Protected Range Base: This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

7.2.62 CSXE Flash Protected Range (BIOS_CSXE_PR3) - Offset 190h

These are not physical registers in the memory space. These addresses provide the host with a read-only view of the values stored in the CSxE Protected Range registers.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 190h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Write Protection Enable (WPE):** Write Protection Enable: When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0000h RO/V	**Protected Range Limit (PRL):** Protected Range Limit: This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0h RO/V	**Read Protection Enable (RPE):** Read Protection Enable: When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0000h RO/V	**Protected Range Base (PRB):** Protected Range Base: This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

7.2.63 CSXE Flash Protected Range (BIOS_CSXE_PR4) - Offset 194h

These are not physical registers in the memory space. These addresses provide the host with a read-only view of the values stored in the CSxE Protected Range registers.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 194h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Write Protection Enable (WPE):** Write Protection Enable: When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0000h RO/V	**Protected Range Limit (PRL):** Protected Range Limit: This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0h RO/V	**Read Protection Enable (RPE):** Read Protection Enable: When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0000h RO/V	**Protected Range Base (PRB):** Protected Range Base: This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

7.2.64 Write Protected Range 0 (BIOS_CSXE_WPR0) - Offset 198h

This is not a physical register in the memory space. This address provides the Host with a read-only view of the values stored in the CSXE Write Protected Range register.

Type	Size	Offset	Default
MMIO	32 bit	BIOS_SPI_BAR + 198h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0000h RO/V	**Blocked Range Limit (BRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0h RO	**Reserved**
14:0	0000h RO/V	**Blocked Range Base (BRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

8 Universal Asynchronous Receiver/Transmitter (UART) Controller

8.1 UART Configuration Registers Summary

This chapter documents the registers in Bus: 0, Device 30, Function 0 and 1. Also lists the registers in Bus 0, Device 25, Function 2.

DID Values:

- UART Controller #0:- D30:F0 - 4B28h
- UART Controller #1:- D30:F1 - 4B29h
- UART Controller #2:- D25:F2 - 4B4Dh

Table 8-1. Summary of Bus: 0, Design: 30, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID And Vendor ID Register (DEVVENDID)	4B288086h
4h	4	Status and Command (STATUSCOMMAND)	00100000h
8h	4	Revision ID and Class Code (REVCLASSCODE)	07800000h
Ch	4	Cache Line Latency Header and BIST (CLLATHEADERBIST)	00800000h
10h	4	Base Address Register (BAR)	00000000h
14h	4	Base Address Register High (BAR_HIGH)	00000000h
18h	4	Base Address Register1 (BAR1)	00000004h
1Ch	4	Base Address Register1 High (BAR1_HIGH)	00000000h
2Ch	4	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)	00000000h
30h	4	Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)	00000000h
34h	4	Capabilities Pointer Register (CAPABILITYPTR)	00000080h
3Ch	4	Interrupt Register (INTERRUPTREG)	00000000h
80h	4	Power Management Capability ID (POWERCAPID)	00039001h
84h	4	Power Management Control and Status Register (PMECTRLSTATUS)	00000008h
90h	4	PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD)	F0140009h
94h	4	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG)	01400010h
98h	4	Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)	00002101h
9Ch	4	Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG)	000024C1h
A0h	4	D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG)	000F0800h
B0h	4	General Purpose Read Write Register1 (GEN_REGRW1)	00000000h
B4h	4	General Purpose Read Write Register2 (GEN_REGRW2)	00000000h
B8h	4	General Purpose Read Write Register3 (GEN_REGRW3)	00000000h
BCh	4	General Purpose Read Write Register4 (GEN_REGRW4)	00000000h
C0h	4	General Purpose Input Register (GEN_INPUT_REG)	00000000h
F8h	4	Manufacturers ID (MANID)	00000000h

8.1.1 Device ID And Vendor ID Register (DEVVENDID) - Offset 0h

Device ID and Vendor ID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + 0h	4B288086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4B28h RO/P	**Device ID Field (DEVICEID):** Device ID identifies the particular PCI device
15:0	8086h RO	**Vendor ID Field (VENDORID):** Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device

8.1.2 Status And Command (STATUSCOMMAND) - Offset 4h

Command register and Status register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW/1C	**RMA Field (RMA):** Received Master Abort
28	0h RW/1C	**RTA Field (RTA):** Received Target Abort
27:21	0h RO	**Reserved**
20	1h RO	**Cap List Field (CAPLIST):** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**Interrupt Status Field (INTR_STATUS):** Interrupt Status: This bit reflects state of interrupt in the device
18:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** Interrupt Disable
9	0h RO	**Reserved**
8	0h RW	**SERR Enable Field (SERR_ENABLE):** SERR Enable Not implemented
7:3	0h RO	**Reserved**
2	0h RW	**BME Field (BME):** Bus Master Enable
1	0h RW	**MSE Field (MSE):** Memory Space Enable
0	0h RO	**Reserved**

8.1.3 Revision ID And Class Code (REVCLASSCODE) - Offset 8h

Revision ID register and Class Code register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + 8h	07800000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	078000h RO	**Revision ID Field (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	00h RO/P	**Class Code Field (RID):** Revision ID identifies the revision of particular PCI device.

8.1.4 Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch

Cache Line size as RW with def 0 Latency timer RW with def 0 Header type with Type 0 configuration header and Reserved BIST register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + Ch	00800000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	1h RO	**Multi Function Device Field (MULFNDEV):** Multi-Function Device
22:16	00h RO	**Header Type Field (HEADERTYPE):** Header Type: Implements Type 0 Configuration header
15:8	00h RO	**Latency Timer Field (LATTIMER):** Latency Timer: This register is implemented as R/W with default as 0
7:0	00h RW/P	**Cache Line Size Field (CACHELINE_SIZE):** Cache Line Size

8.1.5 Base Address Register (BAR) - Offset 10h

Base Address Register Low [31:2] type[2:1] in 32-bit or 64-bit address range and memory space indicator [0].

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR):** Base Address Register Low Base address of the OCP fabric memory space. Taken from Strap values as ones
11:4	00h RO	**Size Field (SIZEINDICATOR):** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**Prefetchable Field (PREFETCHABLE):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE0):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** Memory Space Indicator: 0 indicates this BAR is present in the memory space.

8.1.6 Base Address Register High (BAR_HIGH) - Offset 14h

Base Address Register High enabled if [2:1] of BAR_HIGH is 10.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR_HIGH):** Base Address High - MSB

8.1.7 Base Address Register1 (BAR1) - Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K type in [2:1] and Memory Space Indicator in [0].

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + 18h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR1):** Base Address1 This field is present if BAR1 is enabled through private configuration space.
11:4	00h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	2h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

8.1.8 Base Address Register1 High (BAR1_HIGH) - Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1 register is 10.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR1_HIGH):** Base Address: Base address of the OCP fabric memory space. Taken from Strap values as ones

8.1.9 Subsystem Vendor And Subsystem ID (SUBSYSTEMID) - Offset 2Ch

SVID register along with SID register is to distinguish subsystem from another.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system.
15:0	0000h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

8.1.10 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h

Expansion ROM Base Address register is a RO indicates support for Expansion ROMs.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION ROM base address field (EXPANSION_ROM_BASE):** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

8.1.11 Capabilities Pointer Register (CAPABILITYPTR) - Offset 34h

Capabilities Pointer register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Capabilities Pointer: Indicates what the next capability is.

8.1.12 Interrupt Register (INTERRUPTREG) - Offset 3Ch

Interrupt line Register isn't used in Bridge directly Interrupt Pin register reflects the IPIN value in private configuration space. Min_GNT register indicating the requirements of latency timers and max_LAT register max latency.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + 3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**Min GNT Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers // Re-Check Desc Padma

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11:8	0h RO	**Interrupt Pin Field (INTPIN):** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW/P	**Int Line Field (INTLINE):** Interrupt Line: It is used to communicate to software the interrupt line to which the interrupt pin is connected

8.1.13 Power Management Capability ID (POWERCAPID) - Offset 80h

Power Management Capability ID register points to Next Capability Structure and Power Management Capability with Power Management Capabilities register for PME Support and Version.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + 80h	00039001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved**
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h RO	**Next Cap Field (NXTCAP):** Next Capability: Points to the next capability structure.
7:0	01h RO	**Power Capability ID Field (POWER_CAP):** Power Management Capability: Indicates this is power management capability

8.1.14 Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h

Power Management Control and Status Register to set and read PME Status, PME enable, No Soft Reset and Power State.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/P	**PME Status Field (PMESTATUS):** PME Status
14:9	0h RO	**Reserved**
8	0h RW/P	**PME Enable Field (PMEENABLE):** PME Enable
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset
2	0h RO	**Reserved**
1:0	0h RW	**Power State Field (POWERSTATE):** Power State: This field is used both to determine the current Power State and to set a new Power State

8.1.15 PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h

PCI Device Vendor Specific Capability register defines Vendor Specific Capability ID, Revision, Length, Next Capability and CAPID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + 90h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision ID Field (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	00h RO	**Next Capability Field (NEXT_CAP):** Next Capability
7:0	09h RO	**Capability ID Field (CAPID):** Capability ID

8.1.16 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h

Extended Vendor capability register for VSEC Length, Revision and ID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific ID Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor specific Extended Capability revision
15:0	0010h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

8.1.17 Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h

Software location pointer in MMIO space as an offset specified by BAR.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + 98h	00002101h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000210h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR BAR Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	1h RO	**SW LTR Valid Field (SW_LAT_VALID):** This value is reflected from the SW LTR valid strap at the top level

8.1.18 Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch

Device IDLE pointer register giving details on Device MMIO offset Location, BAR NUM and D0i3 Valid Strap.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + 9Ch	000024C1h

Bit Range	Default & Access	Field Name (ID): Description
31:4	000024Ch RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** Bar num: Indicates that the D0i3 MMIO location is always at BAR0
0	1h RO	**D0i3 Valid Field (VALID):** Valid: This value is reflected from the D0i3 valid strap at the top level.

8.1.19 D0i3 And Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h

D0idle_Max_Power_On_Latency register set at boot and power control enable register to enable communication with the PGCB block below the Bridge.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + A0h	000F0800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW/P	**HAE Field (HAE):** Hardware Autonomous Enable
20	0h RO	**Reserved**
19	1h RW/P	**Sleep Enable Field (SLEEP_EN):** Sleep Enable
18	1h RW/P	**D3 Hen Field (PGE):** DEVIDLE Enable (DEVIDLEN): If '1' then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set.
17	1h RW/P	**Device Idle En Field (I3E):** PMCRE: PMC Request Enable
16	1h RW/P	**PMC Request Enable Field (PMCRE):** D3-Hot Enable (D3HEN): If '1' then function will power gate when idle and the PMCSR[1:0] register in the function ='11' (D3).
15:13	0h RO	**Reserved**
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** Power On Latency Scale
9:0	000h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** Power On Latency value

8.1.20 General Purpose Read Write Register1 (GEN_REGRW1) - Offset B0h

General Purpose PCI Read Write Register1.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_REG_RW1):** General Purpose PCI Register: This register value is brought out as GEN_REG_RW1

8.1.21 General Purpose Read Write Register2 (GEN_REGRW2) - Offset B4h

General Purpose PCI Read Write Register2.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_REG_RW2):** General Purpose PCI Register: This register value is brought out as GEN_REG_RW2

8.1.22 General Purpose Read Write Register3 (GEN_REGRW3) - Offset B8h

General Purpose PCI Read Write Register3.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_REG_RW3):** General Purpose PCI Register: This register value is brought out as GEN_REG_RW3

8.1.23 General Purpose Read Write Register4 (GEN_REGRW4) - Offset BCh

General Purpose PCI Read Write Register4.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_REG_RW4):** General Purpose PCI Register: This register value is brought out as GEN_REG_RW4

8.1.24 General Purpose Input Register (GEN_INPUT_REG) - Offset C0h

General Purpose Input Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General Purpose Input Register: This register value reflects the value of GEN_REG_INPUT_RW

8.1.25 Manufacturers ID (MANID) - Offset F8h

Manufacturers ID register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:0] + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/P	**Manufacturers ID Field (MANID):** Manufacturer ID: Default value comes from straps.

8.2 UART Memory Mapped Registers Summary

Table 8-2. Summary of UART Memory Mapped Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	REG RBR (RBR)	00000000h
4h	4	REG DLH (DLH)	00000000h
8h	4	REG IIR (IIR)	00000001h
Ch	4	REG LCR (LCR)	00000000h
10h	4	REG MCR (MCR)	00000000h
14h	4	REG LSR (LSR)	00000060h
18h	4	REG MSR (MSR)	00000000h
1Ch	4	REG SCR (SCR)	00000000h
30h	4	REG SRBR_STHR0 (SRBR_STHR0)	00000000h
34h	4	REG SRBR_STHR1 (SRBR_STHR1)	00000000h
38h	4	REG SRBR_STHR2 (SRBR_STHR2)	00000000h
3Ch	4	REG SRBR_STHR3 (SRBR_STHR3)	00000000h
40h	4	REG SRBR_STHR4 (SRBR_STHR4)	00000000h
44h	4	REG SRBR_STHR5 (SRBR_STHR5)	00000000h
48h	4	REG SRBR_STHR6 (SRBR_STHR6)	00000000h
4Ch	4	REG SRBR_STHR7 (SRBR_STHR7)	00000000h
50h	4	REG SRBR_STHR8 (SRBR_STHR8)	00000000h
54h	4	REG SRBR_STHR9 (SRBR_STHR9)	00000000h
58h	4	REG SRBR_STHR10 (SRBR_STHR10)	00000000h
5Ch	4	REG SRBR_STHR11 (SRBR_STHR11)	00000000h
60h	4	REG SRBR_STHR12 (SRBR_STHR12)	00000000h
64h	4	REG SRBR_STHR13 (SRBR_STHR13)	00000000h
68h	4	REG SRBR_STHR14 (SRBR_STHR14)	00000000h
6Ch	4	REG SRBR_STHR15 (SRBR_STHR15)	00000000h
70h	4	REG FAR (FAR)	00000000h
74h	4	REG TFR (TFR)	00000000h
78h	4	REG RFW (RFW)	00000000h
7Ch	4	REG USR (USR)	00000006h
80h	4	REG TFL (TFL)	00000000h
84h	4	REG RFL (RFL)	00000000h
88h	4	REG SRR (SRR)	00000000h
8Ch	4	REG SRTS (SRTS)	00000000h
90h	4	REG SBCR (SBCR)	00000000h
94h	4	REG SDMAM (SDMAM)	00000000h
98h	4	REG SFE (SFE)	00000000h
9Ch	4	REG SRT (SRT)	00000000h
A0h	4	REG STET (STET)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
A4h	4	REG HTX (HTX)	00000000h
A8h	4	REG DMASA (DMASA)	00000000h
F4h	4	REG CPR (CPR)	00043F32h
200h	4	REG CLOCKS (CLOCKS)	00000000h
204h	4	REG RESETS (RESETS)	00000000h
210h	4	REG ACTIVELTR_VALUE (ACTIVELTR_VALUE)	00000800h
214h	4	REG IDLELTR_VALUE (IDLELTR_VALUE)	00000800h
218h	4	REG TX_BYTE_COUNT (TX_BYTE_COUNT)	00000000h
21Ch	4	REG RX_BYTE_COUNT (RX_BYTE_COUNT)	00000000h
228h	4	REG SW_SCRATCH_0 (SW_SCRATCH_0)	00000000h
238h	4	REG CLOCK_GATE (CLOCK_GATE)	00000000h
240h	4	REG REMAP_ADDR_LO (REMAP_ADDR_LO)	00000000h
244h	4	REG REMAP_ADDR_HI (REMAP_ADDR_HI)	00000000h
24Ch	4	REG DEVIDLE_CONTROL (DEVIDLE_CONTROL)	00000008h
280h	4	REG UART_HVM_MISR_CRCOUT (UART_HVM_MISR_CRCOUT)	0000FFFFh
2FCh	4	REG CAPABLITIES (CAPABLITIES)	00000010h
800h	4	REG SAR_LO0 (SAR_LO0)	00000000h
804h	4	REG SAR_HI0 (SAR_HI0)	00000000h
808h	4	REG DAR_LO0 (DAR_LO0)	00000000h
80Ch	4	REG DAR_HI0 (DAR_HI0)	00000000h
810h	4	REG LLP_LO0 (LLP_LO0)	00000000h
814h	4	REG LLP_HI0 (LLP_HI0)	00000000h
818h	4	REG CTL_LO0 (CTL_LO0)	00000000h
81Ch	4	REG CTL_HI0 (CTL_HI0)	00000000h
820h	4	REG SSTAT0 (SSTAT0)	00000000h
828h	4	REG DSTAT0 (DSTAT0)	00000000h
830h	4	REG SSTATAR_LO0 (SSTATAR_LO0)	00000000h
834h	4	REG SSTATAR_HI0 (SSTATAR_HI0)	00000000h
838h	4	REG DSTATAR_LO0 (DSTATAR_LO0)	00000000h
83Ch	4	REG DSTATAR_HI0 (DSTATAR_HI0)	00000000h
840h	4	REG CFG_LO0 (CFG_LO0)	00000203h
844h	4	REG CFG_HI0 (CFG_HI0)	00000000h
848h	4	REG SGR0 (SGR0)	00000000h
850h	4	REG DSR0 (DSR0)	00000000h
AC0h	4	REG RawTfr (RAWTFR)	00000000h
AC8h	4	REG RawBlock (RAWBLOCK)	00000000h
AD0h	4	REG RawSrcTran (RAWSRCTRAN)	00000000h
AD8h	4	REG RawDstTran (RAWDSTTRAN)	00000000h
AE0h	4	REG RawErr (RAWERR)	00000000h
AE8h	4	REG StatusTfr (STATUSTFR)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
AF0h	4	REG StatusBlock (STATUSBLOCK)	00000000h
AF8h	4	REG StatusSrcTran (STATUSSRCTRAN)	00000000h
B00h	4	REG StatusDstTran (STATUSDSTTRAN)	00000000h
B08h	4	REG StatusErr (STATUSERR)	00000000h
B10h	4	REG MaskTfr (MASKTFR)	00000000h
B18h	4	REG MaskBlock (MASKBLOCK)	00000000h
B20h	4	REG MaskSrcTran (MASKSRCTRAN)	00000000h
B28h	4	REG MaskDstTran (MASKDSTTRAN)	00000000h
B30h	4	REG MaskErr (MASKERR)	00000000h
B38h	4	REG ClearTfr (CLEARTFR)	00000000h
B40h	4	REG ClearBlock (CLEARBLOCK)	00000000h
B48h	4	REG ClearSrcTran (CLEARSRCTRAN)	00000000h
B50h	4	REG ClearDstTran (CLEARDSTTRAN)	00000000h
B58h	4	REG ClearErr (CLEARERR)	00000000h
B60h	4	REG StatusInt (STATUSINT)	00000000h
B98h	4	REG DmaCfgReg (DMACFGREG)	00000000h
BA0h	4	REG ChEnReg (CHENREG)	00000000h

8.2.1 REG RBR (RBR) - Offset 0h

Receive Buffer Register. RBR mode is only available when LCR register [7] (DLAB bit) = 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h R0	**Reserved**
7:0	00h RO	**RBR:** Data byte received on the serial input port (sin) in UART mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an over-run error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an over-run error occurs.

8.2.2 REG DLH (DLH) - Offset 4h

Divisor Latch (High). DLH mode is only available when LCR register [7] (DLAB bit) = 1

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h R0	**Reserved**
7:0	00h NA	**DLH:** Upper 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may be accessed only when the DLAB bit (LCR[7]) is set. The output baud rate is equal to the serial clock frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor).

8.2.3 REG IIR (IIR) - Offset 8h

Interrupt Control Register. The following table indicates the Interrupt Control

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8h	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved**
7:6	0h RO	**FIFOSE:** FIFOs Enabled. This is used to indicate whether the FIFOs are enabled or disabled. 00 = disabled 11 = enabled
5:4	0h RO	**Reserved**
3:0	1h RO	**IID:** Interrupt ID. This indicates the highest priority pending interrupt which can be one of the following types: 0000 = modem status 0001 = no interrupt pending 0010 = THR empty 0100 = received data available 0110 = receiver line status 0111 = busy detect 1100 = character timeout

8.2.4 REG LCR (LCR) - Offset Ch

Line Control Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved**
7	0h RW	**DLAB:** Divisor Latch Access Bit. If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. Reset Value: 0x0
6	0h RW	**BREAK:** Break Control Bit. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low
5	0h RO	**Reserved**
4	0h RW	**EPS:** Even Parity Select. If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked. Reset Value: 0x0

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**PEN:** Parity Enable. If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0 = parity disabled 1 = parity enabled Reset Value: 0x0
2	0h RW	**STOP:** Number of stop bits. If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bit is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0 = 1 stop bit 1 = 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit Reset Value: 0x0
1:0	0h RW	**DLS:** Data Length Select. If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits Reset Value: 0x0

8.2.5 REG MCR (MCR) - Offset 10h

Modem Control Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW	**AFCE:** Auto Flow Control Enable. Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set. 0 = Auto Flow Control Mode disabled 1 = Auto Flow Control Mode enabled Reset Value: 0x0
4	0h RW	**LOOPBACK:** LoopBack Bit. This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line. Reset Value: 0x0
3:2	0h RO	**Reserved**
1	0h RW	**RTS:** Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high.In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0
0	0h RO	**Reserved**

8.2.6 REG LSR (LSR) - Offset 14h

Line Status Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14h	00000060h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**RFE:** Receiver FIFO Error bit. This bit is only relevant when FIFO_MODE != NONE AND FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. 0 = no error in RX FIFO 1 = error in RX FIFO This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO. Reset Value: 0x0
6	1h RW	**TEMT:** Transmitter Empty bit. If in FIFO mode (FIFO_MODE != NONE) and FIFOs enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in non-FIFO mode or FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty. Reset Value: 0x1
5	1h RW	**THRE:** Transmit Holding Register Empty bit. If THRE_MODE_USER == Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting. Reset Value: 0x1
4	0h RW	**BI:** Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read. Reset Value: 0x0

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**FE:** Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0 = no framing error 1 = framing error Reading the LSR clears the FE bit. Reset Value: 0x0
2	0h RW	**PE:** Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0 = no parity error 1 = parity error Reading the LSR clears the PE bit. Reset Value: 0x0
1	0h RW	**OE:** Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0 = no overrun error 1 = overrun error Reading the LSR clears the OE bit. Reset Value: 0x0
0	0h RW	**DR:** Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0 = no data ready 1 = data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode. Reset Value: 0x0

8.2.7 REG MSR (MSR) - Offset 18h

Modem Status Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**CTS:** Clear to Send. This is used to indicate the current state of the modem control line cts_n.This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the UART. 0 = cts_n input is de-asserted (logic 1) 1 = cts_n input is asserted (logic 0)
3:1	0h RO	**Reserved**
0	0h RO	**DCTS:** Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0 = no change on cts_n since last read of MSR 1 = change on cts_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS).Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs(software or otherwise), then the DCTS bit is set when the reset is removed if the cts_nsignal remains asserted.

8.2.8 REG SCR (SCR) - Offset 1Ch

Scratchpad Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved**
7:0	00h RW	**SCR:** This register is for programmers to use as a temporary storage space. It has no defined purpose in the DW_apb_uart. Reset Value: 0x0

8.2.9 REG SRBR_STHR0 (SRBR_STHR0) - Offset 30h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SRBR_STHR0:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

8.2.10 REG SRBR_STHR1 (SRBR_STHR1) - Offset 34h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 1

Type	Size	Offset	Default
MMIO	32 bit	BAR + 34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SRBR_STHR1:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode

8.2.11 REG SRBR_STHR2 (SRBR_STHR2) - Offset 38h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 2

Type	Size	Offset	Default
MMIO	32 bit	BAR + 38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SRBR_STHR2:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise

8.2.12 REG SRBR_STHR3 (SRBR_STHR3) - Offset 3Ch

Shadow Receive Buffer Register and Shadow Transmit Holding Register 3

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SRBR_STHR3:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

8.2.13 REG SRBR_STHR4 (SRBR_STHR4) - Offset 40h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 4

Type	Size	Offset	Default
MMIO	32 bit	BAR + 40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SRBR_STHR4:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

8.2.14 REG SRBR_STHR5 (SRBR_STHR5) - Offset 44h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 5

Type	Size	Offset	Default
MMIO	32 bit	BAR + 44h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SRBR_STHR5:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register.

8.2.15 REG SRBR_STHR6 (SRBR_STHR6) - Offset 48h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 6

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SRBR_STHR6:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

8.2.16 REG SRBR_STHR7 (SRBR_STHR7) - Offset 4Ch

Shadow Receive Buffer Register and Shadow Transmit Holding Register 7

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SRBR_STHR7:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x

8.2.17 REG SRBR_STHR8 (SRBR_STHR8) - Offset 50h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 8

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SRBR_STHR8:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

8.2.18 REG SRBR_STHR9 (SRBR_STHR9) - Offset 54h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 9

Type	Size	Offset	Default
MMIO	32 bit	BAR + 54h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SRBR_STHR9:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

8.2.19 REG SRBR_STHR10 (SRBR_STHR10) - Offset 58h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 10

Type	Size	Offset	Default
MMIO	32 bit	BAR + 58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SRBR_STHR10:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

8.2.20 REG SRBR_STHR11 (SRBR_STHR11) - Offset 5Ch

Shadow Receive Buffer Register and Shadow Transmit Holding Register 11

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SRBR_STHR11:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

8.2.21 REG SRBR_STHR12 (SRBR_STHR12) - Offset 60h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 12

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SRBR_STHR12:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

8.2.22 REG SRBR_STHR13 (SRBR_STHR13) - Offset 64h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 13

Type	Size	Offset	Default
MMIO	32 bit	BAR + 64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SRBR_STHR13:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

8.2.23 REG SRBR_STHR14 (SRBR_STHR14) - Offset 68h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 14

Type	Size	Offset	Default
MMIO	32 bit	BAR + 68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SRBR_STHR14:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

8.2.24 REG SRBR_STHR15 (SRBR_STHR15) - Offset 6Ch

Shadow Receive Buffer Register and Shadow Transmit Holding Register 15

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SRBR_STHR15:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

8.2.25 REG FAR (FAR) - Offset 70h

FIFO Access Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**SRBR_STHR:** Writes have no effect when FIFO_ACCESS == No, always readable. This register is used to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFOs are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. 0 = FIFO access mode disabled 1 = FIFO access mode enabled Note, that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFOs are treated as empty. Reset Value: 0x0

8.2.26 REG TFR (TFR) - Offset 74h

Transmit FIFO Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 74h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**TFR:** Transmit FIFO Read. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO. When FIFOs are not implemented or not enabled, reading this register gives the data in the THR. Reset Value: 0x0

8.2.27 REG RFW (RFW) - Offset 78h

Receive FIFO Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 78h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	000000h RO	**Reserved**
9	0h WO	**RFFE:** Receive FIFO Framing Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are enabled, this bit is used to write framing error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write framing error detection information to the RBR.
8	0h WO	**RFPE:** Receive FIFO Parity Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are enabled, this bit is used to write parity error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write parity error detection information to the RBR.
7:0	00h WO	**RFWD:** Receive FIFO Write Data. These bits are only valid when FIFO access mode is enabled(FAR[0] is set to one). When FIFOs are enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFOs are not implemented or not enabled, the data that is written to the RFWD is pushed into the RBR.

8.2.28 REG USR (USR) - Offset 7Ch

UART Status Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7Ch	00000006h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**RFF:** Receive FIFO Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO is completely full. 0 = Receive FIFO not full 1 = Receive FIFO Full This bit is cleared when the RX FIFO is no longer full. Reset Value: 0x0
3	0h RO	**RFNE:** Receive FIFO Not Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO contains one or more entries. 0 = Receive FIFO is empty 1 = Receive FIFO is not empty This bit is cleared when the RX FIFO is empty. Reset Value: 0x0

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO	**TFE:** Transmit FIFO Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is completely empty. 0 = Transmit FIFO is not empty 1 = Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty. Reset Value: 0x1
1	1h RO	**TFNF:** Transmit FIFO Not Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO in not full. 0 = Transmit FIFO is full 1 = Transmit FIFO is not full This bit is cleared when the TX FIFO is full. Reset Value: 0x1
0	0h RO	**BUSY:** UART Busy. This bit is valid only when UART_16550_COMPATIBLE == NO and indicates that a serial transfer is in progress, when cleared, indicates that the DW_apb_uart is idle or inactive. 0 = DW_apb_uart is idle or inactive 1 = DW_apb_uart is busy (actively transferring data) NOTE: It is possible for the UART Busy bit to be cleared even though a new character may have been sent from another device. That is, if the DW_apb_uart has no data in THR and RBR and there is no transmission in progress and a start bit of a new character has just reached the DW_apb_uart. This is due to the fact that a valid start is not seen until the middle of the bit period and this duration is dependent on the baud divisor that has been programmed. If a second system clock has been implemented (CLOCK_MODE == Enabled), the assertion of this bit is also delayed by several cycles of the slower clock. Reset Value: 0x0

8.2.29 REG TFL (TFL) - Offset 80h

Transmit FIFO Level

Type	Size	Offset	Default
MMIO	32 bit	BAR + 80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RO	**TFL:** Transmit FIFO Level. This indicates the number of data entries in the transmit FIFO. Reset Value: 0x0

8.2.30 REG RFL (RFL) - Offset 84h

Receive FIFO Level

Type	Size	Offset	Default
MMIO	32 bit	BAR + 84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RO	**RFL:** Receive FIFO Level. This indicates the number of data entries in the receive FIFO. Reset Value: 0x0

8.2.31 REG SRR (SRR) - Offset 88h

Software Reset Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW	**XFR:** XMIT FIFO Reset. This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0 Dependencies: Writes have no effect when FIFO_MODE == None.
1	0h RW	**RFR:** RCVR FIFO Reset. This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO. This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0 Dependencies: Writes have no effect when FIFO_MODE == None.
0	0h RW	**UR:** UART Reset. This asynchronously resets the DW_apb_uart and synchronously removes the reset assertion. For a two clock implementation both pclk and sclk domains are reset. Reset Value: 0x0

8.2.32 REG SRTS (SRTS) - Offset 8Ch

Shadow Request to Send

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**SRTS:** Shadow Request to Send. This is a shadow register for the RTS bit (MCR[1]), this can be used to remove the burden of having to performing a read-modify-write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the DW_apb_uart is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] = 0), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] = 1) and FIFOs enable (FCR[0] = 1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). Note that in Loopback mode (MCR[4] = 1), the rts_n output is held inactive-high while the value of this location is internally looped back to an input. Reset Value: 0x0

8.2.33 REG SBCR (SBCR) - Offset 90h

Shadow Break Control Bit.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**SBCB:** Shadow Break Control Register

8.2.34 REG SDMAM (SDMAM) - Offset 94h

Shadow DMA Mode

Type	Size	Offset	Default
MMIO	32 bit	BAR + 94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**SDMAM:** Shadow DMA Mode. This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. This determines the DMA signaling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == NO). 0 = mode 0 1 = mode 1 Reset Value: 0x0

8.2.35 REG SFE (SFE) - Offset 98h

Shadow FIFO Enable

Type	Size	Offset	Default
MMIO	32 bit	BAR + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**SFE:** Shadow FIFO Enable. This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated. This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs are reset. Reset Value: 0x0

8.2.36 REG SRT (SRT) - Offset 9Ch

Shadow RCVR Trigger

Type	Size	Offset	Default
MMIO	32 bit	BAR + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**SRT:** Shadow RCVR Trigger. This is a shadow register for the RCVR trigger bits (FCR[7:6]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the RCVR trigger bit gets updated. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. It also determines when the dma_rx_req_n signal is asserted when DMA Mode (FCR[3]) = 1. The following trigger levels are supported: 00 = 1 character in the FIFO 01 = FIFO full 10 = FIFO full 11 = FIFO 2 less than full Reset Value: 0x0

8.2.37 REG STET (STET) - Offset A0h

Shadow TX Empty Trigger.

Type	Size	Offset	Default
MMIO	32 bit	BAR + A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**STET:** Shadow TX Empty Trigger: This is a shadow register for the TX empty trigger bits(FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported: 00 = FIFO empty 01 = 2 characters in the FIFO 10 = FIFO 1/4 full 11 = FIFO 1/2 full

8.2.38 REG HTX (HTX) - Offset A4h

Halt TX

Type	Size	Offset	Default
MMIO	32 bit	BAR + A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**HTX:** This register is used to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0 = Halt TX disabled 1 = Halt TX enabled Note, if FIFOs are implemented and not enabled, the setting of the halt TX register has no effect on operation. Reset Value: 0x0 Dependencies: Writes have no effect when FIFO_MODE == None.

8.2.39 REG DMASA (DMASA) - Offset A8h

DMA Software Acknowledge

Type	Size	Offset	Default
MMIO	32 bit	BAR + A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h WO	**DMASA:** This register is used to perform a DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the DW_apb_uart should clear its request. This causes the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0 Dependencies: Writes have no effect when DMA_EXTRA == No.

8.2.40 REG CPR (CPR) - Offset F4h

Component Parameter Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + F4h	00043F32h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	04h RO	**FIFO_MODE:** 0x00 = 0 0x01 = 16 0x02 = 32 to 0x80 = 2048
15:14	0h RO	**Reserved**
13	1h RO	**DMA_EXTRA:** 0 = FALSE, 1 = TRUE
12	1h RO	**UART_ADD_ENCODED_PARAMS:** 0 = FALSE, 1 = TRUE
11	1h RO	**SHADOW:** 0 = FALSE, 1 = TRUE
10	1h RO	**FIFO_STAT:** 0 = FALSE, 1 = TRUE
9	1h RO	**FIFO_ACCESS:** 0 = FALSE, 1 = TRUE
8	1h RO	**ADDITIONAL_FEAT:** 0 = FALSE, 1 = TRUE
7	0h RO	**SIR_LP_MODE:** 0 = FALSE, 1 = TRUE
6	0h RO	**SIR_MODE:** 0 = FALSE, 1 = TRUE
5	1h RO	**THRE_MODE:** 0 = FALSE, 1 = TRUE
4	1h RO	**AFCE_MODE:** 0 = FALSE, 1 = TRUE
3:2	0h RO	**Reserved**
1:0	2h RO	**APB_DATA_WIDTH:** 00 = 8 bits

8.2.41 REG CLOCKS (CLOCKS) - Offset 200h

Private Clock Configuration

Type	Size	Offset	Default
MMIO	32 bit	BAR + 200h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**CLK_UPDATE:** Update the clock divider after setting new m and n values, 0 - No clock Update , 1 - Clock gets updated.
30:16	0000h RW	**N_VAL:** This is the denominator value (N) for the M over N divider logic that creates CLK_OUT. Used to generate the input CLK to the UART.
15:1	0000h RW	**M_VAL:** The numerator value (M) for the M over N divider logic that creates the CLK_OUT. Used to generate the input CLK to the UART.
0	0h RW	**CLK_EN:** UART Serial Clock (output of M/N, input to UART) Clock Enable 0 Clock disabled 1 Clock Enabled.

8.2.42 REG RESETS (RESETS) - Offset 204h

Software Reset

Type	Size	Offset	Default
MMIO	32 bit	BAR + 204h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW	**RESET_DMA:** reset the DMA controller, 0 = IP is in reset (Reset Asserted) 1 = IP is NOT at reset (Reset Released)
1:0	0h RW	**RESET_IP:** IUART Host Controller reset. Used to reset the I2C Host Controller by SW control. All I2C Configuration State and Operational State will be forced to the Default state. There is no timing requirement (SW can assert and de-assert in back to back transactions) This reset does NOT impact the LPSS cluster level settings by BIOS, the PCI configuration header information, DMA channel configuration and interrupt assignment/mapping/etc. Driver should re-initialize registers related to Driver context following an UART host controller reset. 00 = UART Host Controller is in reset (Reset Asserted) 01 = Reserved 10 = Reserved 11 = UART Host Controller is NOT at reset (Reset Released)

8.2.43 REG ACTIVELTR_VALUE (ACTIVELTR_VALUE) - Offset 210h

ACTIVELTR_VALUE_Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 210h	00000800h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**SNOOP_REQUIRMENT:** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10 -bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	**Reserved**
12:10	2h RW	**SNOOP_LATENCY_SCALE:** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which do not match those values will be dropped completely, next read will return previous value.
9:0	000h RW	**SNOOP_VALUE:** 10-bit latency value

8.2.44 REG IDLELTR_VALUE (IDLELTR_VALUE) - Offset 214h

IDLELTR_VALUE_Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 214h	00000800h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**SNOOP_REQUIRMENT:** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10 -bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RO	**Reserved**
12:10	2h RW	**SNOOP_LATENCY_SCALE:** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which do not match those values will be dropped completely, next read will return previous value.
9:0	000h RW	**SNOOP_VALUE:** 10-bit latency value

8.2.45 REG TX_BYTE_COUNT (TX_BYTE_COUNT) - Offset 218h

TX_BYTE_COUNT_Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 218h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**TX_COUNT_OVERFLOW:** 0= count valid 1= count overflow/invalid
30:24	0h RO	**Reserved**
23:0	000000h RO	**TX_BYTE_COUNT:** tx_byte_count

8.2.46 REG RX_BYTE_COUNT (RX_BYTE_COUNT) - Offset 21Ch

RX_BYTE_COUNT_Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 21Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**RX_COUNT_OVERFLOW:** 0= count valid 1= count overflow/invalid
30:24	0h RO	**Reserved**
23:0	000000h RO	**RX_BYTE_COUNT:** rx_byte_count

8.2.47 REG SW_SCRATCH_0 (SW_SCRATCH_0) - Offset 228h

SW_SCRATCH_0_Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 228h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SW_SCRATCH_0:** Scratch Pad Register for SW to generated Local DATA for iDMA

8.2.48 REG CLOCK_GATE (CLOCK_GATE) - Offset 238h

CLOCK_GATE_Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 238h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:2	0h RW	**SW_DMA_CLK_CTL:** Dma Clock Gate Control bits, 00-hw clk en, 01-rsv, 10-force off, 11-force on
1:0	0h RW	**SW_IP_CLK_CTL:** IP Clock Gate Control bits, 00-hw clk en, 01-rsv, 10-force off, 11-force on

8.2.49 REG REMAP_ADDR_LO (REMAP_ADDR_LO) - Offset 240h

REMAP_ADDR_LO_Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 240h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**UART_REMAP_ADDR_LOW:** Low 32 bits of BAR address read by SW

8.2.50 REG REMAP_ADDR_HI (REMAP_ADDR_HI) - Offset 244h

REMAP_ADDR_HI_Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 244h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**UART_REMAP_ADDR_HIGH:** High 32 bits of BAR address read by SW

8.2.51 REG DEVIDLE_CONTROL (DEVIDLE_CONTROL) - Offset 24Ch

This register allows a device driver to enable/disable a devices entry into DevIdle. By enabling DevIdle, SW specifies that it will not touch the device without accessing this register prior to accessing any other MMIO device register. Detailed SW DevIdle entry/exit flows are defined in the Chassis Power Management and Device Idle PFAS specifications

Type	Size	Offset	Default
MMIO	32 bit	BAR + 24Ch	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**INTR_REQ_CAPABLE:** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0.
3	1h RW/1C	**RESTORE_REQUIRED:** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**DEVIDLE:** SW sets this bit to 1 to move the function into the DevIdle state. Writing this bit to 0 will return the function to the fully active D0 state (D0i0)
1	0h RO	Reserved
0	0h RO	**CMD_IN_PROGRESS:** HW sets this bit on a 1->0 or 0->1 transition of DEVIDLE. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. HW clears this bit upon completing the DevIdle transition command. When clear, all the other bits in the register are valid and SW may write to any bit. If Interrupt Request (IR) was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect.

8.2.52 REG UART_HVM_MISR_CRCOUT (UART_HVM_MISR_CRCOUT) - Offset 280h

UART HVM MISR CRCOUT

Type	Size	Offset	Default
MMIO	32 bit	BAR + 280h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	FFFFh RO	**UART_HVM_MISR_CRCOUT:** UART MISR Output for HVM

8.2.53 REG CAPABLITIES (CAPABLITIES) - Offset 2FCh

Capabilities Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2FCh	00000010h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RO	**IDMA_PRESENT:** 0= DMA present 1= DMA not present
7:4	1h RO	**INSTANCE_TYPE:** I2C, SPI or UART
3:0	0h RO	**INSTANCE_NUMBER:** Instance number

8.2.54 REG SAR_LO0 (SAR_LO0) - Offset 800h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer. Source Address Register for lower 32-bits for Channels 0-1

Type	Size	Offset	Default
MMIO	32 bit	BAR + 800h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SAR_LO:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP-based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected). 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.2.55 REG SAR_HI0 (SAR_HI0) - Offset 804h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer. Source Address Register for upper 32-bits for Channels 0-1

Type	Size	Offset	Default
MMIO	32 bit	BAR + 804h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SAR_HI:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.2.56 REG DAR_LO0 (DAR_LO0) - Offset 808h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer. Destination Address Register for Channels 0-1

Type	Size	Offset	Default
MMIO	32 bit	BAR + 808h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DAR_LO:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.2.57 REG DAR_HI0 (DAR_HI0) - Offset 80Ch

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer. Destination Address Register for Upper 32-bits for Channels 0-1

Type	Size	Offset	Default
MMIO	32 bit	BAR + 80Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DAR_HI:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.2.58 REG LLP_LO0 (LLP_LO0) - Offset 810h

You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled. The LLP register has two functions: The logical result of the equation LLP.LOC!= 0is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC!= 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists. The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 810h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**Reserved**

8.2.59 REG LLP_HI0 (LLP_HI0) - Offset 814h

You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled. The LLP register has two functions: The logical result of the equation LLP.LOC != 0is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC!= 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 814h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot b changed or programmed to anything other than 32-bit.

8.2.60 REG CTL_LO0 (CTL_LO0) - Offset 818h

This register contains fields that control the DMA transfer. The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 818h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Reserved (00) Memory to Peripheral (01) Peripheral to Memory (10) Reserved (11) Flow Control is always assigned to the DMA.
19	0h RO	**Reserved**
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gathers enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. Source BURST SIZE (in DW) = (2 ^ SRC_TR_WIDTH)
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**Reserved**
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE (IN DW) = (2^ MSIZE) (i.e. 2 to-the-power-of MSIZE) 1.Transferred Bytes Per Burst = BURST_SIZE * (2 ^ TR_WIDTH) Since Max Burst Length is limited by the OCP fabric to 16 DW, encodings 101 (32 DW), 110 (64 DW) and 111 (128 DW) are not supported by the fabric. 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
3:1	0h RW	**DST_TR_WIDTH:** BURST SIZE (in DW) = (2^ MSIZE) (i.e. 2 to-the-power-of MSIZE) Transferred Bytes Per Burst = BURST_SIZE * (2 ^ TR_WIDTH) Since Max Burst Length is limited by the South-Complex OCP fabric to 16 DW, encodings 101 (32 DW), 110 (64 DW) and 111 (128 DW) are not supported by the fabric. For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.2.61 REG CTL_HI0 (CTL_HI0) - Offset 81Ch

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled. If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 81Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.

Bit Range	Default & Access	Field Name (ID): Description
28:18	0h RO	**Reserved**
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	00000h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It does not mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register.

8.2.62 REG SSTAT0 (SSTAT0) - Offset 820h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block

Type	Size	Offset	Default
MMIO	32 bit	BAR + 820h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.2.63 REG DSTAT0 (DSTAT0) - Offset 828h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI.

This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 828h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface

8.2.64 REG SSTATAR_LO0 (SSTATAR_LO0) - Offset 830h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 830h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTATAR_LO:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block

8.2.65 REG SSTATAR_HI0 (SSTATAR_HI0) - Offset 834h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 834h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTATAR_HI:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block

8.2.66 REG DSTATAR_LO0 (DSTATAR_LO0) - Offset 838h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 838h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTATAR_LO:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.2.67 REG DSTATAR_HI0 (DSTATAR_HI0) - Offset 83Ch

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 83Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTATAR_HI:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.2.68 REG CFG_LO0 (CFG_LO0) - Offset 840h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Type	Size	Offset	Default
MMIO	32 bit	BAR + 840h	00000203h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0h RO	**Reserved**
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length: 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE))
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length: 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE))
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17:11	0h RO	**Reserved**
10	0h RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit affects only when CH_SUSPEND is asserted
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**Reserved**
3	0h RW	**HSHAKE_NP_WR:** 0x1: Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0: Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1: Forces ALL writes to be Non-Posted on DMA Write Port 0x0: Non-Posted Writes will only be used at end of block transfers and in HW Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used
1	1h RW	**SRC_BURST_ALIGN:** 0x1: SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0: SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1: DST Burst Transfers are broken at a Burst Length aligned boundary 0x0: DST Burst Transfers are not broken at a Burst Length aligned boundary

8.2.69 REG CFG_HI0 (CFG_HI0) - Offset 844h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Type	Size	Offset	Default
MMIO	32 bit	BAR + 844h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:18	000h RW	**WR_ISSUE_THD:** Write Issue Threshold. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
17:8	000h RW	**RD_ISSUE_THD:** Read Issue Threshold. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID: Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface.
3:0	0h RW	**SRC_PER:** Source Peripheral ID: Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface.

8.2.70 REG SGR0 (SGR0) - Offset 848h

The Source Gather register contains two fields: Source gathers count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gathers interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 848h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	00000h RW	**SGI:** Source gather interval.

8.2.71 REG DSR0 (DSR0) - Offset 850h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC). Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI). Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 850h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries
19:0	00000h RW	**DSI:** Destination scatter interval.

8.2.72 REG RawTfr (RAWTFR) - Offset AC0h

Interrupt events are stored in this Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers

Type	Size	Offset	Default
MMIO	32 bit	BAR + AC0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**RAW:** Raw Interrupt Status for Ch1 And Ch0

8.2.73 REG RawBlock (RAWBLOCK) - Offset AC8h

RawBlock - Raw Status for Block Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + AC8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**RAW:** Raw Interrupt Status for Ch1 And Ch0

8.2.74 REG RawSrcTran (RAWSRCTRAN) - Offset AD0h

RawSrcTran - Raw Status for Source Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + AD0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**RAW:** Raw Interrupt Status for Ch1 And Ch0

8.2.75 REG RawDstTran (RAWDSTTRAN) - Offset AD8h

RawDstTran - Raw Status for Destination Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + AD8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**RAW:** Raw Interrupt Status for Ch1 And Ch0

8.2.76 REG RawErr (RAWERR) - Offset AE0h

RawErr - Raw Status for Error Interrupts Register Error interrupt will be asserted by the DMA in the following cases:

IOSF Fabric returns an Unsuccessful Completion with UR Completion Status for a Non-Posted transaction issued by the DMA to Memory. This error occurs when an invalid address range is programed into the DMA SRC/Dest Field outside of the Host memory region on the memory side of the DMA transaction IOSF2OCP bridge will return error (triggering error interrupt from DMA) if the IOSF2OCP Bridge is programmed incorrectly.

Peripheral side transactions where invalid addressing can result in an OCP fabric error which will be translated into an Error Interrupt The SW should view this error as a serious programming error and handle it according to the specified error handling procedures for the product and OS.

Type	Size	Offset	Default
MMIO	32 bit	BAR + AE0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**RAW:** Raw Interrupt Status for Ch1 And Ch0

8.2.77 REG StatusTfr (STATUSTFR) - Offset AE8h

Status for Transfer Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + AE8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**STATUS:** Status for Interrupt for Ch1 And Ch0

8.2.78 REG StatusBlock (STATUSBLOCK) - Offset AF0h

StatusBlock: Status for Block Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + AF0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**STATUS:** Status for Interrupt for Ch1 And Ch0

8.2.79 REG StatusSrcTran (STATUSSRCTRAN) - Offset AF8h

StatusSrcTran: Status for Source Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + AF8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**STATUS:** Status for Interrupt for Ch1 And Ch0

8.2.80 REG StatusDstTran (STATUSDSTTRAN) - Offset B00h

StatusDstTran: Status for Destination Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B00h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**STATUS:** Status for Interrupt for Ch1 And Ch0

8.2.81 REG StatusErr (STATUSERR) - Offset B08h

StatusErr, Status for Error Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B08h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**STATUS** Status for Interrupt for Ch1 And Ch0

8.2.82 REG MaskTfr (MASKTFR) - Offset B10h

Mask for Transfer Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable Ch1 and Ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	**Reserved**
1:0	0h RW	**INT_MASK:** Interrupt Mask per Ch1 and Ch0. 0 = mask 1 = unmask

8.2.83 REG MaskBlock (MASKBLOCK) - Offset B18h

MaskBlock: Mask for Block Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable Ch1 and Ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	**Reserved**
1:0	0h RW	**INT_MASK:** Interrupt Mask Ch1 and Ch0. 0 = mask 1 = unmask

8.2.84 REG MaskSrcTran (MASKSRCTRAN) - Offset B20h

Mask for Source Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable Ch1 and Ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	**Reserved**
1:0	0h RW	**INT_MASK:** Interrupt Mask Ch1 and Ch0. 0 = mask 1 = unmask

8.2.85 REG MaskDstTran (MASKDSTTRAN) - Offset B28h

Mask for Destination Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B28h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable Ch1 and Ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	**Reserved**
1:0	0h RW	**INT_MASK:** Interrupt Mask Ch1 and Ch0. 0 = mask 1 = unmask

8.2.86 REG MaskErr (MASKERR) - Offset B30h

Mask for Error Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable Ch1 and Ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	**Reserved**
1:0	0h RW	**INT_MASK:** Interrupt Mask Ch1 and Ch0. 0 = mask 1 = unmask

8.2.87 REG ClearTfr (CLEARTFR) - Offset B38h

Clear for Transfer Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h WO	**CLEAR:** Interrupt Clear Ch1 and Ch0. 0 = no effect 1 = clear interrupt

8.2.88 REG ClearBlock (CLEARBLOCK) - Offset B40h

Clear for Block Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h WO	**CLEAR:** Interrupt Clear Ch1 and Ch0. 0 = no effect 1 = clear interrupt

8.2.89 REG ClearSrcTran (CLEARSRCTRAN) - Offset B48h

Clear for Source Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h WO	**CLEAR:** Interrupt Clear Ch1 and Ch0. 0 = no effect 1 = clear interrupt

8.2.90 REG ClearDstTran (CLEARDSTTRAN) - Offset B50h

Clear for Destination Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h WO	**CLEAR:** Interrupt Clear Ch1 and Ch0. 0 = no effect 1 = clear interrupt

8.2.91 REG ClearErr (CLEARERR) - Offset B58h

Clear for Error Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h WO	**CLEAR:** Interrupt Clear Ch1 and Ch0. 0 = no effect 1 = clear interrupt

8.2.92 REG StatusInt (STATUSINT) - Offset B60h

The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran, StatusErr is ORed to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**ERR:** OR of the contents of StatusErr register.
3	0h RO	**DSTT:** OR of the contents of StatusDst register.
2	0h RO	**SRCT:** OR of the contents of StatusSrcTran register
1	0h RO	**BLOCK:** OR of the contents of StatusBlock register.
0	0h RO	**TFR:** OR of the contents of StatusTfr register.

8.2.93 REG DmaCfgReg (DMACFGREG) - Offset B98h

This register is used to enable the DMA, which must be done before any channel activity can begin. If the global channel enable bit is cleared while any channel is still active, then DmaCfgReg.DMA_EN still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DmaCfgReg.DMA_EN bit returns 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**DMA_EN:** DMA Enable bit. 0 = DMA Disabled 1 = DMA Enabled

8.2.94 REG ChEnReg (CHENREG) - Offset BA0h

This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive, it can then enable an inactive channel with the required priority.

All bits of this register are cleared to 0 when the global DMA channel enable bit, DmaCfgReg(0), is 0. When the global channel enable bit is 0, then a write to the ChEnReg register is ignored and a read will always read back 0. The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE, is asserted on the same OCP write transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BA0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:8	0h WO	**CH_EN_WE:** Channel Enable Write Enable
7:2	0h RO	**Reserved**
1:0	0h RW	**CH_EN:** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

8.3 UART PCR Registers Summary

Table 8-3. Summary of UART PCR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
218h	4	PCICFGCTR7 PCI Configuration Control 7 Register (PCICFGCTR7)	00000100h
21Ch	4	PCICFGCTR8 PCI Configuration Control 8 Register (PCICFGCTR8)	00000100h
220h	4	PCICFGCTR9 PCI Configuration Control 9 Register (PCICFGCTR9)	00000100h
224h	4	PCICFGCTR10 PCI Configuration Control 10 Register (PCICFGCTR10)	00000100h
228h	4	PCICFGCTR11 PCI Configuration Control 11 Register (PCICFGCTR11)	00000100h
22Ch	4	PCICFGCTR12 PCI Configuration Control 12 Register (PCICFGCTR12)	00000100h

8.3.1 PCICFGCTR7 PCI Configuration Control 7 Register (PCICFGCTR7) - Offset 218h

Controls The PCI Configuration Space

Type	Size	Offset	Default
MMIO	32 bit	FDCD0000h + 218h	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RO	**Reserved**
27:20	00h RW	**PCI_IRQ7:** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	00h RW	**ACPI_IRQ7:** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	1h RW	**IPIN7:** Interrupt Pin: This register indicates the values to be used for Global Interrupts.
7	0h RW	**BAR1_DISABLE7:** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	00h RW	**PME_SUPPORT7:** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI_INTR_EN7:** When set, the Bridge uses ACPI Sideband opcodes for messages When cleared, the Bridge uses global IOSF opcodes
0	0h RW	**PCI_CFG_DIS7:** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

8.3.2 PCICFGCTR8 PCI Configuration Control 8 Register (PCICFGCTR8) - Offset 21Ch

Controls The PcI Configuration Space

Type	Size	Offset	Default
MMIO	32 bit	FDCD0000h + 21Ch	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RO	**Reserved**
27:20	00h RW	**PCI_IRQ8:** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	00h RW	**ACPI_IRQ8:** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	1h RW	**IPIN8:** Interrupt Pin: This register indicates the values to be used for Global Interrupts.
7	0h RW	**BAR1_DISABLE8:** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	00h RW	**PME_SUPPORT8:** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI_INTR_EN8:** When set, the Bridge uses ACPI Sideband opcodes for messages When cleared, the Bridge uses global IOSF opcodes
0	0h RW	**PCI_CFG_DIS8:** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

8.3.3 PCICFGCTR9 PCI Configuration Control 9 Register (PCICFGCTR9) - Offset 220h

Controls the PCI configuration space

Type	Size	Offset	Default
MMIO	32 bit	FDCD0000h + 220h	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RO	**Reserved**
27:20	00h RW	**PCI_IRQ9:** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	00h RW	**ACPI_IRQ9:** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	1h RW	**IPIN9:** Interrupt Pin: This register indicates the values to be used for Global Interrupts.
7	0h RW	**BAR1_DISABLE9:** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	00h RW	**PME_SUPPORT9:** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI_INTR_EN9:** When set, the Bridge uses ACPI Sideband opcodes for messages When cleared, the Bridge uses global IOSF opcodes
0	0h RW	**PCI_CFG_DIS9:** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

8.3.4 PCICFGCTR10 PCI Configuration Control 10 Register (PCICFGCTR10) - Offset 224h

Controls The PCI Configuration Space

Type	Size	Offset	Default
MMIO	32 bit	FDCD0000h + 224h	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RO	**Reserved**
27:20	00h RW	**PCI_IRQ10:** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	00h RW	**ACPI_IRQ10:** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	1h RW	**IPIN10:** Interrupt Pin: This register indicates the values to be used for Global Interrupts.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**BAR1_DISABLE10:** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	00h RW	**PME_SUPPORT10:** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI_INTR_EN10:** When set, the Bridge uses ACPI Sideband opcodes for messages When cleared, the Bridge uses global IOSF opcodes
0	0h RW	**PCI_CFG_DIS10:** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

8.3.5 PCICFGCTR11 PCI Configuration Control 11 Register (PCICFGCTR11) - Offset 228h

Controls the PCI configuration space

Type	Size	Offset	Default
MMIO	32 bit	FDCD0000h + 228h	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RO	**Reserved**
27:20	00h RW	**PCI_IRQ11:** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	00h RW	**ACPI_IRQ11:** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	1h RW	**IPIN11:** Interrupt Pin: This register indicates the values to be used for Global Interrupts.
7	0h RW	**BAR1_DISABLE11:** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	00h RW	**PME_SUPPORT11:** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI_INTR_EN11:** When set, the Bridge uses ACPI Sideband opcodes for messages When cleared, the Bridge uses global IOSF opcodes
0	0h RW	**PCI_CFG_DIS11:** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

8.3.6 PCICFGCTR12 PCI Configuration Control 12 Register (PCICFGCTR12) - Offset 22Ch

Controls the PCI configuration space

Type	Size	Offset	Default
MMIO	32 bit	FDCD0000h + 22Ch	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RO	**Reserved**
27:20	00h RW	**PCI_IRQ12:** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	00h RW	**ACPI_IRQ12:** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	1h RW	**IPIN12:** Interrupt Pin: This register indicates the values to be used for Global Interrupts.
7	0h RW	**BAR1_DISABLE12:** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	00h RW	**PME_SUPPORT12:** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI_INTR_EN12:** When set, the Bridge uses ACPI Sideband opcodes for messages When cleared, the Bridge uses global IOSF opcodes
0	0h RW	**PCI_CFG_DIS12:** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

9 Generic Serial Peripheral Interface (GSPI) Controller

9.1 GSPI Configuration Registers Summary

This chapter documents the registers in Bus: 0, Device 30, Function 2 and 3. Also lists the registers in Bus 0, Device 18, Function 0.

DID Values:

- GSPI Controller #0:- D30:F2 - 4B2Ah
- GSPI Controller #1:- D30:F3 - 4B2Bh
- GSPI Controller #2:- D18:F0 - 4B37h

Table 9-1. Summary of Bus: 0, Device: 30, Function: 2 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID And Vendor ID Register (DEVVENDID)	4B2A8086h
4h	4	Status And Command (STATUSCOMMAND)	00100000h
8h	4	Revision ID And Class Code (REVCLASSCODE)	0C800000h
Ch	4	Cache Line Latency Header And BIST (CLLATHEADERBIST)	00800000h
10h	4	Base Address Register (BAR)	00000000h
14h	4	Base Address Register High (BAR_HIGH)	00000000h
18h	4	Base Address Register1 (BAR1)	00000004h
1Ch	4	Base Address Register1 High (BAR1_HIGH)	00000000h
2Ch	4	Subsystem Vendor And Subsystem ID (SUBSYSTEMID)	00000000h
30h	4	Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)	00000000h
34h	4	Capabilities Pointer Register (CAPABILITYPTR)	00000080h
3Ch	4	Interrupt Register (INTERRUPTREG)	00000000h
80h	4	PowerManagement Capability ID (POWERCAPID)	00039001h
84h	4	Power Management Control And Status Register (PMECTRLSTATUS)	00000008h
90h	4	PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD)	F0140009h
94h	4	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG)	01400010h
98h	4	Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)	00002101h
9Ch	4	Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG)	000024C1h
A0h	4	D0i3 And Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG)	000F0800h
B0h	4	General Purpose Read Write Register1 (GEN_REGRW1)	00000000h
B4h	4	General Purpose Read Write Register2 (GEN_REGRW2)	00000000h
B8h	4	General Purpose Read Write Register3 (GEN_REGRW3)	00000000h
BCh	4	General Purpose Read Write Register4 (GEN_REGRW4)	00000000h
C0h	4	General Purpose Input Register (GEN_INPUT_REG)	00000000h
F8h	4	Manufacturers ID (MANID)	00000000h

9.1.1 Device ID And Vendor ID Register (DEVVENDID) - Offset 0h

Device ID and Vendor ID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + 0h	A0AA8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4B2Ah RO/P	**Device ID Field (DEVICEID):** Device ID identifies the particular PCI device
15:0	8086h RO	**Vendor ID Field (VENDORID):** Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device

9.1.2 Status And Command (STATUSCOMMAND) - Offset 4h

Command register and Status register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW/1C	**RMA Field (RMA):** Received Master Abort
28	0h RW/1C	**RTA Field (RTA):** Received Target Abort
27:21	0h RO	**Reserved**
20	1h RO	**Cap List Field (CAPLIST):** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**Interrupt Status Field (INTR_STATUS):** Interrupt Status: This bit reflects state of interrupt in the device
18:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** Interrupt Disable
9	0h RO	**Reserved**
8	0h RW	**SERR Enable Field (SERR_ENABLE):** SERR Enable Not implemented
7:3	0h RO	**Reserved**
2	0h RW	**BME Field (BME):** Bus Master Enable
1	0h RW	**MSE Field (MSE):** Memory Space Enable
0	0h RO	**Reserved**

9.1.3 Revision ID And Class Code (REVCLASSCODE) - Offset 8h

Revision ID register and Class Code register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + 8h	0C800000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0C8000h RO	**Revision ID Field (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	00h RO/P	**Class Code Field (RID):** Revision ID identifies the revision of particular PCI device.

9.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST) - Offset Ch

Cache Line Size as RW with def 0 Latency Timer RW with def 0 Header Type with Type 0 configuration header and Reserved BIST register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + Ch	00800000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	1h RO	**Multi-Function Device Field (MULFNDEV):** Multi-Function Device
22:16	00h RO	**Header Type Field (HEADERTYPE):** Header Type: Implements Type 0 Configuration header
15:8	00h RO	**Latency Timer Field (LATTIMER):** Latency Timer: This register is implemented as R/W with default as 0
7:0	00h RW/P	**Cache Line Size Field (CACHELINE_SIZE):** Cache Line Size

9.1.5 Base Address Register (BAR) - Offset 10h

Base Address Register Low [31:2] type[2:1] in 32bit or 64bit address range and memory space indicator [0].

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR):** Base Address Register Low Base address of the OCP fabric memory space. Taken from Strap values as ones
11:4	00h RO	**Size Field (SIZEINDICATOR):** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**Prefetchable Field (PREFETCHABLE):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE0):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range. If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** Memory Space Indicator: 0 indicates this BAR is present in the memory space.

9.1.6 Base Address Register High (BAR_HIGH) - Offset 14h

Base Address Register High enabled if [2:1] of BAR_HIGH is 10.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR_HIGH):** Base Address High - MSB

9.1.7 Base Address Register1 (BAR1) - Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K type in [2:1] and memory space indicator in [0].

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + 18h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR1):** Base Address1 This field is present if BAR1 is enabled through private configuration space.
11:4	00h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** Prefetchable: Indicates that this BAR is not pre-fetchable.
2:1	2h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

9.1.8 Base Address Register1 High (BAR1_HIGH) - Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1 register is 10.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR1_HIGH):** Base Address: Base address of the OCP fabric memory space. Taken from Strap values as ones

9.1.9 Subsystem Vendor And Subsystem ID (SUBSYSTEMID) - Offset 2Ch

SVID register along with SID register is to distinguish subsystem from another.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system.
15:0	0000h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

9.1.10 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h

Expansion ROM Base Address register is a RO indicates support for Expansion ROMs

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION ROM base address field (EXPANSION_ROM_BASE):** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

9.1.11 Capabilities Pointer Register (CAPABILITYPTR) - Offset 34h

Capabilities Pointer register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Capabilities Pointer: Indicates what the next capability is.

9.1.12 Interrupt Register (INTERRUPTREG) - Offset 3Ch

Interrupt line Register isn't used in Bridge directly Interrupt Pin register reflects the IPIN value in private configuration space. Min_GNT register indicating the requirements of latency timers and Max_LAT register max latency.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + 3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**Min GNT Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers // Re-Check Desc Padma

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11:8	0h RO	**Interrupt Pin Field (INTPIN):** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW/P	**Int Line Field (INTLINE):** Interrupt Line: It is used to communicate to software the interrupt line to which the interrupt pin is connected

9.1.13 Power Management Capability ID (POWERCAPID) - Offset 80h

Power Management Capability ID register points to Next Capability Structure and Power Management Capability with Power Management Capabilities register for PME Support and Version.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + 80h	00039001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved**
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h RO	**Next Cap Field (NXTCAP):** Next Capability: Points to the next capability structure.
7:0	01h RO	**Power Capability ID Field (POWER_CAP):** Power Management Capability: Indicates this is power management capability

9.1.14 Power Management Control and Status Register (PMECTRLSTATUS) - Offset 84h

Power Management Control and Status Register to set and read PME Status, PME Enable, No Soft Reset and Power State.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/P	**PME Status Field (PMESTATUS):** PME Status
14:9	0h RO	**Reserved**
8	0h RW/P	**PME Enable Field (PMEENABLE):** PME Enable
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset
2	0h RO	**Reserved**
1:0	0h RW	**Power State Field (POWERSTATE):** Power State: This field is used both to determine the current Power State and to set a new Power State

9.1.15 PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h

PCI Device Vendor Specific Capability register defines Vendor Specific Capability ID, Revision, Length, Next Capability and CAPID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + 90h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision ID Field (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	00h RO	**Next Capability Field (NEXT_CAP):** Next Capability
7:0	09h RO	**Capability ID Field (CAPID):** Capability ID

9.1.16 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h

Extended Vendor capability register for VSEC Length, Revision and ID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific ID Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor specific Extended Capability revision
15:0	0010h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

9.1.17 Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h

Software location pointer in MMIO space as an offset specified by BAR.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + 98h	00002101h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000210h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR BAR Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	1h RO	**SW LTR Valid Field (SW_LAT_VALID):** This value is reflected from the SW LTR valid strap at the top level

9.1.18 Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch

Device IDLE pointer register giving details on Device MMIO Offset Location, BAR NUM and D0i3 Valid Strap.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + 9Ch	000024C1h

Bit Range	Default & Access	Field Name (ID): Description
31:4	000024Ch RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** Bar Num: Indicates that the D0i3 MMIO location is always at BAR0
0	1h RO	**D0i3 Valid Field (VALID):** Valid: This value is reflected from the D0i3 valid strap at the top level.

9.1.19 D0i3 And Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h

D0idle_Max_Power_On_Latency register set at boot and power control enable register to enable communication with the PGCB block below the Bridge.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + A0h	000F0800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW/P	**HAE Field (HAE):** Hardware Autonomous Enable
20	0h RO	**Reserved**
19	1h RW/P	**Sleep Enable Field (SLEEP_EN):** Sleep Enable
18	1h RW/P	**D3 Hen Field (PGE):** DEVIDLE Enable (DEVIDLEN): If '1' then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set.
17	1h RW/P	**Device Idle En Field (I3E):** PMCRE: PMC Request Enable
16	1h RW/P	**PMC Request Enable Field (PMCRE):** D3-Hot Enable (D3HEN): If '1' then function will power gate when idle and the PMCSR[1:0] register in the function ='11' (D3).
15:13	0h RO	**Reserved**
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** Power On Latency Scale
9:0	000h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** Power On Latency value

9.1.20 General Purpose Read Write Register1 (GEN_REGRW1) - Offset B0h

General Purpose PCI Read Write Register1.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_REG_RW1):** General Purpose PCI Register: This register value is brought out as GEN_REG_RW1

9.1.21 General Purpose Read Write Register2 (GEN_REGRW2) - Offset B4h

General Purpose PCI Read Write Register2.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_REG_RW2):** General Purpose PCI Register: This register value is brought out as GEN_REG_RW2

9.1.22 General Purpose Read Write Register3 (GEN_REGRW3) - Offset B8h

General Purpose PCI Read Write Register3.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_REG_RW3):** General Purpose PCI Register: This register value is brought out as GEN_REG_RW3

9.1.23 General Purpose Read Write Register4 (GEN_REGRW4) - Offset BCh

General Purpose PCI Read Write Register4.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_REG_RW4):** General Purpose PCI Register: This register value is brought out as GEN_REG_RW4

9.1.24 General Purpose Input Register (GEN_INPUT_REG) - Offset C0h

General Purpose Input Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General Purpose Input Register: This register value reflects the value of GEN_REG_INPUT_RW

9.1.25 Manufacturers ID (MANID) - Offset F8h

Manufacturers ID register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:2] + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/P	**Manufacturers ID Field (MANID):** Manufacturer ID: Default value comes from straps.

9.2 GSPI Memory Mapped Registers Summary

Table 9-2. Summary of GSPI Memory Mapped Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	REG SSCR0 (SSCR0)	00000000h
4h	4	REG SSCR1 (SSCR1)	00000000h
8h	4	REG SSSR (SSSR)	00000004h
10h	4	REG SSDR (SSDR)	00000000h
28h	4	REG SSTO (SSTO)	00000000h
44h	4	REG SITF (SITF)	00000000h
48h	4	REG SIRF (SIRF)	00000000h
200h	4	REG CLOCKS (CLOCKS)	00000000h
204h	4	REG RESETS (RESETS)	00000000h
210h	4	REG ACTIVELTR_VALUE (ACTIVELTR_VALUE)	00000800h
214h	4	REG IDLELTR_VALUE (IDLELTR_VALUE)	00000800h
218h	4	REG TX_BIT_COUNT (TX_BIT_COUNT)	00000000h
21Ch	4	REG RX_BIT_COUNT (RX_BIT_COUNT)	00000000h
220h	4	REG SSP_REG (SSP_REG)	00000000h
224h	4	REG SPI_CS_CONTROL (SPI_CS_CONTROL)	0000F000h
228h	4	REG SW_SCRATCH_0 (SW_SCRATCH_0)	00000000h
22Ch	4	REG SW_SCRATCH_1 (SW_SCRATCH_1)	00000000h
230h	4	REG SW_SCRATCH_2 (SW_SCRATCH_2)	00000000h
234h	4	REG SW_SCRATCH_3 (SW_SCRATCH_3)	00000000h
238h	4	REG CLOCK_GATE (CLOCK_GATE)	00000000h
240h	4	REG REMAP_ADDR_LO (REMAP_ADDR_LO)	00000000h
244h	4	REG REMAP_ADDR_HI (REMAP_ADDR_HI)	00000000h
24Ch	4	REG DEVIDLE_CONTROL (DEVIDLE_CONTROL)	00000008h
250h	4	REG DEL_RX_CLK (DEL_RX_CLK)	00000000h
280h	4	REG SPI_HVM_MISR_CRCOUT (SPI_HVM_MISR_CRCOUT)	0000FFFFh
2FCh	4	REG CAPABLITIES (CAPABLITIES)	00000620h
800h	4	REG SAR_LO0 (SAR_LO0)	00000000h
804h	4	REG SAR_HI0 (SAR_HI0)	00000000h
808h	4	REG DAR_LO0 (DAR_LO0)	00000000h
80Ch	4	REG DAR_HI0 (DAR_HI0)	00000000h
810h	4	REG LLP_LO0 (LLP_LO0)	00000000h
814h	4	REG LLP_HI0 (LLP_HI0)	00000000h
818h	4	REG CTL_LO0 (CTL_LO0)	00000000h
81Ch	4	REG CTL_HI0 (CTL_HI0)	00000000h
820h	4	REG SSTAT0 (SSTAT0)	00000000h
828h	4	REG DSTAT0 (DSTAT0)	00000000h
830h	4	REG SSTATAR_LO0 (SSTATAR_LO0)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
834h	4	REG SSTATAR_HI0 (SSTATAR_HI0)	00000000h
838h	4	REG DSTATAR_LO0 (DSTATAR_LO0)	00000000h
83Ch	4	REG DSTATAR_HI0 (DSTATAR_HI0)	00000000h
840h	4	REG CFG_LO0 (CFG_LO0)	00000203h
844h	4	REG CFG_HI0 (CFG_HI0)	00000000h
848h	4	REG SGR0 (SGR0)	00000000h
850h	4	REG DSR0 (DSR0)	00000000h
858h	4	REG SAR_LO1 (SAR_LO1)	00000000h
AC0h	4	REG RawTfr (RAWTFR)	00000000h
AC8h	4	REG RawBlock (RAWBLOCK)	00000000h
AD0h	4	REG RawSrcTran (RAWSRCTRAN)	00000000h
AD8h	4	REG RawDstTran (RAWDSTTRAN)	00000000h
AE0h	4	REG RawErr (RAWERR)	00000000h
AE8h	4	REG StatusTfr (STATUSTFR)	00000000h
AF0h	4	REG StatusBlock (STATUSBLOCK)	00000000h
AF8h	4	REG StatusSrcTran (STATUSSRCTRAN)	00000000h
B00h	4	REG StatusDstTran (STATUSDSTTRAN)	00000000h
B08h	4	REG StatusErr (STATUSERR)	00000000h
B10h	4	REG MaskTfr (MASKTFR)	00000000h
B18h	4	REG MaskBlock (MASKBLOCK)	00000000h
B20h	4	REG MaskSrcTran (MASKSRCTRAN)	00000000h
B28h	4	REG MaskDstTran (MASKDSTTRAN)	00000000h
B30h	4	REG MaskErr (MASKERR)	00000000h
B38h	4	REG ClearTfr (CLEARTFR)	00000000h
B40h	4	REG ClearBlock (CLEARBLOCK)	00000000h
B48h	4	REG ClearSrcTran (CLEARSRCTRAN)	00000000h
B50h	4	REG ClearDstTran (CLEARDSTTRAN)	00000000h
B58h	4	REG ClearErr (CLEARERR)	00000000h
B60h	4	REG StatusInt (STATUSINT)	00000000h
B98h	4	REG DmaCfgReg (DMACFGREG)	00000000h
BA0h	4	REG ChEnReg (CHENREG)	00000000h

9.2.1 REG SSCR0 (SSCR0) - Offset 0h

The Enhanced SSP Control 0 registers contain twelve different bit fields that control various functions within the Enhanced SSP. All bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**MOD:** Set to 0 - Normal SSP Mode: Full Duplex Serial peripheral interface. 1 = reserved
30	0h RW	**ACS:** Set to 0 for Clock selection which is determined by the NCS and ECS bits in this register. 1 = reserved
29	0h RO	**Reserved**
28:24	0h RO	**Reserved**
23	0h RW	**TIM:** Transmit FIFO Under Run Interrupt Mask When set, this bit will mask the Transmit FIFO Under Run (TUR) event from generating an SSP interrupt. The SSSR status register will still indicate that an TUR event has occurred. This bit can be written to at any time (before or after SSP is enabled). 0 = Transmit FIFO Under Run(TUR) events will generate an SSP interrupt 1 = TUR events will be masked
22	0h RW	**RIM:** Receive FIFO Over Run Interrupt Mask When set, this bit will mask the Receive FIFO Over Run (ROR) event from generating an SSP interrupt. The SSSR status register will still indicate that an ROR event has occurred. This bit can be written to at any time (before or after SSP is enabled) 0 = Receive FIFO Over Run (ROR) events will generate an SSP interrupt 1 = ROR events will be masked
21	0h RW	**NCS:** Network Clock Select The SSCR0.NCS bit in conjunction with SSCR0.ECS determines which clock is used. 0 = Clock selection is determined by ECS bit 1 = Reserved
20	0h RW	**EDSS:** Extended Data Size Select The 1-bit extended field is used in conjunction with the data size select SSCR0.DSS bits to select the size of the data transmitted and received by the Enhanced SSP. 0 =A zero is prepended to the DSS value which sets the DSS range from 4 -16 bits 1 =A one is pre-appended to the DSS value which sets the DSS range from 17-32 bits
19:8	000h RW	**SCR:** Serial Clock Rate Value used to generate transmission rate of SSP. Note: The SPI Interface Controller (SSP) baud rate (or Serial bit-rate clock SPI_CLK_OUT) can be generated either by the M/N divider or internally to the SSP (SSCR0.SCR) by dividing the on-chip SSP_CLK (output of M/N) to generate baud rates up to: MCC: 25 Megabits per second

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**SSE:** Synchronous Serial Port Enable The SSP enable bit, SSCR0.SSE, enables and disables all SSP operations. WhenSSCR0.SSE=0, the Enhanced SSP is disabled; when SSCR0.SSE=1, it is enabled. When the Enhanced SSP is disabled, all of its clocks can be stopped by programmers to minimize power consumption. On reset, the Enhanced SSP is disabled. When the SSCR0.SSE bit is cleared during active operation, the Enhanced SSP is disabled immediately, terminating the current frame being transmitted or received.Clearing SSCR0.SSE resets the Enhanced SSP FIFOs and the Enhanced SSP status bits; however, the Enhanced SSP Control registers are not reset. Note: After reset or after clearing the SSCR0.SSE, users must ensure that the SSCR1, SSITR and SSTO control registers are properly re-configured and that the SSSR register is reset before re- enabling the Enhanced SSP with the SSCR0.SSE. Also, the SSCR0.SSE bit must be cleared before reconfiguring the SSCR0, SSCR1, registers; other control bits in SSCR0 can be written at the same time as the SSCR0.SSE. When any SSP is disabled, its five pins can be used as GPIOs. 0 = SSP operation disabled 1 = SSP operation enabled

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**ECS:** External Clock Select: 0 = use On-chip clock (output of M/N Divider) to produce the SSP's serial clock(SSPSCLK). Selects the use of the output of the M/N Divider (MBAR0 + 0x800, CLOCK_PARAMS) to create the SSP's serial clock (SSPCLK) Note: Setting M=N=1 will provide a pass through of the M/N Divider of the serial clock. See SCR for Serial Clock Rate generation. Note: The input (SSPEXTCLK) is treated as SSPSCLKEN, a clock enable used to gate the SSPSCLK output. When the external signal SSPSCLKEN changes, there will be a 1 -2 clock lag before the SSPSCLK is started or stopped due to the internal synchronization of this signal. 1 = Reserved
5:4	0h RW	**FRF:** Frame Format: Set to 00 - Motorola Serial Peripheral Interface (SPI) MCC: Only Motorola interface supported 01 = reserved 10 = reserved 11 = reserved
3:0	0h RW	**DSS:** Data Size Select With EDSS as MSB. The CPU or DMA access data through the Enhanced SSP Ports Transmit and Receive FIFOs. A CPU access takes the form of programmed I/O, transferring one FIFO entry per access. CPU accesses would normally be triggered off of an SSSR Interrupt and must always be 32 bits wide. CPU Writes to the FIFOs are 32 bits wide, but the serializing logic will ignore all bits beyond the programmed FIFO data size (EDSS/DSS value). CPU Reads to the FIFOs are also 32 bits wide, but the Receive data written into the RX FIFO (from the RXD line) is stored with zeroes in the MSBs down to the programmed data size. The FIFOs can also be accessed by DMA Single transactions, which must be 1, 2 or 4 bytes, depending upon the EDSS value, and must also transfer one FIFO entry per access. When the SSCR0.EDSS bit is set, DMA Single transactions must be 4 bytes (the DMA must have the Enhanced SSP configured as a 32-bit peripheral).The DMAs_TR.width register must be at least the SSP data size programmed into the SSP control registers EDSS and DSS. The FIFO is seen as one 32-bit location by the processor. For Writes, the Enhanced SSP port takes the data from the Transmit FIFO, serializes it, and sends it over the serial wire (SSPTXD) to the external peripheral. Receive data from the external peripheral (on SSPRXD) is converted to parallel words and stored in the Receive FIFO. A programmable FIFO trigger threshold, when exceeded, generates an Interrupt or DMA service request that, if enabled, signals the CPU or DMA respectively to empty the Receive FIFO or to refill the Transmit FIFO. The Transmit and Receive FIFOs are differentiated by whether the access is a Read or a Write transfer. Reads automatically target the Receive FIFO, while Writes will write data to the Transmit FIFO. From a memory-map perspective, they are at the same address. FIFOs are 64 samples deep by 32 bits wide. Each read or write is to 1 SSP sample. The 4-bit Data Size Select SSCR0.DSS field is used in conjunction with the extended data size select SSCR0.EDSS bit to select the size of the data transmitted and received by the Enhanced SSP. The concatenated 5-bit value of SSCR0.EDSS and SSCR0.DSS provides a data range from 4 to 32 bits in length. Note: When data is programmed to be less than 32 bits, the FIFO should be programmed right-justified. Although it is possible to program data sizes of 1, 2, and 3 bits, these sizes are reserved and produce unpredictable results in the Enhanced SSP. 0011 4 bits 0111 8 bits 1111 16, 32 bits (Note: To differentiate between 16 bits and 32 bits check the EDSS bit, for 32 bit data EDSS = 1)

9.2.2 REG SSCR1 (SSCR1) - Offset 4h

The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits should be zeroes, and Read value of these bits are undetermined.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:24	00h NA	**RES_29_24:** Reserved
23	0h RW	**RWOT:** Receive With Out Transmit The SSCR1.RWOT bit is a read-write bit used to put the Enhanced SSP into a mode similar to half duplex. When the Enhanced SSP is in Transmit/Receive mode as determined SSCR1.RWOT=0, the Enhanced SSP simultaneously transmits and receives data (as supported by the individual protocols, i.e., normally all modes are full duplex except microwire) and the serial clock SSPSCLK only toggles while an active data transfer is underway. When in Receive-without-Transmit mode as determined by SSCR1.RWOT=1, the Enhanced SSP will continue to clock in receive data despite data existing or not in the Transmit FIFO. Data is sent/ received according to the selected format immediately after the Enhanced SSP enable bit (SSCR0.SSE) is set. This allows the Enhanced SSP to receive data without transmitting data (half-duplex only). During this mode, if there is no data to send, programmers should disable the DMA service requests and Interrupts for the Transmit FIFO (clear the SSCR1.TSRE and SSCR1.TIE bits). If the Transmit FIFO is empty, the SSPTXD line will be driven to 0. The Transmit FIFO underrun condition will not occur when SSCR1.RWOT=1. When RWOT is enabled, the SSSR.BUSY bit will remain active (set to 1) until software clears the RWOT bit. If the Enhanced SSP has been in RWOT mode, and software disables this by clearing the RWOT bit, an extra frame cycle may occur due to the synchronization between clock domains. This bit must not be used when the SSCR0.MOD bit is set. 0 = Transmit/Receive mode 1 = Receive without transmit mode Warning: When RWOT =1, the first entry of the TX FIFO must be initialized with all zeros. Note: RWOT is not used in Windows drivers at all. When you enable RWOT you have no control on the data flow (the clock is free-running). Even if there have half-duplex operation support from windows, it need to control how many data that need to read without transmit. Use full-duplex operation to do that putting dummy data into the TX FIFO. Registers SIRFL, TX_BIT_COUNT and RX_BIT_COUNT cannot be referred when using RWOT mode.
22	0h RW	**TRAIL:** 0 = Processor based, trailing bytes are handled by processor 1 = DMA based, trailing bytes are handled by DMA

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**TSRE:** Transmit FIFO Service Request Enable The SSCR1.TSRE bit enables the Transmit FIFO DMA Service Request. When SSCR1.TSRE=0, the DMA Service Request is masked, and the state of the transmit FIFO service request (SSSR.TFS) bit within the Enhanced SSP Status register is ignored. When SSCR1.TSRE=1, the DMA Service Request is enabled, and whenever SSSR.TFS is set to one, a DMA Service Request is made to the DMA. Note that programming SSCR1.TSRE=0 does not affect the current state of SSSR.TFS or the ability of the Transmit FIFO logic to set and clear SSSR.TFS it only blocks the generation of the DMA Service Request. Also, the state of SSCR1.TSRE does not affect the generation of the Interrupt, which is asserted whenever the SSSR.TFS is set to 1.
20	0h RW	**RSRE:** Receive FIFO Service Request Enable The SSCR1.RSRE bit enables the Receive FIFO DMA Service Request. WhenSSCR1.RSRE=0, the DMA Service Request is masked, and the state of the receive FIFO service request SSSR.RFS bit within the Enhanced SSP Status register is ignored. When SSCR1.RSRE=1, the DMA Service Request is enabled, and whenever SSSR.RFS is set to one, a DMA Service Request is made to the DMA. Note that programming SSCR1.RSRE=0 does not affect the current state of SSSR.RFS or the ability of the Receive FIFO logic to set and clear SSSR.RFS it only blocks the generation of the DMA Service Request. Also, the state of SSCR1.RFRS does not affect the generation of the Interrupt, which is asserted whenever the SSSR.RFS is set to 1. 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
19	0h RW	**TINTE:** Receive FIFO Time-out Interrupt Enable The SSCR1.TINTE is a read-write bit used to mask or enable the Receiver Time-out Interrupt. When SSCR1.TINTE=0, the Interrupt is masked and the state of the SSSR.TINT bit is ignored by the Interrupt controller. When SSCR1.TINTE=1, the Interrupt is enabled, and whenever the SSSR.TINT bit is set to one an Interrupt request is made to the Interrupt controller. Note that programming SSCR1.TINTE=0 does not affect the current state of the SSSR.TINT or the ability of logic to set and clear the SSSR.TINT; it only blocks the generation of the Interrupt request. 0 = Receiver Time-out interrupts are disabled 1 = Receiver Time-out interrupts are enabled
18	0h RW	**PINTE:** Peripheral Trailing Byte Interrupts Enable This feature is not recommended for use in the LPSS implementation. 0 = Peripheral Trailing Byte Interrupts are disabled 1 = Peripheral Trailing Byte Interrupts are enabled.
17	0h RO	**Reserved**
16	0h RW	**IFS:** Invert Frame Signal 0 - Frame signal (Chip Select) is active low 1 - Frame signal (Chip Select) is active high
15	0h RW	**STRF:** Select FIFO for Enable FIFO Write/Read (STRF) This is a test mode bit that selects whether the Transmit or Receive FIFO is enabled for Writes and Reads whenever the SSCR1. EFWR is programmed to 1, which puts the Enhanced SSP in a Test mode. 0 = Transmit FIFO is selected for both writes and reads through the SSP Data Register (SSDR) 1 = Receive FIFO is selected for both writes and reads through the SSP Data Register (SSDR)

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**EFWR:** Enable FIFO Write/Read (test mode bit) This bit enables a Test mode for the Enhanced SSP. When SSCR1.EFWR = 0, the Enhanced SSP operates in the Normal mode. WhenSSCR1.EFWR = 1, the Enhanced SSP enters a mode that whenever the CPU reads or writes to the Enhanced SSP Data register, it actually reads and writes directly to either the Transmit FIFO or the Receive FIFO, depending on the programmed state of the select FIFO for enable FIFO write/read (SSCR1.STRF) bit. With SSCR1.STRF = 0, all Writes to the SSDR are performed on the Transmit FIFO, and Reads to the SSDR will read back the data written to the Transmit FIFO in first-in-first-out order. WithSSCR1.STRF = 1, all Writes to the SSDR are performed on the Receive FIFO, and Reads to the SSDR will read back the data written to the Receive FIFO in first-in-first out order. In EFWR Test mode, data will not be transmitted on the SSPTXD pin, data input on the SSPRXD pin will not be stored, and the busy and ROR bits will not work. The Interrupt Test Register, however, will still be functional. Using software, this mode can test whether or not the Transmit FIFO or the Receive FIFO operates properly as a FIFO memory stack. Software should verify that the SSSR.CSS bit has gone from a 1 to a 0 before reading the TX FIFO. 0 = FIFO write/read special function is disabled (normal SSP operational mode) 1 = FIFO write/read special function is enabled.
13:5	000h RO	**Reserved**
4	0h RW	**SPH:** Motorola SPI SSPSCLK phase setting The SSCR1.SPH bit determines the phase relationship between the SSPSCLK and the serial frame (SSPSFRM) pins when the Motorola* SPI format is selected (SSCR0.FRF=00). WhenSSCR1.SPH=0, SSPSCLK remains in its Inactive/Idle state (as determined by theSSCR1.SPO setting) for one full cycle after SSPSFRM is asserted low at the beginning of a frame. SSPSCLK continues to transition for the rest of the frame and is then held in its Inactive state for one-half of an SSPSCLK period before SSPSFRM is de-asserted high at the end of the frame. When SSCR1.SPH=1, SSPSCLK remains in its Inactive/Idle state (as determined by the SSCR1.SPO setting) for one-half cycle after SSPSFRM is asserted low at the beginning of a frame. SSPSCLK continues to transition for the remainder of the frame, and is then held in its Inactive state for one full SSPSCLK period before SSPSFRM is de-asserted high at the end of the frame. The combination of the SSCR1.SPO and SSCR1.SPH settings determines when SSPSCLK is active during the assertion of SSPSFRM, and which SSPSCLK edge transmits and receives data on the SSPTXD and SSPRXD pins. When SSCR1.SPO and SSCR1.SPH are programmed to the same value (both 0 or both1) Transmit data is driven on the falling edge of SSPSCLK, and Receive data is latched on the rising edge of SSPSCLK. When SSCR1.SPO and SSCR1.SPH are programmed to opposite values (one 0 and the other 1), Transmit data is driven on the rising edge of SSPSCLK, and Receive data is latched on the falling edge of SSPSCLK. 0 - SSPSCLK is inactive one cycle at the start of a frame and cycle at the end of a frame 1 - SSPSCLK is inactive for one half cycle at the start of a frame and one cycle at the end of a frame

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**SPO:** Motorola SPI SSPSCLK polarity setting The SSCR1.SPO bit selects the polarity of the inactive state of the SSPSCLK pin when the Motorola* SPI format is selected (SSCR0.FRF=00). For S SCR1.SPO=0, the SSPSCLK is held low in the Inactive or Idle state when the Enhanced SSP is not transmitting/receiving data. For SSCR1.SPO=1, the SSPSCLK is held high during the Inactive/Idle state. The programmed setting of the SSCR1.SPOalone does not determine which SSPSCLK edge transmits or receives data theSSCR1.SPO setting in combination with the SSPSCLK phase bit SSCR1.SPH does. 0 - The inactive or idle state of SSPSCLK is low 1 - The inactive or idle state of SSPSCLK is high
2	0h RW	**LBM:** Loop-Back Mode (test mode bit) The SSCR1.LBM bit is a test mode bit that enables and disables the ability of the Enhanced SSP Transmit and Receive logic to communicate. When SSCR1.LBM=0, the Enhanced SSP operates normally. The Transmit and Receive data paths are independent and communicate via their respective pins. When SSCR1.LBM=1, the output of the Transmit serial shifter is connected directly to the input of the Receive serial shifter internally. During Loop-Back mode, the Transmit pin (SSPTXD) continues to function as normal. 0 = Normal serial port operation enabled 1 = Output of transmit serial shifter connected to input of receive serial shifter, internally
1	0h RW	**TIE:** Transmit FIFO Interrupt Enable The SSCR1.TIE bit enables the Transmit FIFO Service Request Interrupt. WhenSSCR1.TIE=0, the Interrupt is masked, and the state of the transmit FIFO service request (SSSR.TFS) bit within the Enhanced SSP Status register is ignored. When SSCR1.TIE=1, the Interrupt is enabled, and whenever SSSR.TFS is set to one, an Interrupt request is made to the Interrupt controller. Note that programming SSCR1.TIE=0 does not affect the current state of SSSR.TFS or the ability of the Transmit FIFO logic to set and clearSSSR.TFS it only blocks the generation of the Interrupt request. Also, the state ofSSCR1.TIE does not affect the generation of the Transmit FIFO DMA service request, which is asserted whenever the SSSR.TFS is set to 1. 0 - Transmit FIFO level interrupt is disabled 1 - Transmit FIFO level interrupt is enabled
0	0h RW	**RIE:** Receive FIFO Interrupt Enable The SSCR1.RIE bit enables the Receive FIFO Service Request Interrupt. WhenSSCR1.RIE=0, the Interrupt is masked, and the state of the receive FIFO service request SSSR.RFS bit within the Enhanced SSP Status register is ignored. When SSCR1.RIE=1, the Interrupt is enabled, and whenever SSSR.RFS is set to one, an Interrupt request is made to the Interrupt controller. Note that programming SSCR1.RIE=0 does not affect the current state ofSSSR.RFS or the ability of the Receive FIFO logic to set and clear SSSR.RFS it only blocks the generation of the Interrupt request. Also, the state of SSCR1.RIE does not affect the generation of the Receive FIFO DMA service request, which is asserted whenever the SSSR.RFS bit is set to 1. 0 - Receive FIFO level interrupt is disabled 1 - Receive FIFO level interrupt is enabled

9.2.3 REG SSSR (SSSR) - Offset 8h

The Enhanced SSP Status registers contain bits that signal overrun errors as well as the Transmit and Receive FIFO service requests. Each of these hardware-detected events signals an Interrupt request to the Interrupt controller. The Status register also contains flags that indicate when the Enhanced SSP is actively transmitting data, when the Transmit FIFO is not full, and when the Receive FIFO is not empty. One Interrupt signal is sent to the Interrupt Controller for each SSP. These events can cause an

Interrupt: End-of-Chain, Receiver Time-out, Peripheral Trailing Byte, Receive FIFO overrun, Receive FIFO request, and Transmit FIFO request

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW/1C	**TUR:** Transmit FIFO Under Run The SSSR.TUR bit is a read-write, one-to-clear status bit that indicates that the transmitter tried to send data from the Transmit FIFO when the Transmit FIFO was empty. When the SSSR.TUR bit is set, an Interrupt is generated to the CPU that can be locally masked by the SSCR0.TIM bit. The setting of the SSSR.TUR bit does not, however, generate any DMA service request. The SSSR.TUR bit remains set until cleared by software writing a 1 to this bit which will also reset its Interrupt request; writing a 0 to this bit does not affect SSSR.TUR status. This bit can only be set when the Enhanced SSP is a slave to the FRAME signal (SSCR1.SFRMDIR = 1), or if the Enhanced SSP is a master to the FRAME signal and the Enhanced SSP is in Network mode, and will not be set if the Enhanced SSP is in Receive-Without- Transmit mode(SSCR1.RWOT =1). 0 = Transmit FIFO has not experienced an under run 1 = Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	0h RO	**Reserved**
19	0h RW/1C	**TINT:** Receiver Time-out Interrupt The SSSR.TINT bit is a read-write bit that is set to 1 when the Receive FIFO has been idle (no samples received) for a period of time defined by the value programmed within the Time-Out register (SSTO). This interrupt can be masked by the SSCR1.TINTE bit. The SSSR.TINT bit is cleared by programmers by writing a 1 to it. 0 = No receiver time-out pending 1 = Receive FIFO has been idle for period defined by SSTO
18	0h RW/1C	**PINT:** Peripheral Trailing Byte Interrupt This feature is not recommended for use in the LPSS implementation. 0 = No peripheral trailing byte interrupt pending 1 = Peripheral trailing byte interrupt pending
17:8	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/1C	**ROR:** Receive FIFO Overrun The receiver overrun status bit SSSR.ROR is a read-write bit that is set when the Receive logic attempts to place data into the Receive FIFO after it has been completely filled. If the Receive FIFO is full and new data is received, the SSSR.ROR bit is set, and the newly received data is discarded. This process is repeated for each new data-chunk received until at least one empty FIFO entry exists. When the SSSR.ROR bit is set, an Interrupt is generated to the CPU that can be locally masked by theSSCR0.RIM bit. The setting of the SSSR.ROR bit does not, however, generate any DMA service request. The SSSR.ROR bit remains set until cleared by software writing a 1 to this bit which will also reset its Interrupt request; writing a 0 to this bit does not affect SSSR.ROR status. 0 = Receive FIFO has not experienced an overrun 1 = Attempted data write to full receive FIFO, request interrupt
6	0h RO	**RFS:** Receive FIFO Service Request The receive FIFO service request flag SSSR.RFS is a read-only bit that is set to generate an Interrupt when the Receive FIFO requires service to prevent an overrun.SSSR.RFS is set any time the Receive FIFO has more entries of valid data than the number indicated by the Receive FIFO Trigger threshold, and it is cleared when it has the same or fewer entries than the threshold value. When the SSSR.RFS bit is set, an Interrupt is generated unless the receive FIFO interrupt request enable (SSCR1.RIE) bit is cleared. Also, the setting of the SSSR.RFS bit will signal a DMA service request if the SSCR1.RSRE bit is set. After the CPU or DMA reads the FIFO such that it has the same or fewer entries than the SIRF.WMRF value, the SSSR.RFS flag (and the service request and/or Interrupt) is automatically cleared. Software should not set both the SSCR1.RSRE and the SSCR1.RIE bits. 0 = Receive FIFO level is at or below the water mark for the SPI receive FIFO (WMRF) or SSP disabled 1 = Receive FIFO level exceeds the water mark for the SPI receive FIFO (WMRF), request interrupt
5	0h RO	**TFS:** Transmit FIFO Service Request The transmit FIFO service request flag SSSR.TFS is a read-only bit that is set to generate an Interrupt when the Transmit FIFO requires service to prevent an underrun.SSSR.TFS is set any time the Transmit FIFO has the same or fewer entries of valid data than indicated by the Transmit FIFO Trigger threshold, and it is cleared when it has more entries of valid data than the threshold value (the service request is triggered when the number of FIFO entries is less than or equal to 1 + LWMTF). When the SSSR.TFSbit is set, an Interrupt is generated unless the transmit FIFO interrupt request enables(SSCR1.TIE) bit is cleared. Also, the setting of the SSSR.TFS bit will generate a DMA service request if the SSCR.TSRE bit was set. After the CPU or the DMA fills the FIFO such that it exceeds the threshold, the SSSR.TFS flag (and the service request and/or Interrupt) is automatically cleared. If the threshold has not been exceeded, another request will be made. Software should not set both the SSCR1.TSRE and theSSCR1.TIE bits. 0 = Transmit FIFO level exceeds the Low Water Mark Transmit FIFO (SITF.LWMTF), or SSP disabled 1 = Transmit FIFO level is at or below the Low Water Mark Transmit FIFO (SITF.LWMTF), request interrupt
4	0h RO	**BSY:** The Enhanced SSP busy SSSR.BSY flag is a read-only bit that is set when the SSP is actively transmitting and/or receiving data, and is cleared when the SSP is idle or disabled (SSCR0.SSE=0). This bit does not generate an Interrupt. 0 = SSP is idle or disabled 1 = SSP currently transmitting or receiving a frame

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**RNE:** Receive FIFO Not Empty The receive FIFO not empty flag SSSR.RNE is a read-only bit that is set whenever the Receive FIFO contains one or more entries of valid data, and is cleared when it no longer contains any valid data. This bit can be polled when using programmed I/O to remove remaining bytes of data from the Receive FIFO since CPU Interrupt requests are made only when the Receive FIFO Trigger threshold has been met or exceeded. This bit does not generate an Interrupt. 0 = Receive FIFO is empty 1 = Receive FIFO is not empty
2	1h RO	**TNF:** Transmit FIFO Not Full The receive FIFO not empty flag SSSR.RNE is a read-only bit that is set whenever the Receive FIFO contains one or more entries of valid data, and is cleared when it no longer contains any valid data. This bit can be polled when using programmed I/O to remove remaining bytes of data from the Receive FIFO since CPU Interrupt requests are made only when the Receive FIFO Trigger threshold has been met or exceeded. This bit does not generate an Interrupt. 0 = Transmit FIFO is full 1 = Transmit FIFO is not full
1:0	0h RO	**Reserved**

9.2.4 REG SSDR (SSDR) - Offset 10h

The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access. The SSDR represents two physical registers: the first is temporary storage for data on its way out through the Transmit FIFO, the other is temporary storage for data coming in through the Receive FIFO. As the system accesses the register, FIFO Control logic transfers data automatically between register and FIFO as fast as the system moves it. Data in the FIFO shifts up or down to accommodate the new word (unless it's an attempted Write to a full Transmit FIFO). Status bits (such as SSSR.RNE, and SSSR.TNF) show users whether the FIFO is full, above/below a programmable FIFO trigger threshold, or empty. For Transmit data transfers (Write from system to SSP peripheral), the register can be loaded (written) by the system processor anytime it falls below its threshold level when using programmed I/O. When a data size of less than 32-bits is selected, users should not left-justify data written to the Transmit FIFO. Transmit logic left-justifies the data and ignores any unused bits. Received data of less than 32 -bits is automatically right-justified in the Receive FIFO.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DATA:** Data word to be written to/read from transmit/receive FIFO

9.2.5 REG SSTO (SSTO) - Offset 28h

The Enhanced SSP Time-Out registers have single bit fields that specify the time-out value used to signal a period of inactivity within the Receive FIFO. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 28h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RW	**TIMEOUT:** Timeout Value Is the value that defines the timeout interval for the RcV FIFO. The Interval is given by TIMEOUT/Parallel (Bus) Clock Frequency. When the number of samples in the Receive FIFO is less than RcV FIFO trigger threshold level, and no additional data is received, the Timeout timer will decrement. The time-out timer is reset after a new sample is received. In DMA Mode of operation this value needs to be set when the RcV FIFO Trigger Threshold is greater than 1 RcV FIFO Entry (the required Msize (Single Burst) for SSP DMA peripheral transfers); When in PIO mode of operation this value needs to be set when the total transfer size is not an even division of the RcV FIFO trigger threshold level. Is such a case the TIMEOUT value is calculated to be greater than the time to transfer the FIFO Entry size at the desired Bit Rate. Example Calculation: Timeout is greater than (RcV FIFO Entry Size) x (1/Serial Bit Rate)/ (1/Bus CLK) = Guard Band x (RcV FIFO Entry Size) x (1/Serial Bit Rate)/ (1/Bus CLK) Example: RcV FIFO Entry = 32 Bits Serial Bit Rate = 1 Mbs Bus CLK = 120 MHz Guard Band = 2x TIMEOUT = (32 (1x10-6))/(8.33 x10-9) = 3840 x 2 = 7680.

9.2.6 REG SITF (SITF) - Offset 44h

The SPI Transmit FIFO register is for writing the water mark for the SPI transmit FIFO and also for reading the number of entries in the SPI transmit FIFO

Type	Size	Offset	Default
MMIO	32 bit	BAR + 44h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:16	00h RO	**SITFL:** SPI Transmit FIFO Level Number of entries in SPI Transmit FIFO.
15:14	0h RO	**Reserved**
13:8	00h RW	**LWMTF:** Low Water Mark Transmit FIFO. Set the low water mark of the SPI transmit FIFO.
7:6	0h RO	**Reserved**
5:0	00h RW	**HWMTF:** High Water Mark Transmit FIFO. Set the high water mark of the SPI transmit FIFO.

9.2.7 REG SIRF (SIRF) - Offset 48h

The SPI Receive FIFO register is for writing the water mark for the SPI receive FIFO and also for reading the number of entries in the SPI receive FIFO

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:8	00h RO	**SIRFL:** SPI Receive FIFO Level Number of entries in SPI Receive FIFO.
7:6	0h RO	**Reserved**
5:0	00h RW	**WMRF:** Water Mark Receive FIFO. Set the water mark of the SPI receive FIFO.

9.2.8 REG CLOCKS (CLOCKS) - Offset 200h

Private Clock Configuration

Type	Size	Offset	Default
MMIO	32 bit	BAR + 200h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**CLK_UPDATE:** 0 No clock update 1 Clock gets updated
30:16	0000h RW	**N_VAL:** This is the denominator value (N) for the M over N divider logic that creates the SPI_CLK_OUT for the SSP. Used to generate the input CLK to SSP.
15:1	0000h RW	**M_VAL:** The numerator value (M) for the M over N divider logic that creates the SPI_CLK_OUT for the SSP. Used to generate the input CLK to SSP.
0	0h RW	**CLK_EN:** IP Functional (SPI Serial Clock) Clock Enable 0 - Clock Disabled 1 - Clock Enabled

9.2.9 REG RESETS (RESETS) - Offset 204h

Software Reset

Type	Size	Offset	Default
MMIO	32 bit	BAR + 204h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW	**RESET_DMA:** 0 = IP is in reset (Reset Asserted) 1 = IP is NOT at reset (Reset Released)
1:0	0h RW	**RESET_IP:** SSP Host Controller reset. Used to reset the SSP Host Controller by SW control. All SSP Configuration State and Operational State will be forced to the Default state. There is no timing requirement (SW can assert and de-assert in back to back transactions) This reset does NOT impact the LPSS cluster level settings by BIOS, the MMIO configuration header information, DMA channel configuration and interrupt assignment/mapping/etc. Driver should re-initialize registers related to Driver context following an SSP host controller reset. 00 = SSP Host Controller is in reset (Reset Asserted) 01 = Reserved 10 = Reserved 11 = SSP Host Controller is NOT at reset (Reset Released)

9.2.10 REG ACTIVELTR_VALUE (ACTIVELTR_VALUE) - Offset 210h

ActiveLTR_Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 210h	00000800h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**SNOOP_REQUIRMENT:** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	**Reserved**
12:10	2h RW	**SNOOP_LATENCY_SCALE:** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which do not match those values will be dropped completely, next read will return previous value.
9:0	000h RW	**SNOOP_VALUE:** 10-bit latency value

9.2.11 REG IDLELTR_VALUE (IDLELTR_VALUE) - Offset 214h

IdleLTR_Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 214h	00000800h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**SNOOP_REQUIRMENT:** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10 -bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RO	**Reserved**
12:10	2h RW	**SNOOP_LATENCY_SCALE:** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which do not match those values will be dropped completely, next read will return previous value.
9:0	000h RW	**SNOOP_VALUE:** 10-bit latency value

9.2.12 REG TX_BIT_COUNT (TX_BIT_COUNT) - Offset 218h

TX_BIT_COUNT_Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 218h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**TX_COUNT_OVERFLOW:** 0= count valid 1= count overflow/invalid
30:24	0h RO	**Reserved**
23:0	000000h RO	**TX_BIT_COUNT:** 24-bit up-counter which counts the number of TX bits on the Serial bus. The counter is forced to be cleared by software Read

9.2.13 REG RX_BIT_COUNT (RX_BIT_COUNT) - Offset 21Ch

RX_BIT_COUNT_Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 21Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**RX_COUNT_OVERFLOW:** 0= count valid 1= count overflow/invalid
30:24	0h RO	**Reserved**
23:0	000000h RO	**RX_BIT_COUNT:** 24-bit up-counter which counts the number of RX Bits on the Serial bus. The counter is forced to be cleared by software Read

9.2.14 REG SSP_REG (SSP_REG) - Offset 220h

SSP_Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 220h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**DISABLE_SSP_DMA_FINISH:** This bit needs to be set to 1 if SPI is using DMA multi-Block Chaining and the SW driver does not plan to re-enable the DMA manually after every Link List completion; 1 DMA finish disabled Note: Required for multi-block transfer 0 DMA finish not disabled

9.2.15 REG SPI_CS_CONTROL (SPI_CS_CONTROL) - Offset 224h

SPI_CS_CONTROL_Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 224h	0000F000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	1h RW	**CS3_POLARITY:** This Bit selects the Inactive/Idle polarity of SPI CS3 Signal. The steering logic will ensure that when switching to another active SPI CS port the inactive port will be forced to the inactive polarity, 0 = Low 1 = High
14	1h RW	**CS2_POLARITY:** This Bit selects the Inactive/Idle polarity of SPI CS2 Signal. The steering logic will ensure that when switching to another active SPI CS port the inactive port will be forced to the inactive polarity, 0 = Low 1 = High
13	1h RW	**CS1_POLARITY:** This Bit selects the Inactive/Idle polarity of SPI CS1 Signal. The steering logic will ensure that when switching to another active SPI CS port the inactive port will be forced to the inactive polarity, 0 = Low 1 = High

Bit Range	Default & Access	Field Name (ID): Description
12	1h RW	**CS0_POLARITY:** This Bit selects the Inactive/Idle polarity of SPI CS0 Signal. The steering logic will ensure that when switching to another active SPI CS port the inactive port will be forced to the inactive polarity, 0 = Low 1 = High
11:10	0h RO	**Reserved**
9:8	0h RW	**CS1_OUTPUT_SEL:** These Bits select which SPI CS Signal is to be driven by the SSP Frame (CS). The steering logic will ensure that when switching to another active SPI CS port the inactive port will be forced to the inactive polarity defined by the corresponding SPI CS Polarity Bit, 00 = CS 0 01 = CS 1 10 = CS 2 11 = CS 3
7:2	0h RO	**Reserved**
1	0h RW	**CS_STATE:** Manual SW control of SPI Chip Select (CS) 0 = CS is set to low 1 = CS is set to high MCC: The state of this bit 0=>CS asserted; 1 => CS de-asserted. The state of the CS pin also includes the polarity setting in bits 15:12 of this register.
0	0h RW	**CS_MODE:** SPI Chip Select Mode Section. 0 = HW Mode- CS is under SSP control 1 = SW Mode CS is under SW Control using cs_state bit

9.2.16 REG SW_SCRATCH_0 (SW_SCRATCH_0) - Offset 228h

SW_SCRATCH_0_Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 228h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**REG_SW_SCRATCH_0:** Scratch Pad Register for SW to generated Local DATA for iDMA

9.2.17 REG SW_SCRATCH_1 (SW_SCRATCH_1) - Offset 22Ch

SW_SCRATCH_1_Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 22Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**REG_SW_SCRATCH_1:** Scratch Pad Register for SW to generated Local DATA for iDMA

9.2.18 REG SW_SCRATCH_2 (SW_SCRATCH_2) - Offset 230h

SW_SCRATCH_2_Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 230h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**REG_SW_SCRATCH_2:** Scratch Pad Register for SW to generated Local DATA for iDMA

9.2.19 REG SW_SCRATCH_3 (SW_SCRATCH_3) - Offset 234h

SW_SCRATCH_3_Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 234h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**REG_SW_SCRATCH_3:** Scratch Pad Register for SW to generated Local DATA for iDMA

9.2.20 REG CLOCK_GATE (CLOCK_GATE) - Offset 238h

CLOCK_GATE_Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 238h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:2	0h RW	**SW_DMA_CLK_CTL:** DMA Clock Gate Control bits, 00-hw clk en 01-rsv 10-force off 11-force on
1:0	0h RW	**SW_IP_CLK_CTL:** IP Clock Gate Control bits, 00-hw clk en 01-rsv 10-force off 11-force on

9.2.21 REG REMAP_ADDR_LO (REMAP_ADDR_LO) - Offset 240h

REMAP_ADDR_LO_Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 240h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SPI_REMAP_ADDR_LOW:** Low 32 bits of BAR address read by SW

9.2.22 REG REMAP_ADDR_HI (REMAP_ADDR_HI) - Offset 244h

REMAP_ADDR_HI_Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 244h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SPI_REMAP_ADDR_HIGH:** High 32 bits of BAR address read by SW

9.2.23 REG DEVIDLE_CONTROL (DEVIDLE_CONTROL) - Offset 24Ch

This register allows a device driver to enable/disable a devices entry into DevIdle. By enabling DevIdle, SW specifies that it will not touch the device without accessing this register prior to accessing any other MMIO device register. Detailed SW DevIdle entry/exit flows are defined in the Chassis Power Management and Device Idle PFAS specifications, reference

Type	Size	Offset	Default
MMIO	32 bit	BAR + 24Ch	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**INTR_REQ_CAPABLE:** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0.
3	1h RW/1C	**RESTORE_REQUIRED:** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up. Note: If SW is setting bit 3 together with any other bit of this register, only bit 3 is written; SW is required to do 2 writes in this case: bit 3 first and all other bits second. This (Restore Required) field of the D0i3C register needs to be preserved during the S0ix restore window even though the D0i3C register is being restored (during restore window, RR bit should be restored to 1.
2	0h RW	**DEVIDLE:** SW sets this bit to 1 to move the function into the DevIdle state. Writing this bit to 0 will return the function to the fully active D0 state (D0i0).
1	0h RO	**Reserved**
0	0h RO	**CMD_IN_PROGRESS:** HW sets this bit on a 1->0 or 0->1 transition of DEVIDLE. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. HW clears this bit upon completing the DevIdle transition command. When clear, all the other bits in the register are valid and SW may write to any bit. If Interrupt Request (IR) was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect.

9.2.24 REG DEL_RX_CLK (DEL_RX_CLK) - Offset 250h

MMIO (Convergence Layer) bit per SPI Controller allows selection of the Delayed Rx Clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 250h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**RX_CLK_SEL:** 2'b00: The output of the internal (M/N and/or baud rate) clock divider is used as-is to clock in the receive data to the RxFIFO. 2'b01: An internally delayed version of the internal clock divider output is used to clock in the receive data to the RxFIFO. This allows some additional setup time on the PCH side. 2'b10: The receive data is clocked on the subsequent negedge of the Tx clock, allowing a full cycle propagation delay on the platform. 2'b11: The receive data is clocked on the subsequent negedge of the delayed Rx clock, maximizing the amount of delay allowed for capturing the receive data. This mode is required for 50 MHz operation.

9.2.25 REG SPI_HVM_MISR_CRCOUT (SPI_HVM_MISR_CRCOUT) - Offset 280h

SPI HVM MISR CRCOUT

Type	Size	Offset	Default
MMIO	32 bit	BAR + 280h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	FFFFh RO	**SPI_HVM_MISR_CRCOUT:** SPI MISR Output for HVM

9.2.26 REG CAPABLITIES (CAPABLITIES) - Offset 2FCh

Capabilities Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2FCh	00000620h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RO	**SPI_CS3_OE_STAT:** 0 = unconnected 1 = connected
11	0h RO	**SPI_CS2_OE_STAT:** 0 = unconnected 1 = connected
10	1h RO	**SPI_CS1_OE_STAT:** 0 = unconnected 1 = connected
9	1h RO	**SPI_CS0_OE_STAT:** 0 = unconnected 1 = connected
8	0h RO	**IDMA_PRESENT:** 0= DMA present 1= DMA not present
7:4	2h RO	**INSTANCE_TYPE:** I2C, SPI or UART
3:0	0h RO	**INSTANCE_NUMBER:** Instance number

9.2.27 REG SAR_LO0 (SAR_LO0) - Offset 800h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer. Source Address Register for lower 32-bits for Channels 0-1

Type	Size	Offset	Default
MMIO	32 bit	BAR + 800h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SAR_LO:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected)6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

9.2.28 REG SAR_HI0 (SAR_HI0) - Offset 804h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer. Source Address Register for upper 32-bits for Channels 0-1

Type	Size	Offset	Default
MMIO	32 bit	BAR + 804h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SAR_HI:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

9.2.29 REG DAR_LO0 (DAR_LO0) - Offset 808h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer. Destination Address Register for Channels 0-1

Type	Size	Offset	Default
MMIO	32 bit	BAR + 808h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DAR_LO:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e.CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected(i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

9.2.30 REG DAR_HI0 (DAR_HI0) - Offset 80Ch

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer. Destination Address Register for Upper 32-bits for Channels 0-1

Type	Size	Offset	Default
MMIO	32 bit	BAR + 80Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DAR_HI:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e.CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected(i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

9.2.31 REG LLP_LO0 (LLP_LO0) - Offset 810h

You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled. The LLP register has two functions: The logical result of the equation LLP.LOC!=0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC!= 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC!= 0 contains the pointer to the next LLI for block chaining using linked lists. The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 810h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**Reserved**

9.2.32 REG LLP_HI0 (LLP_HI0) - Offset 814h

You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled. The LLP register has two functions: The logical result of the equation LLP.LOC ! 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC!= 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 814h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.

9.2.33 REG CTL_LO0 (CTL_LO0) - Offset 818h

This register contains fields that control the DMA transfer. The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 818h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Reserved (00) Memory to Peripheral (01) Peripheral to Memory (10) Reserved (11) Flow Control is always assigned to the DMA.
19	0h RO	**Reserved**
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. Source BURST SIZE (in DW) = (2 ^ SRC_TR_WIDTH)
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**Reserved**
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE (IN DW) = (2^ MSIZE) (i.e. 2 to-the-power-of MSIZE) 1.Transferred Bytes Per Burst = BURST_SIZE * (2 ^ TR_WIDTH) Since Max Burst Length is limited by the OCP fabric to 16 DW, encodings 101 (32 DW), 110 (64 DW) and 111 (128 DW) are not supported by the fabric. 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
3:1	0h RW	**DST_TR_WIDTH:** BURST SIZE (in DW) = (2^ MSIZE) (i.e. 2 to-the-power-of MSIZE) Transferred Bytes Per Burst = BURST_SIZE * (2 ^ TR_WIDTH) Since Max Burst Length is limited by the South-Complex OCP fabric to 16 DW, encodings 101 (32 DW), 110 (64 DW) and 111 (128 DW) are not supported by the fabric. For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

9.2.34 REG CTL_HI0 (CTL_HI0) - Offset 81Ch

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled. If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 81Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.

Bit Range	Default & Access	Field Name (ID): Description
28:18	0h RO	**Reserved**
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	00000h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It does not means Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register.

9.2.35 REG SSTAT0 (SSTAT0) - Offset 820h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block

Type	Size	Offset	Default
MMIO	32 bit	BAR + 820h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

9.2.36 REG DSTAT0 (DSTAT0) - Offset 828h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI.

Note: This register is a temporary placeholder for the destination status information on its way to the DSTATx register

location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 828h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface

9.2.37 REG SSTATAR_LO0 (SSTATAR_LO0) - Offset 830h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 830h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTATAR_LO:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block

9.2.38 REG SSTATAR_HI0 (SSTATAR_HI0) - Offset 834h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 834h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTATAR_HI:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block

9.2.39 REG DSTATAR_LO0 (DSTATAR_LO0) - Offset 838h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 838h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTATAR_LO:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

9.2.40 REG DSTATAR_HI0 (DSTATAR_HI0) - Offset 83Ch

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 83Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTATAR_HI:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

9.2.41 REG CFG_LO0 (CFG_LO0) - Offset 840h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Type	Size	Offset	Default
MMIO	32 bit	BAR + 840h	00000203h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0h RO	**Reserved**
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length: 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE))
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length: 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE))
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17:11	0h RO	**Reserved**
10	0h RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit affects only when CH_SUSPEND ia asserted
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**Reserved**
3	0h RW	**HSHAKE_NP_WR:** 0x1: Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0: Issues Posted writes on HW-Handshake on DMA Write Port (Except end-ofblock writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1: Forces ALL writes to be Non-Posted on DMA Write Port 0x0: Non-Posted Writes will only be used at end of block transfers and in HWHandshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used
1	1h RW	**SRC_BURST_ALIGN:** 0x1: SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0: SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1: DST Burst Transfers are broken at a Burst Length aligned boundary 0x0: DST Burst Transfers are not broken at a Burst Length aligned boundary

9.2.42 REG CFG_HI0 (CFG_HI0) - Offset 844h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Type	Size	Offset	Default
MMIO	32 bit	BAR + 844h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:18	000h RW	**WR_ISSUE_THD:** Write Issue Threshold. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
17:8	000h RW	**RD_ISSUE_THD:** Read Issue Threshold. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID: Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface.
3:0	0h RW	**SRC_PER:** Source Peripheral ID: Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface.

9.2.43 REG SGR0 (SGR0) - Offset 848h

The Source Gather register contains two fields: Source gathers count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gathers interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 848h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	00000h RW	**SGI:** Source gather interval.

9.2.44 REG DSR0 (DSR0) - Offset 850h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC). Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI). Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 850h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries
19:0	00000h RW	**DSI:** Destination scatter interval.

9.2.45 REG SAR_LO1 (SAR_LO1) - Offset 858h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer. Source Address Register for lower 32-bits for Channels 0-1

Type	Size	Offset	Default
MMIO	32 bit	BAR + 858h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SAR_LO:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

9.2.46 REG RawTfr (RAWTFR) - Offset AC0h

Interrupt events are stored in this Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + AC0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**RAW:** Raw interrupt status for ch 1 and ch0

9.2.47 REG RawBlock (RAWBLOCK) - Offset AC8h

RawBlock - Raw Status for Block Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + AC8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**RAW:** Raw interrupt status for ch 1 and ch0

9.2.48 REG RawSrcTran (RAWSRCTRAN) - Offset AD0h

RawSrcTran - Raw Status for Source Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + AD0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**RAW:** Raw interrupt status for ch 1 and ch0

9.2.49 REG RawDstTran (RAWDSTTRAN) - Offset AD8h

RawDstTran - Raw Status for Destination Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + AD8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**RAW:** Raw interrupt status for ch 1 and ch0

9.2.50 REG RawErr (RAWERR) - Offset AE0h

RawErr - Raw Status for Error Interrupts Register Error interrupt will be asserted by the DMA in the following cases: IOSF Fabric returns an Unsuccessful Completion with UR Completion Status for a Non-Posted transaction issued by the DMA to Memory. This error occurs when an invalid address range is programed into the DMA SRC/Dest Field outside of the Host memory region on the memory side of the DMA transaction IOSF2OCP bridge will return error (triggering error interrupt from DMA) if the IOSF2OCP Bridge is programmed incorrectly. Peripheral side transaction where invalid addressing can result in an OCP fabric error which will be translated into an Error Interrupt. The SW should view this error as a serious programming error and handle it according to the specified error handling procedures for the product and OS.

Type	Size	Offset	Default
MMIO	32 bit	BAR + AE0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**RAW:** Raw interrupt status for ch 1 and ch0

9.2.51 REG StatusTfr (STATUSTFR) - Offset AE8h

Status for Transfer Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + AE8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**STATUS:** Status for interrupt for ch 1 and ch0

9.2.52 REG StatusBlock (STATUSBLOCK) - Offset AF0h

statusBlock: Status for Block Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + AF0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**STATUS:** Status for interrupt for ch 1 and ch0

9.2.53 REG StatusSrcTran (STATUSSRCTRAN) - Offset AF8h

StatusSrcTran: Status for Source Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + AF8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**STATUS:** Status for interrupt for ch 1 and ch0

9.2.54 REG StatusDstTran (STATUSDSTTRAN) - Offset B00h

StatusDstTran: Status for Destination Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B00h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**STATUS:** Status for interrupt for ch 1 and ch0

9.2.55 REG StatusErr (STATUSERR) - Offset B08h

StatusErr, Status for Error Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B08h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**STATUS:** Status for interrupt for ch 1 and ch0

9.2.56 REG MaskTfr (MASKTFR) - Offset B10h

Mask for Transfer Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable ch 1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	**Reserved**
1:0	0h RW	**INT_MASK:** Interrupt mask per ch1 and ch0. 0-mask 1-unmask

9.2.57 REG MaskBlock (MASKBLOCK) - Offset B18h

MaskBlock: Mask for Block Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	**Reserved**
1:0	0h RW	**INT_MASK:** Interrupt mask ch1 and ch0. 0-mask 1-unmask

9.2.58 REG MaskSrcTran (MASKSRCTRAN) - Offset B20h

Mask for Source Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	**Reserved**
1:0	0h RW	**INT_MASK:** Interrupt mask ch1 and ch0. 0-mask 1-unmask

9.2.59 REG MaskDstTran (MASKDSTTRAN) - Offset B28h

Mask for Destination Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B28h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	**Reserved**
1:0	0h RW	**INT_MASK:** Interrupt mask ch1 and ch0. 0-mask 1-unmask

9.2.60 REG MaskErr (MASKERR) - Offset B30h

Mask for Error Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	**Reserved**
1:0	0h RW	**INT_MASK:** Interrupt mask ch1 and ch0. 0-mask 1-unmask

9.2.61 REG ClearTfr (CLEARTFR) - Offset B38h

Clear for Transfer Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h WO	**CLEAR:** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

9.2.62 REG ClearBlock (CLEARBLOCK) - Offset B40h

Clear for Block Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h WO	**CLEAR:** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

9.2.63 REG ClearSrcTran (CLEARSRCTRAN) - Offset B48h

Clear for Source Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h WO	**CLEAR:** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

9.2.64 REG ClearDstTran (CLEARDSTTRAN) - Offset B50h

Clear for Destination Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h WO	**CLEAR:** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

9.2.65 REG ClearErr (CLEARERR) - Offset B58h

Clear for Error Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h WO	**CLEAR:** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

9.2.66 REG StatusInt (STATUSINT) - Offset B60h

The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran, StatusErr is Ored to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**ERR:** OR of the contents of StatusErr register.
3	0h RO	**DSTT:** OR of the contents of StatusDst register.
2	0h RO	**SRCT:** OR of the contents of StatusSrcTran register
1	0h RO	**BLOCK:** OR of the contents of StatusBlock register.
0	0h RO	**TFR:** OR of the contents of StatusTfr register.

9.2.67 REG DmaCfgReg (DMACFGREG) - Offset B98h

This register is used to enable the DMA, which must be done before any channel activity can begin. If the global channel enable bit is cleared while any channel is still active, then DmaCfgReg.DMA_EN still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DmaCfgReg.DMA_EN bit returns 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**DMA_EN:** DMA Enable bit. 0 = DMA Disabled 1 = DMA Enabled

9.2.68 REG ChEnReg (CHENREG) - Offset BA0h

This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in

order to find out which channels are currently inactive, it can then enable an inactive channel with the required priority. All bits of this register are cleared to 0 when the global DMA channel enable bit, DmaCfgReg(0), is 0. When the global channel enable bit is 0, then a write to the ChEnReg register is ignored and a read will always read back 0. The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE, is asserted on the same OCP write transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BA0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h WO	**CH_EN_WE:** Channel enable write enable.
7:2	0h RO	**Reserved**
1:0	0h RW	**CH_EN:** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

9.3 GSPI PCR Registers Summary

Table 9-3. Summary of GSPI PCR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
224h	4	PCICFGCTR10 PCI Configuration Control 10 Register (PCICFGCTR10)	00000100h
228h	4	PCICFGCTR11 PCI Configuration Control 11 Register (PCICFGCTR11)	00000100h
22Ch	4	PCICFGCTR12 PCI Configuration Control 12 Register (PCICFGCTR12)	00000100h

9.3.1 PCICFGCTR10 PCI Configuration Control 10 Register (PCICFGCTR10) - Offset 224h

Controls The Pci Configuration Space

Type	Size	Offset	Default
MMIO	32 bit	FDCD0000h + 224h	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RO	**Reserved**
27:20	00h RW	**PCI_IRQ10:** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	00h RW	**ACPI_IRQ10:** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	1h RW	**IPIN10:** Interrupt Pin: This register indicates the values to be used for Global Interrupts.
7	0h RW	**BAR1_DISABLE10:** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	00h RW	**PME_SUPPORT10:** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI_INTR_EN10:** When set, the Bridge uses ACPI Sideband opcodes for messages When cleared, the Bridge uses global IOSF opcodes
0	0h RW	**PCI_CFG_DIS10:** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

9.3.2 PCICFGCTR11 PCI Configuration Control 11 Register (PCICFGCTR11) - Offset 228h

Controls the PCI configuration space

Type	Size	Offset	Default
MMIO	32 bit	FDCD0000h + 228h	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RO	**Reserved**
27:20	00h RW	**PCI_IRQ11:** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	00h RW	**ACPI_IRQ11:** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	1h RW	**IPIN11:** Interrupt Pin: This register indicates the values to be used for Global Interrupts.
7	0h RW	**BAR1_DISABLE11:** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	00h RW	**PME_SUPPORT11:** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI_INTR_EN11:** When set, the Bridge uses ACPI Sideband opcodes for messages When cleared, the Bridge uses global IOSF opcodes
0	0h RW	**PCI_CFG_DIS11:** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

9.3.3 PCICFGCTR12 PCI Configuration Control 12 Register (PCICFGCTR12) - Offset 22Ch

Controls the PCI configuration space

Type	Size	Offset	Default
MMIO	32 bit	FDCD0000h + 22Ch	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RO	**Reserved**
27:20	00h RW	**PCI_IRQ12:** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	00h RW	**ACPI_IRQ12:** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	1h RW	**IPIN12:** Interrupt Pin: This register indicates the values to be used for Global Interrupts.
7	0h RW	**BAR1_DISABLE12:** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	00h RW	**PME_SUPPORT12:** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI_INTR_EN12:** When set, the Bridge uses ACPI Sideband opcodes for messages When cleared, the Bridge uses global IOSF opcodes
0	0h RW	**PCI_CFG_DIS12:** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

10 TSN GbE Controller

10.1 TSN GbE Configuration Registers Summary

This chapter documents the registers in Bus: 0, Device: 30, Function: 4.

DID Values:

• TSN GbE Controller - D30: F4

- 4B30h (Reserved)

- 4B32h (SGMII: 1Gb and 2.5Gb Mode)

Note: SGMII 1Gb & 2.5Gb Modes share the same Device ID. The GCR.LINK_MODE register field shall be used to configure operation at 1Gb or 2.5Gb.

The Function is discovered by software as a Root Complex integrated Endpoint (RCiEP). The PCI Bus Number, Device Number, and Function Number are assigned by the PCH design and not enumerated. Because it is an RCiEP, some of the register fields are designed to be altered by BIOS for a particular system implementation.

Note: BIOS has the capability to disable software access to the PCI Configuration Space of this Function. When disabled, the Function returns Unsupported Request (UR) to requests to access its configuration registers.

Table 10-1. Summary of Bus: 0, Device: 30, Function: 4 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID and Vendor ID Register (DEVVENDID)	4B320000h
4h	4	Status and Command (STATUSCOMMAND)	00100000h
8h	4	Revision ID and Class Code (REVCLASSCODE)	00000000h
Ch	4	Cache Line Latency Header and BIST (CLLATHEADERBIST)	00000000h
10h	4	Base Address Register (BAR)	00000000h
14h	4	Base Address Register High (BAR_HIGH)	00000000h
18h	4	Base Address Register1 (BAR1)	00000000h
1Ch	4	Base Address Register1 High (BAR1_HIGH)	00000000h
2Ch	4	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)	00000000h
30h	4	Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)	00000000h
34h	4	Capabilities Pointer (CAPABILITYPTR)	00000080h
3Ch	4	Interrupt Register (INTERRUPTREG)	00000100h
40h	4	PCIe Capabilities Register (PCIECAPREG)	00920010h
44h	4	PCIe Device Capability Register (DEVCAPREG)	10008FC0h
48h	4	PCIe Device Control Status Register (DEVCTRLSTAT)	00000000h
64h	4	PCIe Device Capability2 Register (DEVCAPREG2)	00000000h
68h	4	PCIe Device Control2 Status Register (DEVCTRLSTAT2)	00000000h
80h	4	Power Management Capability ID (POWERCAPID)	48030001h
84h	4	Power Management Control And Status Register (PMECTRLSTATUS)	00000008h
90h	4	PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD)	F0140009h
94h	4	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG)	01400010h
98h	4	Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)	00000000h
9Ch	4	Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG)	00000000h
A0h	4	D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG)	00000800h
B0h	4	General Purpose Read Write Register1 (GEN_PCI_REGRW1)	00000000h
B4h	4	General Purpose Read Write Register2 (GEN_PCI_REGRW2)	00000000h
B8h	4	General Purpose Read Write Register3 (GEN_PCI_REGRW3)	00000000h
BCh	4	General Purpose Read Write Register4 (GEN_PCI_REGRW4)	00000000h
C0h	4	General Purpose Input Register (GEN_INPUT_REG)	00000000h
D0h	4	MSI Capability Register (MSI_CAP_REG)	01800005h
D4h	4	MSI Message Low Address (MSI_ADDR_LOW)	00000000h
D8h	4	MSI Message High Address (MSI_ADDR_HIGH)	00000000h
DCh	4	MSI Message Data (MSI_MSG_DATA)	00000000h
E0h	4	MSI Mask Register (MSI_MASK)	00000000h
E4h	4	MSI Pending Register (MSI_PENDING)	00000000h
F8h	4	Manufacturers ID (MANID)	00000000h

10.1.1 Device ID and Vendor ID Register (DEVVENDID) — Offset 0h

Device ID and Vendor ID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 0h	4B320000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4B32h RO/P	**Device ID Field (DEVICEID):** Device ID identifies the particular PCI device - 4B30h (Reserved) - 4B32h (SGMII: 1Gb and 2.5Gb Mode) ***Note:*** SGMII 1Gb & 2.5Gb Modes share the same Device ID. The GCR.LINK_MODE register field shall be used to configure operation at 1Gb or 2.5Gb.
15:0	0000h RO	**Vendor ID Field (VENDORID):** Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device

10.1.2 Status and Command (STATUSCOMMAND) — Offset 4h

Command Register and Status Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**Detected Parity Error (DPE):** Detected Parity Error
30	0h RW/1C	**Signaled System Error (SSE):** Signaled System Error
29	0h RW/1C	**RMA Field (RMA):** Received Master Abort
28	0h RW/1C	**RTA Field (RTA):** Received Target Abort
27:25	0h RO	**Reserved**
24	0h RW/1C	**Master Data Parity Error (MDPE):** Master Data Parity Error
23:21	0h RO	**Reserved**
20	1h RO	**Cap List Field (CAPLIST):** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**Interrupt Status Field (INTR_STATUS):** Interrupt Status: This bit reflects state of interrupt in the device

Bit Range	Default & Access	Field Name (ID): Description
18:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** If '1', SB Interrupt generation is disabled If '0', SB Interrupt generation is enabled
9	0h RO	**Reserved**
8	0h RW	**SERR Enable Field (SERR_ENABLE):** SERR Enable Not implemented
7	0h RO	**Reserved**
6	0h RW	**Parity Error Response Enable (PERE):** Parity Error Response Enable
5:3	0h RO	**Reserved**
2	0h RW	**BME Field (BME):** Bus Master Enable
1	0h RW	**MSE Field (MSE):** Memory Space Enable
0	0h RO	**Reserved**

10.1.3 Revision ID and Class Code (REVCLASSCODE) — Offset 8h

Revision ID register and Class Code Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Revision Id Field (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	00h RO/P	**Class Code Field (RID):** Revision ID identifies the revision of particular PCI device.

10.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST) — Offset Ch

Cache Line size as RW with def 0 Latency timer RW with def 0 Header type with Type 0 configuration header and Reserved BIST Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**MultifunctionDevice Field (MULFNDEV):** Multi-Function Device: This bit is set only if the device has multiple functions. For VF, this bit is set to 0
22:16	00h RO	**Header Type Field (HEADERTYPE):** Header Type: Implements Type 0 Configuration header
15:8	00h RO	**Latency Timer Field (LATTIMER):** Latency Timer:. This register is implemented as R/W with default as 0
7:0	00h RW/P	**Cache Line Size Field (CACHELINE_SIZE):** Cache Line Size: Does not apply to PCI Express. PCI Express spec requires this to be implemented as an R/W register but has no functional impact on the AMBA Device connected. This field is RO and tied to 0 for VFs.

10.1.5 Base Address Register (BAR) — Offset 10h

Base Address Register low [31:2] type[2:1] in 32bit or 64bit address range and memory space indicator [0].

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR):** Base Address Register Low Base address of the AXI fabric memory space. Taken from Strap values as ones
11:4	00h RO	**Size Field (SIZEINDICATOR):** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**Prefetchable Field (PREFETCHABLE):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE0):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** Memory Space Indicator: 0 indicates this BAR is present in the memory space.

10.1.6 Base Address Register High (BAR_HIGH) — Offset 14h

Base Address Register High enabled if [2:1] of BAR_HIGH is 10.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR_HIGH):** Base Address High - MSB

10.1.7 Base Address Register1 (BAR1) — Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K type in [2:1] and memory space indicator in [0].

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR1):** Base Address1 This field is present if BAR1 is enabled through private configuration space.
11:4	00h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

10.1.8 Base Address Register1 High (BAR1_HIGH) — Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1_HIGH Register is 10.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR1_HIGH):** Base Address: Base address of the AXI fabric memory space. Taken from Strap values as ones

10.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID) — Offset 2Ch

SVID Register along with SID Register is to distinguish subsystem from another.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system.
15:0	0000h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

10.1.10 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) — Offset 30h

Expansion ROM Base Address Register is a RO indicates support for Expansion ROMs

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Expansion Rom Base Address Field (EXPANSION_ROM_BASE):** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

10.1.11 Capabilities Pointer (CAPABILITYPTR) — Offset 34h

Capabilities Pointer Register indicates what the next capability is.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Capabilities Pointer: Indicates what the next capability is.

10.1.12 Interrupt Register (INTERRUPTREG) — Offset 3Ch

Interrupt Line Register isn't used in Bridge directly Interrupt Pin Register reflects the IPIN value in private configuration space. MIN_GNT Register indicating the requirement of latency timers and MAX_LAT Register max latency.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 3Ch	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**Min GNT Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	**Reserved**
11:8	1h RO	**Interrupt Pin Field (INTPIN):** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW/P	**Interrupt Line Field (INTLINE):** Interrupt Line: It is used to communicate to software the interrupt line to which the interrupt pin is connected

10.1.13 PCIe Capabilities Register (PCIECAPREG) — Offset 40h

PCIe Capabilities Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 40h	00920010h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:25	00h RO/V	**Interrupt Message Number Field (INTR_MSG_NUM):** PCIe Interrupt Message Number
24	0h RO	**Slot Implemented Field (SLOT_IMPLEMENTED):** Slot Implemented. Tied to 0
23:20	9h RO	**Dev Port Type Field (DEV_PORT_TYPE):** Device Port Type. Taken from strap
19:16	2h RO	**Cap Version Field (CAP_VER):** PCI Capability Version
15:8	00h RO	**Next Capability Pointer Field (NEXT_CAP_PTR):** Next Capability Pointer
7:0	10h RO	**Capability ID Field (PCIE_CAP_ID):** PCIe Capability ID

10.1.14 PCIe Device Capability Register (DEVCAPREG) — Offset 44h

PCIe Device Cap Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 44h	10008FC0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	1h RO	**FLR Capability Field (FLR_CAP):** FLR Capability
27:26	0h RO	**Captured Slot Power Limit Scale Field (CAP_SLOT_PWR_LIM_SCALE):** Captured Slot Power Limit Scale. Tied to 0
25:18	00h RO	**Captured Slot Power Limit Value Field (CAP_SLOT_PWR_LIM_VAL):** Captured Slot Power Limit Value. Tied to 0
17:16	0h RO	**Reserved**
15	1h RO	**RB error PTR Field (RB_ERR_RPTR):** Role Based Error Reporting
14:12	0h RO	**Reserved**
11:9	7h RO	**EP L01 Acceptable Latency Field (EP_L1_ACC_LAT):** L1 Acceptable Latency
8:6	7h RO	**EP L0 Acceptable Latency Field (EP_L0_ACC_LAT):** L0 Acceptable Latency
5	0h RO	**ETF Support Field (ETF_SUPPORT):** Extended Tag Field Support
4:3	0h RO	**Phantom Functions Support Field (PHANTOM_FUNC_SUPPORT):** Phantom Functions SUPPORT. NA for Bridge
2:0	0h RO	**Max Pl Size Support Field (MAX_PL_SIZE_SUPPORT):** Max Payload Size

10.1.15 PCIe Device Control Status Register (DEVCTRLSTAT) — Offset 48h

PCIe Device Status Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RO/V	**TXN Pending Field (TXN_PENDING):** Transaction Pending bit
20	0h RO	**Aux Power Detected Field (AUX_PWR_DETECTED):** Aux Power Detected. Always tied to 0
19	0h RW/1C	**UR Field (UR_DETECTED):** Unsupported Request Detected
18	0h RW/1C	**Fatal Error Detected Field (FER_DETECTED):** Fatal Error Detected
17	0h RO	**Non Fatal Err Detected Field (NFER_DETECTED):** Non Fatal Error Detected
16	0h RO	**Correctable Error Detected Field (CER_DETECTED):** Correctable Error Detected
15	0h WO	**Initiate FLR Field (INITIATE_FLR):** Initiate Function Level Reset
14:12	0h RO	**Max Read Request Size Field (MAX_RD_REQ_SIZE):** Max Read Request Size
11	0h RW	**Enable No Snoop Field (EN_NS):** Enable No Snoop
10	0h RO	**Aux Power Detected Field (AUX_PWR_PM_EN):** Aux Power Enable
9	0h RO	**Phantom Function En Field (PHANTOM_FUNC_EN):** Phantom Function Enable. Not support by Bridge
8	0h RW	**ETF En Field (ETF_EN):** Extended Tag Field Enable
7:5	0h RO	**Max Payload Size Field (MAX_PL_SIZE):** Maximum Payload Size
4	0h RW	**Enable Relaxed Ordering Field (EN_RO):** Enable Relaxed Ordering
3	0h RW	**UR Reporting En Field (URR_EN):** Unsupported Request Reporting Enable
2	0h RW	**Fatal Err Reporting En Field (FER_EN):** Fatal Error Reporting Enable
1	0h RW	**Non Fatal Err Reporting En Field (NFER_EN):** Non Fatal Error Reporting Enable
0	0h RW	**Correctable Error Reporting En Field (CER_EN):** Correctable Error Reporting Enable

10.1.16 PCIe Device Capability2 Register (DEVCAPREG2) — Offset 64h

PCIe Device Cap Register2.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:22	0h RO	**Max End2end TLP Prefix Field (MAX_EE_TLP_PREFIXES):** Max End2End TLP Prefixes
21	0h RO	**End2end TLP Prefix Supported Field (EE_TLP_PREFIX_SUPPORT):** End2End TLP Prefixes Support
20	0h RO	**Ext Format Support Field (EXTD_FMT_SUPPORT):** Extended Format Support
19:18	0h RO	**OBFF Support Field (OBFF_SUPPORT):** PCI OBFF Support
17:14	0h RO	**Reserved**
13:12	0h RO	**TPH Completer Supported Field (TPH_CPL_SUPPORT):** TPH Completer Support
11	0h RO	**LTR Support Field (LTR_SUPPORT):** LTR Support
10	0h RO	**No RO Enable Field (NRO_EN_PRPR_PASS):** No RO based PR-PR Passing
9	0h RO	**CAS Cpl 128 Support Field (CAS_CPL_SUPPORT_128):** CAS128 Support
8	0h RO	**CAS Cpl 64 Support Field (ATM_OP_CPL_SUPPORT_64):** CAS64 Completion Support
7	0h RO	**CAS Cpl 32 Support Field (ATM_OP_CPL_SUPPORT_32):** CAS32 Completion Support
6	0h RO	**Atomic Operation Routing Field (ATOR_SUPPORT):** Atomic Operation Routing Support
5	0h RO	**PCI Ari Forwarding Support Field (ARI_FWD_SUPPORT):** ARI Forwarding Support
4	0h RO	**Cpl Timeout Disable Support Field (CPL_TO_DIS_SUPPORT):** Completion Timeout Disable Support
3:0	0h RO	**Cpl Timeout Range Support Field (CPL_TO_RNG_SUPPORT):** Completion Timeout Ranges Support

10.1.17 PCIe Device Control2 Status Register (DEVCTRLSTAT2) — Offset 68h

PCIe Device Status Register2.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RO	**End2end TLP Prefix Blocking Field (EE_TLP_PREFIX_EN):** End2End TLP Prefixes Blocking
14:13	0h RO	**OBFF Enable Field (OBFF_EN):** OBFF Enable
12:11	0h RO	**Reserved**
10	0h RW	**LTR Mechanism Enable Field (LTR_MECH_EN):** LTR Mechanism Enable
9	0h RO	**IDO Based Cpl Enable Field (IDO_CPL_EN):** IDO Completion Enable
8	0h RO	**IDO Based Request Enable Field (IDO_REQ_EN):** IDO Request Enable
7	0h RO	**Atomic Op Egress Blocking Field (ATM_OP_EGR_BLK):** Atomic Operation Egress Blocking
6	0h RO	**Atomic Op Requester Enable Field (ATM_OP_REQ_EN):** Atomic Operation Requester Enable
5	0h RO	**ARI Fwd Enable Field (ARI_FWD_EN):** ARI Forwarding Enable
4	0h RW	**Cpl Timeout Disable Field (CPL_TO_DIS):** Completion Timeout Disable Support
3:0	0h RW	**Cpl Timeout Value Field (CPL_TO_VAL):** Completion Timeout Value

10.1.18 Power Management Capability ID (POWERCAPID) — Offset 80h

Power Management Capability ID Register points to Next Capability Structure and Power Management Capability with pOwer Management Capabilities Register for PME Support and Version.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 80h	48030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	09h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	00h RO	**Next Cap Field (NXTCAP):** Next Capability: Points to the next capability structure.
7:0	01h RO	**Power Capability ID Field (POWER_CAP):** Power Management Capability: Indicates this is power management capability

10.1.19 Power Management Control and Status Register (PMECTRLSTATUS) — Offset 84h

Power Management Control and Status Register to set and read PME Status, PME Enable No Soft Reset and Power State.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/P	**PME Status Field (PMESTATUS):** PME Status: 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the AMBA Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0h RO	**Reserved**
8	0h RW/P	**PME Enable Field (PMEENABLE):** PME Enable: A 1 enables the function to assert PME#. When 0, PME# message on Sideband is disabled.
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset
2	0h RO	**Reserved**
1:0	0h RW	**Power State Field (POWERSTATE):** Power State: This field is used both to determine the current power state and to set a new power state

10.1.20 PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) — Offset 90h

PCI Device Vendor Specific Capability Register defines Vendor Specific Capability ID, Revision Length, Next Capability and CAPID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 90h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision ID Field (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	00h RO	**Next Capability Field (NEXT_CAP):** Next Capability
7:0	09h RO	**Capability ID Field (CAPID):** Capability ID

10.1.21 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) — Offset 94h

Extended Vendor Capability Register for VSEC Length, Revision and ID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific ID Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor specific Extended Capability revision
15:0	0010h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

10.1.22 Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) — Offset 98h

Software Location Pointer in MMIO space as an offset specified by BAR.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**SW LTR DWord Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR Bar Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW LTR Valid Field (SW_LAT_VALID):** This value is reflected from the SW LTR valid strap at the top level

10.1.23 Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) — Offset 9Ch

Device IDLE Pointer Register giving details on Device MMIO Offset, Location BAR NUM and D0i3 Valid Strap.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**D0i3 DWord Offset Field (DWORD_OFFSET):** contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** BAR NUM: Indicates that the D0i3 MMIO location is always at BAR0
0	0h RO	**D0i3 Valid Field (VALID):** Valid: This value is reflected from the D0i3 valid strap at the top level.

10.1.24 D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) — Offset A0h

D0idle_Max_Power_On_Latency Register set at boot and Power Control Enable Register to enable communication with the PGCB block below the Bridge.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + A0h	00000800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW/P	**HAE:** Hardware Autonomous Enable: If 1, then hardware may request power gating whenever it has reached an idle condition.
20	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW/P	**Sleep Enable Field (SLEEP_EN):** SE: Sleep Enable: If 1, then the function may assert Sleep during power gating. If 0, then function will never asset Sleep to the retention flops. Note that some platforms may default this bit to 0, others to 1.
18	0h RW/P	**D3 Hen Field (D3HEN):** DEVIDLE Enable (DEVIDLEN): If '1' then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set.
17	0h RW/P	**Device Idle En Field (DEVIDLEN):** PMCRE: PMC Request Enable
16	0h RW/P	**PMC Request Enable Field (PMCRE):** D3-Hot Enable (D3HEN): If 1, then function will power gate when idle and the PMCSR[1:0] register in the function ='11' (D3).
15:13	0h RO	**Reserved**
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** Power On Latency Scale
9:0	000h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** Power On Latency Value

10.1.25 General Purpose Read Write Register1 (GEN_PCI_REGRW1) — Offset B0h

General Purpose PCI Read Write Register1.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_PCI_REG_RW1):** General Purpose PCI Register: This register value is brought out as GEN_PCI_REG_RW1

10.1.26 General Purpose Read Write Register2 (GEN_PCI_REGRW2) — Offset B4h

General Purpose PCI Read Write Register2.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_PCI_REG_RW2):** General Purpose PCI Register: This register value is brought out as GEN_PCI_REG_RW2

10.1.27 General Purpose Read Write Register3 (GEN_PCI_REGRW3) — Offset B8h

General Purpose PCI Read Write Register3.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_PCI_REG_RW3):** General Purpose PCI Register: This register value is brought out as GEN_PCI_REG_RW3

10.1.28 General Purpose Read Write Register4 (GEN_PCI_REGRW4) — Offset BCh

General Purpose PCI Read Write Register4.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_PCI_REG_RW4):** General Purpose PCI Register: This register value is brought out as GEN_PCI_REG_RW4

10.1.29 General Purpose Input Register (GEN_INPUT_REG) — Offset C0h

General Purpose Input Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General Purpose Input Register: This register value reflects the value of GEN_REG_INPUT_RW

10.1.30 MSI Capability Register (MSI_CAP_REG) — Offset D0h

MSI Capability Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + D0h	01800005h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	1h RO	**Per Vector Masking Capability Field (PER_VECTOR_MSK_CAP):** Per Vector Masking Capability
23	1h RO	**MSI Capability Field (MSI_CAP_64B):** 64 bit message address capability
22:20	0h RW	**Multi Message En Field (MUL_MSG_EN):** Multiple Message Enable
19:17	0h RO	**Multi Message Cap Field (MUL_MSG_CAP):** Multiple Message Capable
16	0h RW	**MSI Enable Field (MSG_MSI_ENABLE):** MSI Enable: If 1, then the PCI Device is allowed to use MSI to request service. The PCI Device is prohibited to use INTx, when MSI is enabled If 0, then the PCI Device is prohibited from using MSI to request service.
15:8	00h RO	**Next Pointer Field (MSG_NXT_PTR):** Next Capability Pointer
7:0	05h RO	**MSI Capability Field (MSG_CAP_ID):** MSI Capability ID

10.1.31 MSI Message Low Address (MSI_ADDR_LOW) — Offset D4h

MSI Message Low Address.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**MSI Message Low Address Field (MSI_ADDR_LOW):** MSI Message Low Address
1:0	0h RO	**Reserved**

10.1.32 MSI Message High Address (MSI_ADDR_HIGH) — Offset D8h

MSI Message High Address.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Message High Address Field (MSI_ADDR_HIGH):** MSI Message High Address

10.1.33 MSI Message Data (MSI_MSG_DATA) — Offset DCh

MSI Message Data.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**MSI Message Data Field (MSI_MSG_DATA):** MSI Message Data

10.1.34 MSI Mask Register (MSI_MASK) — Offset E0h

MSI Mask Bits.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Mask Field (MSI_MASK):** MSI Mask bits

10.1.35 MSI Pending Register (MSI_PENDING) — Offset E4h

MSI Pending Bits.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**MSI Pending Field (MSI_PENDING):** MSI Pending bits

10.1.36 Manufacturers ID (MANID) — Offset F8h

Manufacturers ID register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/P	**Manufacturers ID Field (MANID):** Manufacturer ID: Default value comes from straps.

10.2 TSN GbE Memory Mapped Registers Summary

These are the I/O Registers in Memory Space for this Function that are accessible to BIOS and software running on the Host Root (RS0) processor. The Base Address Register (BAR) is located at offset 10h in PCI Configuration Space.

Table 10-2. Summary of TSN GbE Memory Mapped Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	MAC_CONFIGURATION	00000000h
4h	4	MAC_EXT_CONFIGURATION	00000000h
8h	4	MAC_PACKET_FILTER	00000000h
Ch	4	MAC_WATCHDOG_TIMEOUT	00000000h
10h	4	MAC_HASH_TABLE_REG0	00000000h
14h	4	MAC_HASH_TABLE_REG1	00000000h
50h	4	MAC_VLAN_TAG_CTRL	00000000h
54h	4	MAC_VLAN_TAG_DATA	00000000h
58h	4	MAC_VLAN_HASH_TABLE	00000000h
60h	4	MAC_VLAN_INCL	00000000h
64h	4	MAC_INNER_VLAN_INCL	00000000h
70h	4	MAC_Q0_TX_FLOW_CTRL	00000000h
74h	4	MAC_Q1_TX_FLOW_CTRL	00000000h
78h	4	MAC_Q2_TX_FLOW_CTRL	00000000h
7Ch	4	MAC_Q3_TX_FLOW_CTRL	00000000h
80h	4	MAC_Q4_TX_FLOW_CTRL	00000000h
84h	4	MAC_Q5_TX_FLOW_CTRL	00000000h
88h	4	MAC_Q6_TX_FLOW_CTRL	00000000h
8Ch	4	MAC_Q7_TX_FLOW_CTRL	00000000h
90h	4	MAC_RX_FLOW_CTRL	00000000h
94h	4	MAC_RXQ_CTRL4	00000000h
98h	4	MAC_TXQ_PRTY_MAP0	00000000h
9Ch	4	MAC_TXQ_PRTY_MAP1	00000000h
A0h	4	MAC_RXQ_CTRL0	00000000h
A4h	4	MAC_RXQ_CTRL1	00000000h
A8h	4	MAC_RXQ_CTRL2	00000000h
ACh	4	MAC_RXQ_CTRL3	00000000h
B0h	4	MAC_INTERRUPT_STATUS	00000000h
B4h	4	MAC_INTERRUPT_ENABLE	00000000h
B8h	4	MAC_RX_TX_STATUS	00000000h
C0h	4	MAC_PMT_CONTROL_STATUS	00000000h
C4h	4	MAC_RWK_PACKET_FILTER	00000000h
D0h	4	MAC_LPI_CONTROL_STATUS	00000000h
D4h	4	MAC_LPI_TIMERS_CONTROL	03E80000h
D8h	4	MAC_LPI_ENTRY_TIMER	00000000h
DCh	4	MAC_1US_TIC_COUNTER	00000063h
F8h	4	MAC_PHYIF_CONTROL_STATUS	00000000h
110h	4	MAC_VERSION	00005152h
114h	4	MAC_DEBUG	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
11Ch	4	MAC_HW_FEATURE0	0EFD73F7h
120h	4	MAC_HW_FEATURE1	119F7A28h
124h	4	MAC_HW_FEATURE2	22DF71C7h
128h	4	MAC_HW_FEATURE3	2C395632h
140h	4	MAC_DPP_FSM_INTERRUPT_STATUS	00000000h
144h	4	MAC_AXI_SLV_DPE_ADDR_STATUS	00000000h
148h	4	MAC_FSM_CONTROL	00000000h
14Ch	4	MAC_FSM_ACT_TIMER	00000000h
150h	4	SNPS_SCS_REG1	00000000h
200h	4	MAC_MDIO_ADDRESS	00000000h
204h	4	MAC_MDIO_DATA	00000000h
208h	4	MAC_GPIO_CONTROL	00000000h
20Ch	4	MAC_GPIO_STATUS	00000000h
210h	4	MAC_ARP_ADDRESS	00000000h
230h	4	MAC_CSR_SW_CTRL	00000000h
234h	4	MAC_FPE_CTRL_STS	00000000h
238h	4	MAC_EXT_CFG1	00000002h
240h	4	MAC_PRESN_TIME_NS	00000000h
244h	4	MAC_PRESN_TIME_UPDT	00000000h
300h	4	MAC_ADDRESS0_HIGH	8000FFFFh
304h	4	MAC_ADDRESS0_LOW	FFFFFFFFh
308h	4	MAC_ADDRESS1_HIGH	0000FFFFh
30Ch	4	MAC_ADDRESS1_LOW	FFFFFFFFh
310h	4	MAC_ADDRESS2_HIGH	0000FFFFh
314h	4	MAC_ADDRESS2_LOW	FFFFFFFFh
318h	4	MAC_ADDRESS3_HIGH	0000FFFFh
31Ch	4	MAC_ADDRESS3_LOW	FFFFFFFFh
320h	4	MAC_ADDRESS4_HIGH	0000FFFFh
324h	4	MAC_ADDRESS4_LOW	FFFFFFFFh
328h	4	MAC_ADDRESS5_HIGH	0000FFFFh
32Ch	4	MAC_ADDRESS5_LOW	FFFFFFFFh
330h	4	MAC_ADDRESS6_HIGH	0000FFFFh
334h	4	MAC_ADDRESS6_LOW	FFFFFFFFh
338h	4	MAC_ADDRESS7_HIGH	0000FFFFh
33Ch	4	MAC_ADDRESS7_LOW	FFFFFFFFh
340h	4	MAC_ADDRESS8_HIGH	0000FFFFh
344h	4	MAC_ADDRESS8_LOW	FFFFFFFFh
348h	4	MAC_ADDRESS9_HIGH	0000FFFFh
34Ch	4	MAC_ADDRESS9_LOW	FFFFFFFFh
350h	4	MAC_ADDRESS10_HIGH	0000FFFFh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
354h	4	MAC_ADDRESS10_LOW	FFFFFFFFh
358h	4	MAC_ADDRESS11_HIGH	0000FFFFh
35Ch	4	MAC_ADDRESS11_LOW	FFFFFFFFh
360h	4	MAC_ADDRESS12_HIGH	0000FFFFh
364h	4	MAC_ADDRESS12_LOW	FFFFFFFFh
368h	4	MAC_ADDRESS13_HIGH	0000FFFFh
36Ch	4	MAC_ADDRESS13_LOW	FFFFFFFFh
370h	4	MAC_ADDRESS14_HIGH	0000FFFFh
374h	4	MAC_ADDRESS14_LOW	FFFFFFFFh
378h	4	MAC_ADDRESS15_HIGH	0000FFFFh
37Ch	4	MAC_ADDRESS15_LOW	FFFFFFFFh
380h	4	MAC_ADDRESS16_HIGH	0000FFFFh
384h	4	MAC_ADDRESS16_LOW	FFFFFFFFh
388h	4	MAC_ADDRESS17_HIGH	0000FFFFh
38Ch	4	MAC_ADDRESS17_LOW	FFFFFFFFh
390h	4	MAC_ADDRESS18_HIGH	0000FFFFh
394h	4	MAC_ADDRESS18_LOW	FFFFFFFFh
398h	4	MAC_ADDRESS19_HIGH	0000FFFFh
39Ch	4	MAC_ADDRESS19_LOW	FFFFFFFFh
3A0h	4	MAC_ADDRESS20_HIGH	0000FFFFh
3A4h	4	MAC_ADDRESS20_LOW	FFFFFFFFh
3A8h	4	MAC_ADDRESS21_HIGH	0000FFFFh
3ACh	4	MAC_ADDRESS21_LOW	FFFFFFFFh
3B0h	4	MAC_ADDRESS22_HIGH	0000FFFFh
3B4h	4	MAC_ADDRESS22_LOW	FFFFFFFFh
3B8h	4	MAC_ADDRESS23_HIGH	0000FFFFh
3BCh	4	MAC_ADDRESS23_LOW	FFFFFFFFh
3C0h	4	MAC_ADDRESS24_HIGH	0000FFFFh
3C4h	4	MAC_ADDRESS24_LOW	FFFFFFFFh
3C8h	4	MAC_ADDRESS25_HIGH	0000FFFFh
3CCh	4	MAC_ADDRESS25_LOW	FFFFFFFFh
3D0h	4	MAC_ADDRESS26_HIGH	0000FFFFh
3D4h	4	MAC_ADDRESS26_LOW	FFFFFFFFh
3D8h	4	MAC_ADDRESS27_HIGH	0000FFFFh
3DCh	4	MAC_ADDRESS27_LOW	FFFFFFFFh
3E0h	4	MAC_ADDRESS28_HIGH	0000FFFFh
3E4h	4	MAC_ADDRESS28_LOW	FFFFFFFFh
3E8h	4	MAC_ADDRESS29_HIGH	0000FFFFh
3ECh	4	MAC_ADDRESS29_LOW	FFFFFFFFh
3F0h	4	MAC_ADDRESS30_HIGH	0000FFFFh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3F4h	4	MAC_ADDRESS30_LOW	FFFFFFFFh
3F8h	4	MAC_ADDRESS31_HIGH	0000FFFFh
3FCh	4	MAC_ADDRESS31_LOW	FFFFFFFFh
400h	4	MAC_ADDRESS32_HIGH	0000FFFFh
404h	4	MAC_ADDRESS32_LOW	FFFFFFFFh
408h	4	MAC_ADDRESS33_HIGH	0000FFFFh
40Ch	4	MAC_ADDRESS33_LOW	FFFFFFFFh
410h	4	MAC_ADDRESS34_HIGH	0000FFFFh
414h	4	MAC_ADDRESS34_LOW	FFFFFFFFh
418h	4	MAC_ADDRESS35_HIGH	0000FFFFh
41Ch	4	MAC_ADDRESS35_LOW	FFFFFFFFh
420h	4	MAC_ADDRESS36_HIGH	0000FFFFh
424h	4	MAC_ADDRESS36_LOW	FFFFFFFFh
428h	4	MAC_ADDRESS37_HIGH	0000FFFFh
42Ch	4	MAC_ADDRESS37_LOW	FFFFFFFFh
430h	4	MAC_ADDRESS38_HIGH	0000FFFFh
434h	4	MAC_ADDRESS38_LOW	FFFFFFFFh
438h	4	MAC_ADDRESS39_HIGH	0000FFFFh
43Ch	4	MAC_ADDRESS39_LOW	FFFFFFFFh
440h	4	MAC_ADDRESS40_HIGH	0000FFFFh
444h	4	MAC_ADDRESS40_LOW	FFFFFFFFh
448h	4	MAC_ADDRESS41_HIGH	0000FFFFh
44Ch	4	MAC_ADDRESS41_LOW	FFFFFFFFh
450h	4	MAC_ADDRESS42_HIGH	0000FFFFh
454h	4	MAC_ADDRESS42_LOW	FFFFFFFFh
458h	4	MAC_ADDRESS43_HIGH	0000FFFFh
45Ch	4	MAC_ADDRESS43_LOW	FFFFFFFFh
460h	4	MAC_ADDRESS44_HIGH	0000FFFFh
464h	4	MAC_ADDRESS44_LOW	FFFFFFFFh
468h	4	MAC_ADDRESS45_HIGH	0000FFFFh
46Ch	4	MAC_ADDRESS45_LOW	FFFFFFFFh
470h	4	MAC_ADDRESS46_HIGH	0000FFFFh
474h	4	MAC_ADDRESS46_LOW	FFFFFFFFh
478h	4	MAC_ADDRESS47_HIGH	0000FFFFh
47Ch	4	MAC_ADDRESS47_LOW	FFFFFFFFh
480h	4	MAC_ADDRESS48_HIGH	0000FFFFh
484h	4	MAC_ADDRESS48_LOW	FFFFFFFFh
488h	4	MAC_ADDRESS49_HIGH	0000FFFFh
48Ch	4	MAC_ADDRESS49_LOW	FFFFFFFFh
490h	4	MAC_ADDRESS50_HIGH	0000FFFFh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
494h	4	MAC_ADDRESS50_LOW	FFFFFFFFh
498h	4	MAC_ADDRESS51_HIGH	0000FFFFh
49Ch	4	MAC_ADDRESS51_LOW	FFFFFFFFh
4A0h	4	MAC_ADDRESS52_HIGH	0000FFFFh
4A4h	4	MAC_ADDRESS52_LOW	FFFFFFFFh
4A8h	4	MAC_ADDRESS53_HIGH	0000FFFFh
4ACh	4	MAC_ADDRESS53_LOW	FFFFFFFFh
4B0h	4	MAC_ADDRESS54_HIGH	0000FFFFh
4B4h	4	MAC_ADDRESS54_LOW	FFFFFFFFh
4B8h	4	MAC_ADDRESS55_HIGH	0000FFFFh
4BCh	4	MAC_ADDRESS55_LOW	FFFFFFFFh
4C0h	4	MAC_ADDRESS56_HIGH	0000FFFFh
4C4h	4	MAC_ADDRESS56_LOW	FFFFFFFFh
4C8h	4	MAC_ADDRESS57_HIGH	0000FFFFh
4CCh	4	MAC_ADDRESS57_LOW	FFFFFFFFh
4D0h	4	MAC_ADDRESS58_HIGH	0000FFFFh
4D4h	4	MAC_ADDRESS58_LOW	FFFFFFFFh
4D8h	4	MAC_ADDRESS59_HIGH	0000FFFFh
4DCh	4	MAC_ADDRESS59_LOW	FFFFFFFFh
4E0h	4	MAC_ADDRESS60_HIGH	0000FFFFh
4E4h	4	MAC_ADDRESS60_LOW	FFFFFFFFh
4E8h	4	MAC_ADDRESS61_HIGH	0000FFFFh
4ECh	4	MAC_ADDRESS61_LOW	FFFFFFFFh
4F0h	4	MAC_ADDRESS62_HIGH	0000FFFFh
4F4h	4	MAC_ADDRESS62_LOW	FFFFFFFFh
4F8h	4	MAC_ADDRESS63_HIGH	0000FFFFh
4FCh	4	MAC_ADDRESS63_LOW	FFFFFFFFh
700h	4	MMC_CONTROL	00000000h
704h	4	MMC_RX_INTERRUPT	00000000h
708h	4	MMC_TX_INTERRUPT	00000000h
70Ch	4	MMC_RX_INTERRUPT_MASK	00000000h
710h	4	MMC_TX_INTERRUPT_MASK	00000000h
714h	4	TX_OCTET_COUNT_GOOD_BAD	00000000h
718h	4	TX_PACKET_COUNT_GOOD_BAD	00000000h
71Ch	4	TX_BROADCAST_PACKETS_GOOD	00000000h
720h	4	TX_MULTICAST_PACKETS_GOOD	00000000h
724h	4	TX_64OCTETS_PACKETS_GOOD_BAD	00000000h
728h	4	TX_65TO127OCTETS_PACKETS_GOOD_BAD	00000000h
72Ch	4	TX_128TO255OCTETS_PACKETS_GOOD_BAD	00000000h
730h	4	TX_256TO511OCTETS_PACKETS_GOOD_BAD	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
734h	4	TX_512TO1023OCTETS_PACKETS_GOOD_BAD	00000000h
738h	4	TX_1024TOMAXOCTETS_PACKETS_GOOD_BAD	00000000h
73Ch	4	TX_UNICAST_PACKETS_GOOD_BAD	00000000h
740h	4	TX_MULTICAST_PACKETS_GOOD_BAD	00000000h
744h	4	TX_BROADCAST_PACKETS_GOOD_BAD	00000000h
748h	4	TX_UNDERFLOW_ERROR_PACKETS	00000000h
74Ch	4	TX_SINGLE_COLLISION_GOOD_PACKETS	00000000h
750h	4	TX_MULTIPLE_COLLISION_GOOD_PACKETS	00000000h
754h	4	TX_DEFERRED_PACKETS	00000000h
758h	4	TX_LATE_COLLISION_PACKETS	00000000h
75Ch	4	TX_EXCESSIVE_COLLISION_PACKETS	00000000h
760h	4	TX_CARRIER_ERROR_PACKETS	00000000h
764h	4	TX_OCTET_COUNT_GOOD	00000000h
768h	4	TX_PACKET_COUNT_GOOD	00000000h
76Ch	4	TX_EXCESSIVE_DEFERRAL_ERROR	00000000h
770h	4	TX_PAUSE_PACKETS	00000000h
774h	4	TX_VLAN_PACKETS_GOOD	00000000h
778h	4	TX_OSIZE_PACKETS_GOOD	00000000h
780h	4	RX_PACKETS_COUNT_GOOD_BAD	00000000h
784h	4	RX_OCTET_COUNT_GOOD_BAD	00000000h
788h	4	RX_OCTET_COUNT_GOOD	00000000h
78Ch	4	RX_BROADCAST_PACKETS_GOOD	00000000h
790h	4	RX_MULTICAST_PACKETS_GOOD	00000000h
794h	4	RX_CRC_ERROR_PACKETS	00000000h
798h	4	RX_ALIGNMENT_ERROR_PACKETS	00000000h
79Ch	4	RX_RUNT_ERROR_PACKETS	00000000h
7A0h	4	RX_JABBER_ERROR_PACKETS	00000000h
7A4h	4	RX_UNDERSIZE_PACKETS_GOOD	00000000h
7A8h	4	RX_OVERSIZE_PACKETS_GOOD	00000000h
7ACh	4	RX_64OCTETS_PACKETS_GOOD_BAD	00000000h
7B0h	4	RX_65TO127OCTETS_PACKETS_GOOD_BAD	00000000h
7B4h	4	RX_128TO255OCTETS_PACKETS_GOOD_BAD	00000000h
7B8h	4	RX_256TO511OCTETS_PACKETS_GOOD_BAD	00000000h
7BCh	4	RX_512TO1023OCTETS_PACKETS_GOOD_BAD	00000000h
7C0h	4	RX_1024TOMAXOCTETS_PACKETS_GOOD_BAD	00000000h
7C4h	4	RX_UNICAST_PACKETS_GOOD	00000000h
7C8h	4	RX_LENGTH_ERROR_PACKETS	00000000h
7CCh	4	RX_OUT_OF_RANGE_TYPE_PACKETS	00000000h
7D0h	4	RX_PAUSE_PACKETS	00000000h
7D4h	4	RX_FIFO_OVERFLOW_PACKETS	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
7D8h	4	RX_VLAN_PACKETS_GOOD_BAD	00000000h
7DCh	4	RX_WATCHDOG_ERROR_PACKETS	00000000h
7E0h	4	RX_RECEIVE_ERROR_PACKETS	00000000h
7E4h	4	RX_CONTROL_PACKETS_GOOD	00000000h
7ECh	4	TX_LPI_USEC_CNTR	00000000h
7F0h	4	TX_LPI_TRAN_CNTR	00000000h
7F4h	4	RX_LPI_USEC_CNTR	00000000h
7F8h	4	RX_LPI_TRAN_CNTR	00000000h
800h	4	MMC_IPC_RX_INTERRUPT_MASK	00000000h
808h	4	MMC_IPC_RX_INTERRUPT	00000000h
810h	4	RXIPV4_GOOD_PACKETS	00000000h
814h	4	RXIPV4_HEADER_ERROR_PACKETS	00000000h
818h	4	RXIPV4_NO_PAYLOAD_PACKETS	00000000h
81Ch	4	RXIPV4_FRAGMENTED_PACKETS	00000000h
820h	4	RXIPV4_UDP_CHECKSUM_DISABLED_PACKETS	00000000h
824h	4	RXIPV6_GOOD_PACKETS	00000000h
828h	4	RXIPV6_HEADER_ERROR_PACKETS	00000000h
82Ch	4	RXIPV6_NO_PAYLOAD_PACKETS	00000000h
830h	4	RXUDP_GOOD_PACKETS	00000000h
834h	4	RXUDP_ERROR_PACKETS	00000000h
838h	4	RXTCP_GOOD_PACKETS	00000000h
83Ch	4	RXTCP_ERROR_PACKETS	00000000h
840h	4	RXICMP_GOOD_PACKETS	00000000h
844h	4	RXICMP_ERROR_PACKETS	00000000h
850h	4	RXIPV4_GOOD_OCTETS	00000000h
854h	4	RXIPV4_HEADER_ERROR_OCTETS	00000000h
858h	4	RXIPV4_NO_PAYLOAD_OCTETS	00000000h
85Ch	4	RXIPV4_FRAGMENTED_OCTETS	00000000h
860h	4	RXIPV4_UDP_CHECKSUM_DISABLE_OCTETS	00000000h
864h	4	RXIPV6_GOOD_OCTETS	00000000h
868h	4	RXIPV6_HEADER_ERROR_OCTETS	00000000h
86Ch	4	RXIPV6_NO_PAYLOAD_OCTETS	00000000h
870h	4	RXUDP_GOOD_OCTETS	00000000h
874h	4	RXUDP_ERROR_OCTETS	00000000h
878h	4	RXTCP_GOOD_OCTETS	00000000h
87Ch	4	RXTCP_ERROR_OCTETS	00000000h
880h	4	RXICMP_GOOD_OCTETS	00000000h
884h	4	RXICMP_ERROR_OCTETS	00000000h
8A0h	4	MMC_FPE_TX_INTERRUPT	00000000h
8A4h	4	MMC_FPE_TX_INTERRUPT_MASK	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8A8h	4	MMC_TX_FPE_FRAGMENT_CNTR	00000000h
8ACh	4	MMC_TX_HOLD_REQ_CNTR	00000000h
8C0h	4	MMC_FPE_RX_INTERRUPT	00000000h
8C4h	4	MMC_FPE_RX_INTERRUPT_MASK	00000000h
8C8h	4	MMC_RX_PACKET_ASSEMBLY_ERR_CNTR	00000000h
8CCh	4	MMC_RX_PACKET_SMD_ERR_CNTR	00000000h
8D0h	4	MMC_RX_PACKET_ASSEMBLY_OK_CNTR	00000000h
8D4h	4	MMC_RX_FPE_FRAGMENT_CNTR	00000000h
900h	4	MAC_L3_L4_CONTROL0	00000000h
904h	4	MAC_LAYER4_ADDRESS0	00000000h
910h	4	MAC_LAYER3_ADDR0_REG0	00000000h
914h	4	MAC_LAYER3_ADDR1_REG0	00000000h
918h	4	MAC_LAYER3_ADDR2_REG0	00000000h
91Ch	4	MAC_LAYER3_ADDR3_REG0	00000000h
930h	4	MAC_L3_L4_CONTROL1	00000000h
934h	4	MAC_LAYER4_ADDRESS1	00000000h
940h	4	MAC_LAYER3_ADDR0_REG1	00000000h
944h	4	MAC_LAYER3_ADDR1_REG1	00000000h
948h	4	MAC_LAYER3_ADDR2_REG1	00000000h
94Ch	4	MAC_LAYER3_ADDR3_REG1	00000000h
B00h	4	MAC_TIMESTAMP_CONTROL	00002000h
B04h	4	MAC_SUB_SECOND_INCREMENT	00000000h
B08h	4	MAC_SYSTEM_TIME_SECONDS	00000000h
B0Ch	4	MAC_SYSTEM_TIME_NANOSECONDS	00000000h
B10h	4	MAC_SYSTEM_TIME_SECONDS_UPDATE	00000000h
B14h	4	MAC_SYSTEM_TIME_NANOSECONDS_UPDATE	00000000h
B18h	4	MAC_TIMESTAMP_ADDEND	00000000h
B1Ch	4	MAC_SYSTEM_TIME_HIGHER_WORD_SECONDS	00000000h
B20h	4	MAC_TIMESTAMP_STATUS	00000000h
B30h	4	MAC_TX_TIMESTAMP_STATUS_NANOSECONDS	00000000h
B34h	4	MAC_TX_TIMESTAMP_STATUS_SECONDS	00000000h
B40h	4	MAC_AUXILIARY_CONTROL	00000000h
B48h	4	MAC_AUXILIARY_TIMESTAMP_NANOSECONDS	00000000h
B4Ch	4	MAC_AUXILIARY_TIMESTAMP_SECONDS	00000000h
B50h	4	MAC_TIMESTAMP_INGRESS_ASYM_CORR	00000000h
B54h	4	MAC_TIMESTAMP_EGRESS_ASYM_CORR	00000000h
B58h	4	MAC_TIMESTAMP_INGRESS_CORR_NANOSECOND	00000000h
B5Ch	4	MAC_TIMESTAMP_EGRESS_CORR_NANOSECOND	00000000h
B60h	4	MAC_TIMESTAMP_INGRESS_CORR_SUBNANOSEC	00000000h
B64h	4	MAC_TIMESTAMP_EGRESS_CORR_SUBNANOSEC	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
B68h	4	MAC_TIMESTAMP_INGRESS_LATENCY	00000000h
B6Ch	4	MAC_TIMESTAMP_EGRESS_LATENCY	00000000h
B70h	4	MAC_PPS_CONTROL	00000000h
B80h	4	MAC_PPS0_TARGET_TIME_SECONDS	00000000h
B84h	4	MAC_PPS0_TARGET_TIME_NANOSECONDS	00000000h
B88h	4	MAC_PPS0_INTERVAL	00000000h
B8Ch	4	MAC_PPS0_WIDTH	00000000h
B90h	4	MAC_PPS1_TARGET_TIME_SECONDS	00000000h
B94h	4	MAC_PPS1_TARGET_TIME_NANOSECONDS	00000000h
B98h	4	MAC_PPS1_INTERVAL	00000000h
B9Ch	4	MAC_PPS1_WIDTH	00000000h
BC0h	4	MAC_PTO_CONTROL	00000000h
BC4h	4	MAC_SOURCE_PORT_IDENTITY0	00000000h
BC8h	4	MAC_SOURCE_PORT_IDENTITY1	00000000h
BCCh	4	MAC_SOURCE_PORT_IDENTITY2	00000000h
BD0h	4	MAC_LOG_MESSAGE_INTERVAL	00000000h
C00h	4	MTL_OPERATION_MODE	00000000h
C08h	4	MTL_DBG_CTL	00000000h
C0Ch	4	MTL_DBG_STS	00000018h
C10h	4	MTL_FIFO_DEBUG_DATA	00000000h
C20h	4	MTL_INTERRUPT_STATUS	00000000h
C30h	4	MTL_RXQ_DMA_MAP0	00000000h
C34h	4	MTL_RXQ_DMA_MAP1	00000000h
C40h	4	MTL_TBS_CTRL	00000000h
C50h	4	MTL_EST_CONTROL	00000000h
C58h	4	MTL_EST_STATUS	00000000h
C60h	4	MTL_EST_SCH_ERROR	00000000h
C64h	4	MTL_EST_FRM_SIZE_ERROR	00000000h
C68h	4	MTL_EST_FRM_SIZE_CAPTURE	00000000h
C70h	4	MTL_EST_INTR_ENABLE	00000000h
C80h	4	MTL_EST_GCL_CONTROL	00000000h
C84h	4	MTL_EST_GCL_DATA	00000000h
C90h	4	MTL_FPE_CTRL_STS	00000000h
C94h	4	MTL_FPE_ADVANCE	00000000h
CA0h	4	MTL_RXP_CONTROL_STATUS	80FF00FFh
CA4h	4	MTL_RXP_INTERRUPT_CONTROL_STATUS	00000000h
CA8h	4	MTL_RXP_DROP_CNT	00000000h
CACh	4	MTL_RXP_ERROR_CNT	00000000h
CB0h	4	MTL_RXP_INDIRECT_ACC_CONTROL_STATUS	00000000h
CB4h	4	MTL_RXP_INDIRECT_ACC_DATA	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
CC0h	4	MTL_ECC_CONTROL	00000000h
CC4h	4	MTL_SAFETY_INTERRUPT_STATUS	00000000h
CC8h	4	MTL_ECC_INTERRUPT_ENABLE	00000000h
CCCh	4	MTL_ECC_INTERRUPT_STATUS	00000000h
CD0h	4	MTL_ECC_ERR_STS_RCTL	00000000h
CD4h	4	MTL_ECC_ERR_ADDR_STATUS	00000000h
CD8h	4	MTL_ECC_ERR_CNTR_STATUS	00000000h
CE0h	4	MTL_DPP_CONTROL	00000000h
D00h	4	MTL_TXQ0_OPERATION_MODE	00000000h
D04h	4	MTL_TXQ0_UNDERFLOW	00000000h
D08h	4	MTL_TXQ0_DEBUG	00000000h
D14h	4	MTL_TXQ0_ETS_STATUS	00000000h
D18h	4	MTL_TXQ0_QUANTUM_WEIGHT	00000000h
D2Ch	4	MTL_Q0_INTERRUPT_CONTROL_STATUS	00000000h
D30h	4	MTL_RXQ0_OPERATION_MODE	00000000h
D34h	4	MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT	00000000h
D38h	4	MTL_RXQ0_DEBUG	00000000h
D3Ch	4	MTL_RXQ0_CONTROL	00000000h
D40h	4	MTL_TXQ1_OPERATION_MODE	00000000h
D44h	4	MTL_TXQ1_UNDERFLOW	00000000h
D48h	4	MTL_TXQ1_DEBUG	00000000h
D50h	4	MTL_TXQ1_ETS_CONTROL	00000000h
D54h	4	MTL_TXQ1_ETS_STATUS	00000000h
D58h	4	MTL_TXQ1_QUANTUM_WEIGHT	00000000h
D5Ch	4	MTL_TXQ1_SENDSLOPECREDIT	00000000h
D60h	4	MTL_TXQ1_HICREDIT	00000000h
D64h	4	MTL_TXQ1_LOCREDIT	00000000h
D6Ch	4	MTL_Q1_INTERRUPT_CONTROL_STATUS	00000000h
D70h	4	MTL_RXQ1_OPERATION_MODE	00000000h
D74h	4	MTL_RXQ1_MISSED_PACKET_OVERFLOW_CNT	00000000h
D78h	4	MTL_RXQ1_DEBUG	00000000h
D7Ch	4	MTL_RXQ1_CONTROL	00000000h
D80h	4	MTL_TXQ2_OPERATION_MODE	00000000h
D84h	4	MTL_TXQ2_UNDERFLOW	00000000h
D88h	4	MTL_TXQ2_DEBUG	00000000h
D90h	4	MTL_TXQ2_ETS_CONTROL	00000000h
D94h	4	MTL_TXQ2_ETS_STATUS	00000000h
D98h	4	MTL_TXQ2_QUANTUM_WEIGHT	00000000h
D9Ch	4	MTL_TXQ2_SENDSLOPECREDIT	00000000h
DA0h	4	MTL_TXQ2_HICREDIT	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
DA4h	4	MTL_TXQ2_LOCREDIT	00000000h
DACh	4	MTL_Q2_INTERRUPT_CONTROL_STATUS	00000000h
DB0h	4	MTL_RXQ2_OPERATION_MODE	00000000h
DB4h	4	MTL_RXQ2_MISSED_PACKET_OVERFLOW_CNT	00000000h
DB8h	4	MTL_RXQ2_DEBUG	00000000h
DBCh	4	MTL_RXQ2_CONTROL	00000000h
DC0h	4	MTL_TXQ3_OPERATION_MODE	00000000h
DC4h	4	MTL_TXQ3_UNDERFLOW	00000000h
DC8h	4	MTL_TXQ3_DEBUG	00000000h
DD0h	4	MTL_TXQ3_ETS_CONTROL	00000000h
DD4h	4	MTL_TXQ3_ETS_STATUS	00000000h
DD8h	4	MTL_TXQ3_QUANTUM_WEIGHT	00000000h
DDCh	4	MTL_TXQ3_SENDSLOPECREDIT	00000000h
DE0h	4	MTL_TXQ3_HICREDIT	00000000h
DE4h	4	MTL_TXQ3_LOCREDIT	00000000h
DECh	4	MTL_Q3_INTERRUPT_CONTROL_STATUS	00000000h
DF0h	4	MTL_RXQ3_OPERATION_MODE	00000000h
DF4h	4	MTL_RXQ3_MISSED_PACKET_OVERFLOW_CNT	00000000h
DF8h	4	MTL_RXQ3_DEBUG	00000000h
DFCh	4	MTL_RXQ3_CONTROL	00000000h
E00h	4	MTL_TXQ4_OPERATION_MODE	00000000h
E04h	4	MTL_TXQ4_UNDERFLOW	00000000h
E08h	4	MTL_TXQ4_DEBUG	00000000h
E10h	4	MTL_TXQ4_ETS_CONTROL	00000000h
E14h	4	MTL_TXQ4_ETS_STATUS	00000000h
E18h	4	MTL_TXQ4_QUANTUM_WEIGHT	00000000h
E1Ch	4	MTL_TXQ4_SENDSLOPECREDIT	00000000h
E20h	4	MTL_TXQ4_HICREDIT	00000000h
E24h	4	MTL_TXQ4_LOCREDIT	00000000h
E2Ch	4	MTL_Q4_INTERRUPT_CONTROL_STATUS	00000000h
E30h	4	MTL_RXQ4_OPERATION_MODE	00000000h
E34h	4	MTL_RXQ4_MISSED_PACKET_OVERFLOW_CNT	00000000h
E38h	4	MTL_RXQ4_DEBUG	00000000h
E3Ch	4	MTL_RXQ4_CONTROL	00000000h
E40h	4	MTL_TXQ5_OPERATION_MODE	00000000h
E44h	4	MTL_TXQ5_UNDERFLOW	00000000h
E48h	4	MTL_TXQ5_DEBUG	00000000h
E50h	4	MTL_TXQ5_ETS_CONTROL	00000000h
E54h	4	MTL_TXQ5_ETS_STATUS	00000000h
E58h	4	MTL_TXQ5_QUANTUM_WEIGHT	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
E5Ch	4	MTL_TXQ5_SENDSLOPECREDIT	00000000h
E60h	4	MTL_TXQ5_HICREDIT	00000000h
E64h	4	MTL_TXQ5_LOCREDIT	00000000h
E6Ch	4	MTL_Q5_INTERRUPT_CONTROL_STATUS	00000000h
E70h	4	MTL_RXQ5_OPERATION_MODE	00000000h
E74h	4	MTL_RXQ5_MISSED_PACKET_OVERFLOW_CNT	00000000h
E78h	4	MTL_RXQ5_DEBUG	00000000h
E7Ch	4	MTL_RXQ5_CONTROL	00000000h
E80h	4	MTL_TXQ6_OPERATION_MODE	00000000h
E84h	4	MTL_TXQ6_UNDERFLOW	00000000h
E88h	4	MTL_TXQ6_DEBUG	00000000h
E90h	4	MTL_TXQ6_ETS_CONTROL	00000000h
E94h	4	MTL_TXQ6_ETS_STATUS	00000000h
E98h	4	MTL_TXQ6_QUANTUM_WEIGHT	00000000h
E9Ch	4	MTL_TXQ6_SENDSLOPECREDIT	00000000h
EA0h	4	MTL_TXQ6_HICREDIT	00000000h
EA4h	4	MTL_TXQ6_LOCREDIT	00000000h
EACh	4	MTL_Q6_INTERRUPT_CONTROL_STATUS	00000000h
EB0h	4	MTL_RXQ6_OPERATION_MODE	00000000h
EB4h	4	MTL_RXQ6_MISSED_PACKET_OVERFLOW_CNT	00000000h
EB8h	4	MTL_RXQ6_DEBUG	00000000h
EBCh	4	MTL_RXQ6_CONTROL	00000000h
EC0h	4	MTL_TXQ7_OPERATION_MODE	00000000h
EC4h	4	MTL_TXQ7_UNDERFLOW	00000000h
EC8h	4	MTL_TXQ7_DEBUG	00000000h
ED0h	4	MTL_TXQ7_ETS_CONTROL	00000000h
ED4h	4	MTL_TXQ7_ETS_STATUS	00000000h
ED8h	4	MTL_TXQ7_QUANTUM_WEIGHT	00000000h
EDCh	4	MTL_TXQ7_SENDSLOPECREDIT	00000000h
EE0h	4	MTL_TXQ7_HICREDIT	00000000h
EE4h	4	MTL_TXQ7_LOCREDIT	00000000h
EECh	4	MTL_Q7_INTERRUPT_CONTROL_STATUS	00000000h
EF0h	4	MTL_RXQ7_OPERATION_MODE	00000000h
EF4h	4	MTL_RXQ7_MISSED_PACKET_OVERFLOW_CNT	00000000h
EF8h	4	MTL_RXQ7_DEBUG	00000000h
EFCh	4	MTL_RXQ7_CONTROL	00000000h
1000h	4	DMA_MODE	00000000h
1004h	4	DMA_SYSBUS_MODE	01010000h
1008h	4	DMA_INTERRUPT_STATUS	00000000h
100Ch	4	DMA_DEBUG_STATUS0	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1010h	4	DMA_DEBUG_STATUS1	00000000h
1014h	4	DMA_DEBUG_STATUS2	00000000h
1020h	4	AXI4_TX_AR_ACE_CONTROL	00000000h
1024h	4	AXI4_RX_AW_ACE_CONTROL	00000000h
1028h	4	AXI4_TXRX_AWAR_ACE_CONTROL	00000000h
1040h	4	AXI_LPI_ENTRY_INTERVAL	00000000h
1050h	4	DMA_TBS_CTRL0	00000000h
1054h	4	DMA_TBS_CTRL1	00000000h
1058h	4	DMA_TBS_CTRL2	00000000h
105Ch	4	DMA_TBS_CTRL3	00000000h
1080h	4	DMA_SAFETY_INTERRUPT_STATUS	00000000h
1084h	4	DMA_ECC_INTERRUPT_ENABLE	00000000h
1088h	4	DMA_ECC_INTERRUPT_STATUS	00000000h
1100h	4	DMA_CH0_CONTROL	00000000h
1104h	4	DMA_CH0_TX_CONTROL	00000000h
1108h	4	DMA_CH0_RX_CONTROL	00000000h
1110h	4	DMA_CH0_TXDESC_LIST_HADDRESS	00000000h
1114h	4	DMA_CH0_TXDESC_LIST_ADDRESS	00000000h
1118h	4	DMA_CH0_RXDESC_LIST_HADDRESS	00000000h
111Ch	4	DMA_CH0_RXDESC_LIST_ADDRESS	00000000h
1120h	4	DMA_CH0_TXDESC_TAIL_POINTER	00000000h
1128h	4	DMA_CH0_RXDESC_TAIL_POINTER	00000000h
112Ch	4	DMA_CH0_TXDESC_RING_LENGTH	00000000h
1130h	4	DMA_CH0_RXDESC_RING_LENGTH	00000000h
1134h	4	DMA_CH0_INTERRUPT_ENABLE	00000000h
1138h	4	DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
113Ch	4	DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
1144h	4	DMA_CH0_CURRENT_APP_TXDESC	00000000h
114Ch	4	DMA_CH0_CURRENT_APP_RXDESC	00000000h
1150h	4	DMA_CH0_CURRENT_APP_TXBUFFER_H	00000000h
1154h	4	DMA_CH0_CURRENT_APP_TXBUFFER	00000000h
1158h	4	DMA_CH0_CURRENT_APP_RXBUFFER_H	00000000h
115Ch	4	DMA_CH0_CURRENT_APP_RXBUFFER	00000000h
1160h	4	DMA_CH0_STATUS	00000000h
1164h	4	DMA_CH0_MISS_FRAME_CNT	00000000h
1168h	4	DMA_CH0_RXP_ACCEPT_CNT	00000000h
116Ch	4	DMA_CH0_RX_ERI_CNT	00000000h
1180h	4	DMA_CH1_CONTROL	00000000h
1184h	4	DMA_CH1_TX_CONTROL	00000000h
1188h	4	DMA_CH1_RX_CONTROL	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1190h	4	DMA_CH1_TXDESC_LIST_HADDRESS	00000000h
1194h	4	DMA_CH1_TXDESC_LIST_ADDRESS	00000000h
1198h	4	DMA_CH1_RXDESC_LIST_HADDRESS	00000000h
119Ch	4	DMA_CH1_RXDESC_LIST_ADDRESS	00000000h
11A0h	4	DMA_CH1_TXDESC_TAIL_POINTER	00000000h
11A8h	4	DMA_CH1_RXDESC_TAIL_POINTER	00000000h
11ACh	4	DMA_CH1_TXDESC_RING_LENGTH	00000000h
11B0h	4	DMA_CH1_RXDESC_RING_LENGTH	00000000h
11B4h	4	DMA_CH1_INTERRUPT_ENABLE	00000000h
11B8h	4	DMA_CH1_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
11BCh	4	DMA_CH1_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
11C4h	4	DMA_CH1_CURRENT_APP_TXDESC	00000000h
11CCh	4	DMA_CH1_CURRENT_APP_RXDESC	00000000h
11D0h	4	DMA_CH1_CURRENT_APP_TXBUFFER_H	00000000h
11D4h	4	DMA_CH1_CURRENT_APP_TXBUFFER	00000000h
11D8h	4	DMA_CH1_CURRENT_APP_RXBUFFER_H	00000000h
11DCh	4	DMA_CH1_CURRENT_APP_RXBUFFER	00000000h
11E0h	4	DMA_CH1_STATUS	00000000h
11E4h	4	DMA_CH1_MISS_FRAME_CNT	00000000h
11E8h	4	DMA_CH1_RXP_ACCEPT_CNT	00000000h
11ECh	4	DMA_CH1_RX_ERI_CNT	00000000h
1200h	4	DMA_CH2_CONTROL	00000000h
1204h	4	DMA_CH2_TX_CONTROL	00000000h
1208h	4	DMA_CH2_RX_CONTROL	00000000h
1210h	4	DMA_CH2_TXDESC_LIST_HADDRESS	00000000h
1214h	4	DMA_CH2_TXDESC_LIST_ADDRESS	00000000h
1218h	4	DMA_CH2_RXDESC_LIST_HADDRESS	00000000h
121Ch	4	DMA_CH2_RXDESC_LIST_ADDRESS	00000000h
1220h	4	DMA_CH2_TXDESC_TAIL_POINTER	00000000h
1228h	4	DMA_CH2_RXDESC_TAIL_POINTER	00000000h
122Ch	4	DMA_CH2_TXDESC_RING_LENGTH	00000000h
1230h	4	DMA_CH2_RXDESC_RING_LENGTH	00000000h
1234h	4	DMA_CH2_INTERRUPT_ENABLE	00000000h
1238h	4	DMA_CH2_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
123Ch	4	DMA_CH2_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
1244h	4	DMA_CH2_CURRENT_APP_TXDESC	00000000h
124Ch	4	DMA_CH2_CURRENT_APP_RXDESC	00000000h
1250h	4	DMA_CH2_CURRENT_APP_TXBUFFER_H	00000000h
1254h	4	DMA_CH2_CURRENT_APP_TXBUFFER	00000000h
1258h	4	DMA_CH2_CURRENT_APP_RXBUFFER_H	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
125Ch	4	DMA_CH2_CURRENT_APP_RXBUFFER	00000000h
1260h	4	DMA_CH2_STATUS	00000000h
1264h	4	DMA_CH2_MISS_FRAME_CNT	00000000h
1268h	4	DMA_CH2_RXP_ACCEPT_CNT	00000000h
126Ch	4	DMA_CH2_RX_ERI_CNT	00000000h
1280h	4	DMA_CH3_CONTROL	00000000h
1284h	4	DMA_CH3_TX_CONTROL	00000000h
1288h	4	DMA_CH3_RX_CONTROL	00000000h
1290h	4	DMA_CH3_TXDESC_LIST_HADDRESS	00000000h
1294h	4	DMA_CH3_TXDESC_LIST_ADDRESS	00000000h
1298h	4	DMA_CH3_RXDESC_LIST_HADDRESS	00000000h
129Ch	4	DMA_CH3_RXDESC_LIST_ADDRESS	00000000h
12A0h	4	DMA_CH3_TXDESC_TAIL_POINTER	00000000h
12A8h	4	DMA_CH3_RXDESC_TAIL_POINTER	00000000h
12ACh	4	DMA_CH3_TXDESC_RING_LENGTH	00000000h
12B0h	4	DMA_CH3_RXDESC_RING_LENGTH	00000000h
12B4h	4	DMA_CH3_INTERRUPT_ENABLE	00000000h
12B8h	4	DMA_CH3_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
12BCh	4	DMA_CH3_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
12C4h	4	DMA_CH3_CURRENT_APP_TXDESC	00000000h
12CCh	4	DMA_CH3_CURRENT_APP_RXDESC	00000000h
12D0h	4	DMA_CH3_CURRENT_APP_TXBUFFER_H	00000000h
12D4h	4	DMA_CH3_CURRENT_APP_TXBUFFER	00000000h
12D8h	4	DMA_CH3_CURRENT_APP_RXBUFFER_H	00000000h
12DCh	4	DMA_CH3_CURRENT_APP_RXBUFFER	00000000h
12E0h	4	DMA_CH3_STATUS	00000000h
12E4h	4	DMA_CH3_MISS_FRAME_CNT	00000000h
12E8h	4	DMA_CH3_RXP_ACCEPT_CNT	00000000h
12ECh	4	DMA_CH3_RX_ERI_CNT	00000000h
1300h	4	DMA_CH4_CONTROL	00000000h
1304h	4	DMA_CH4_TX_CONTROL	00000000h
1308h	4	DMA_CH4_RX_CONTROL	00000000h
1310h	4	DMA_CH4_TXDESC_LIST_HADDRESS	00000000h
1314h	4	DMA_CH4_TXDESC_LIST_ADDRESS	00000000h
1318h	4	DMA_CH4_RXDESC_LIST_HADDRESS	00000000h
131Ch	4	DMA_CH4_RXDESC_LIST_ADDRESS	00000000h
1320h	4	DMA_CH4_TXDESC_TAIL_POINTER	00000000h
1328h	4	DMA_CH4_RXDESC_TAIL_POINTER	00000000h
132Ch	4	DMA_CH4_TXDESC_RING_LENGTH	00000000h
1330h	4	DMA_CH4_RXDESC_RING_LENGTH	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1334h	4	DMA_CH4_INTERRUPT_ENABLE	00000000h
1338h	4	DMA_CH4_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
133Ch	4	DMA_CH4_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
1344h	4	DMA_CH4_CURRENT_APP_TXDESC	00000000h
134Ch	4	DMA_CH4_CURRENT_APP_RXDESC	00000000h
1350h	4	DMA_CH4_CURRENT_APP_TXBUFFER_H	00000000h
1354h	4	DMA_CH4_CURRENT_APP_TXBUFFER	00000000h
1358h	4	DMA_CH4_CURRENT_APP_RXBUFFER_H	00000000h
135Ch	4	DMA_CH4_CURRENT_APP_RXBUFFER	00000000h
1360h	4	DMA_CH4_STATUS	00000000h
1364h	4	DMA_CH4_MISS_FRAME_CNT	00000000h
1368h	4	DMA_CH4_RXP_ACCEPT_CNT	00000000h
136Ch	4	DMA_CH4_RX_ERI_CNT	00000000h
1380h	4	DMA_CH5_CONTROL	00000000h
1384h	4	DMA_CH5_TX_CONTROL	00000000h
1388h	4	DMA_CH5_RX_CONTROL	00000000h
1390h	4	DMA_CH5_TXDESC_LIST_HADDRESS	00000000h
1394h	4	DMA_CH5_TXDESC_LIST_ADDRESS	00000000h
1398h	4	DMA_CH5_RXDESC_LIST_HADDRESS	00000000h
139Ch	4	DMA_CH5_RXDESC_LIST_ADDRESS	00000000h
13A0h	4	DMA_CH5_TXDESC_TAIL_POINTER	00000000h
13A8h	4	DMA_CH5_RXDESC_TAIL_POINTER	00000000h
13ACh	4	DMA_CH5_TXDESC_RING_LENGTH	00000000h
13B0h	4	DMA_CH5_RXDESC_RING_LENGTH	00000000h
13B4h	4	DMA_CH5_INTERRUPT_ENABLE	00000000h
13B8h	4	DMA_CH5_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
13BCh	4	DMA_CH5_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
13C4h	4	DMA_CH5_CURRENT_APP_TXDESC	00000000h
13CCh	4	DMA_CH5_CURRENT_APP_RXDESC	00000000h
13D0h	4	DMA_CH5_CURRENT_APP_TXBUFFER_H	00000000h
13D4h	4	DMA_CH5_CURRENT_APP_TXBUFFER	00000000h
13D8h	4	DMA_CH5_CURRENT_APP_RXBUFFER_H	00000000h
13DCh	4	DMA_CH5_CURRENT_APP_RXBUFFER	00000000h
13E0h	4	DMA_CH5_STATUS	00000000h
13E4h	4	DMA_CH5_MISS_FRAME_CNT	00000000h
13E8h	4	DMA_CH5_RXP_ACCEPT_CNT	00000000h
13ECh	4	DMA_CH5_RX_ERI_CNT	00000000h
1400h	4	DMA_CH6_CONTROL	00000000h
1404h	4	DMA_CH6_TX_CONTROL	00000000h
1408h	4	DMA_CH6_RX_CONTROL	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1410h	4	DMA_CH6_TXDESC_LIST_HADDRESS	00000000h
1414h	4	DMA_CH6_TXDESC_LIST_ADDRESS	00000000h
1418h	4	DMA_CH6_RXDESC_LIST_HADDRESS	00000000h
141Ch	4	DMA_CH6_RXDESC_LIST_ADDRESS	00000000h
1420h	4	DMA_CH6_TXDESC_TAIL_POINTER	00000000h
1428h	4	DMA_CH6_RXDESC_TAIL_POINTER	00000000h
142Ch	4	DMA_CH6_TXDESC_RING_LENGTH	00000000h
1430h	4	DMA_CH6_RXDESC_RING_LENGTH	00000000h
1434h	4	DMA_CH6_INTERRUPT_ENABLE	00000000h
1438h	4	DMA_CH6_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
143Ch	4	DMA_CH6_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
1444h	4	DMA_CH6_CURRENT_APP_TXDESC	00000000h
144Ch	4	DMA_CH6_CURRENT_APP_RXDESC	00000000h
1450h	4	DMA_CH6_CURRENT_APP_TXBUFFER_H	00000000h
1454h	4	DMA_CH6_CURRENT_APP_TXBUFFER	00000000h
1458h	4	DMA_CH6_CURRENT_APP_RXBUFFER_H	00000000h
145Ch	4	DMA_CH6_CURRENT_APP_RXBUFFER	00000000h
1460h	4	DMA_CH6_STATUS	00000000h
1464h	4	DMA_CH6_MISS_FRAME_CNT	00000000h
1468h	4	DMA_CH6_RXP_ACCEPT_CNT	00000000h
146Ch	4	DMA_CH6_RX_ERI_CNT	00000000h
1480h	4	DMA_CH7_CONTROL	00000000h
1484h	4	DMA_CH7_TX_CONTROL	00000000h
1488h	4	DMA_CH7_RX_CONTROL	00000000h
1490h	4	DMA_CH7_TXDESC_LIST_HADDRESS	00000000h
1494h	4	DMA_CH7_TXDESC_LIST_ADDRESS	00000000h
1498h	4	DMA_CH7_RXDESC_LIST_HADDRESS	00000000h
149Ch	4	DMA_CH7_RXDESC_LIST_ADDRESS	00000000h
14A0h	4	DMA_CH7_TXDESC_TAIL_POINTER	00000000h
14A8h	4	DMA_CH7_RXDESC_TAIL_POINTER	00000000h
14ACh	4	DMA_CH7_TXDESC_RING_LENGTH	00000000h
14B0h	4	DMA_CH7_RXDESC_RING_LENGTH	00000000h
14B4h	4	DMA_CH7_INTERRUPT_ENABLE	00000000h
14B8h	4	DMA_CH7_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
14BCh	4	DMA_CH7_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
14C4h	4	DMA_CH7_CURRENT_APP_TXDESC	00000000h
14CCh	4	DMA_CH7_CURRENT_APP_RXDESC	00000000h
14D0h	4	DMA_CH7_CURRENT_APP_TXBUFFER_H	00000000h
14D4h	4	DMA_CH7_CURRENT_APP_TXBUFFER	00000000h
14D8h	4	DMA_CH7_CURRENT_APP_RXBUFFER_H	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
14DCh	4	DMA_CH7_CURRENT_APP_RXBUFFER	00000000h
14E0h	4	DMA_CH7_STATUS	00000000h
14E4h	4	DMA_CH7_MISS_FRAME_CNT	00000000h
14E8h	4	DMA_CH7_RXP_ACCEPT_CNT	00000000h
14ECh	4	DMA_CH7_RX_ERI_CNT	00000000h

10.2.1 MAC_CONFIGURATION — Offset 0h

The MAC Configuration Register establishes the operating mode of the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ARP Offload Enable (ARPEN):** When this bit is set, the MAC can recognize an incoming ARP request packet and schedules the ARP packet for transmission. It forwards the ARP packet to the application and also indicate the events in the RxStatus. When this bit is reset, the MAC receiver does not recognize any ARP packet and indicates them as Type frame in the RxStatus. This bit is available only when the Enable IPv4 ARP Offload is selected. 0x0 (DISABLE): ARP Offload is disabled. 0x1 (ENABLE): ARP Offload is enabled.
30:28	0h RW	**Source Address Insertion or Replacement Control (SARC):** This field controls the source address insertion or replacement for all transmitted packets. Bit 30 specifies which MAC Address register (0 or 1) is used for source address insertion or replacement based on the values of Bits[29:28]: 2'b0x: - The mti_sa_ctrl_i and ati_sa_ctrl_i input signals control the SA field generation. 2'b10: - If Bit 30 is set to 0, the MAC inserts the content of the MAC Address 0 registers in the SA field of all transmitted packets. - If Bit 30 is set to 1 and the Enable MAC Address Register 1 option is selected while configuring the core, the MAC inserts the content of the MAC Address 1 registers in the SA field of all transmitted packets. 2'b11: - If Bit 30 is set to 0, the MAC replaces the content of the MAC Address 0 registers in the SA field of all transmitted packets. - If Bit 30 is set to 1 and the MAC Address Register 1 is enabled, the MAC replaces the content of the MAC Address 1 registers in the SA field of all transmitted packets. Note: - Changes to this field take effect only on the start of a packet. If you write to this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value. 0x0 (SA_CTRL_IN): mti_sa_ctrl_i and ati_sa_ctrl_i input signals control the SA field generation. 0x2 (MAC0_INS_SA): Contents of MAC Addr-0 inserted in SA field. 0x3 (MAC0_REP_SA): Contents of MAC Addr-0 replaces SA field. 0x6 (MAC1_INS_SA): Contents of MAC Addr-1 inserted in SA field. 0x7 (MAC1_REP_SA): Contents of MAC Addr-1 replaces SA field.
27	0h RW	**Checksum Offload (IPC):** When set, this bit enables the IPv4 header checksum checking and IPv4 or IPv6 TCP, UDP, or ICMP payload checksum checking. When this bit is reset, the COE function in the receiver is disabled. The Layer 3 and Layer 4 Packet Filter and Enable Split Header features automatically selects the IPC Full Checksum Offload Engine on the Receive side. When any of these features are enabled, you must set the IPC bit. 0x0 (DISABLE): IP header/payload checksum checking is disabled. 0x1 (ENABLE): IP header/payload checksum checking is enabled.

Bit Range	Default & Access	Field Name (ID): Description
26:24	0h RW	**Inter-Packet Gap (IPG):** These bits control the minimum IPG between packets during transmission. This range of minimum IPG is valid in full-duplex mode. In the half-duplex mode, the minimum IPG can be configured only for 64-bit times (IPG = 100). Lower values are not considered. When a JAM pattern is being transmitted because of backpressure activation, the MAC does not consider the minimum IPG. The above function (IPG less than 96 bit times) is valid only when EIPGEN bit in MAC_Ext_Configuration register is reset. When EIPGEN is set, then the minimum IPG (greater than 96 bit times) is controlled as per the description given in EIPG field in MAC_Ext_Configuration register. 0x0 (IPG96): 96 bit times IPG. 0x1 (IPG88): 88 bit times IPG. 0x2 (IPG80): 80 bit times IPG. 0x3 (IPG72): 72 bit times IPG. 0x4 (IPG64): 64 bit times IPG. 0x5 (IPG56): 56 bit times IPG. 0x6 (IPG48): 48 bit times IPG. 0x7 (IPG40): 40 bit times IPG.
23	0h RW	**Giant Packet Size Limit Control Enable (GPSLCE):** When this bit is set, the MAC considers the value in GPSL field in MAC_Ext_Configuration register to declare a received packet as Giant packet. This field must be programmed to more than 1,518 bytes. Otherwise, the MAC considers 1,518 bytes as giant packet limit. When this bit is reset, the MAC considers a received packet as Giant packet when its size is greater than 1,518 bytes (1522 bytes for tagged packet). The watchdog timeout limit, Jumbo Packet Enable and 2K Packet Enable have higher precedence over this bit, that is the MAC considers a received packet as Giant packet when its size is greater than 9,018 bytes (9,022 bytes for tagged packet) with Jumbo Packet Enabled and greater than 2,000 bytes with 2K Packet Enabled. The watchdog timeout, if enabled, terminates the received packet when watchdog limit is reached. Therefore, the programmed giant packet limit should be less than the watchdog limit to get the giant packet status. 0x0 (DISABLE): Giant Packet Size Limit Control is disabled. 0x1 (ENABLE): Giant Packet Size Limit Control is enabled.
22	0h RW	**IEEE 802.3as Support for 2K Packets (S2KP):** When this bit is set, the MAC considers all packets with up to 2,000 bytes length as normal packets. When the JE bit is not set, the MAC considers all received packets of size more than 2K bytes as Giant packets. When this bit is reset and the JE bit is not set, the MAC considers all received packets of size more than 1,518 bytes (1,522 bytes for tagged) as giant packets. Note: When the JE bit is set, setting this bit has no effect on the giant packet status. 0x0 (DISABLE): Support upto 2K packet is disabled. 0x1 (ENABLE): Support upto 2K packet is Enabled.
21	0h RW	**CRC stripping for Type packets (CST):** When this bit is set, the last four bytes (FCS) of all packets of Ether type (type field greater than 1,536) are stripped and dropped before forwarding the packet to the application. 0x0 (DISABLE): CRC stripping for Type packets is disabled. 0x1 (ENABLE): CRC stripping for Type packets is enabled.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**Automatic Pad or CRC Stripping (ACS):** When this bit is set, the MAC strips the Pad or FCS field on the incoming packets only if the value of the length field is less than 1,536 bytes. All received packets with length field greater than or equal to 1,536 bytes are passed to the application without stripping the Pad or FCS field. When this bit is reset, the MAC passes all incoming packets to the application, without any modification. 0x0 (DISABLE): Automatic Pad or CRC Stripping is disabled. 0x1 (ENABLE): Automatic Pad or CRC Stripping is enabled.
19	0h RW	**Watchdog Disable (WD):** When this bit is set, the MAC disables the watchdog timer on the receiver. The MAC can receive packets of up to 16,383 bytes. When this bit is reset, the MAC does not allow more than 2,048 bytes (10,240 if JE is set high) of the packet being received. The MAC cuts off any bytes received after 2,048 bytes. 0x0 (ENABLE): Watchdog is enabled. 0x1 (DISABLE): Watchdog is disabled.
18	0h RW	**Packet Burst Enable (BE):** When this bit is set, the MAC allows packet bursting during transmission in the GMII half-duplex mode. 0x0 (DISABLE): Packet Burst is disabled. 0x1 (ENABLE): Packet Burst is enabled.
17	0h RW	**Jabber Disable (JD):** When this bit is set, the MAC disables the jabber timer on the transmitter. The MAC can transfer packets of up to 16,383 bytes. When this bit is reset, if the application sends more than 2,048 bytes of data (10,240 if JE is set high) during transmission, the MAC does not send rest of the bytes in that packet. 0x0 (ENABLE): Jabber is enabled. 0x1 (DISABLE): Jabber is disabled.
16	0h RW	**Jumbo Packet Enable (JE):** When this bit is set, the MAC allows jumbo packets of 9,018 bytes (9,022 bytes for VLAN tagged packets) without reporting a giant packet error in the Rx packet status. 0x0 (DISABLE): Jumbo packet is disabled. 0x1 (ENABLE): Jumbo packet is enabled.
15	0h RW	**Port Select (PS):** This bit selects the Ethernet line speed. This bit, along with Bit 14, selects the exact line speed. In the 10/100 Mbps-only (always 1) or 1000 Mbps-only (always 0) configurations, this bit is read-only (RO) with appropriate value. In default 10/100/1000 Mbps configurations, this bit is read-write (R/W). 0x0 (M_1000_2500M): For 1000 or 2500 Mbps operations. 0x1 (M_10_100M): For 10 or 100 Mbps operations.
14	0h RW	**FES:** This bit selects the speed mode. 0x0 (M_10_1000M): 10 Mbps when PS bit is 1 and 1 Gbps when PS bit is 0. 0x1 (M_100_2500M): 100 Mbps when PS bit is 1 and 2.5 Gbps when PS bit is 0.
13	0h RW	**Duplex Mode (DM):** When this bit is set, the MAC operates in the full-duplex mode in which it can transmit and receive simultaneously. This bit is RO with default value of 1'b1 in the full-duplex-only configurations. 0x0 (HDUPLX): Half-duplex mode. 0x1 (FDUPLX): Full-duplex mode.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**Loopback Mode (LM):** When this bit is set, the MAC operates in the loopback mode at GMII or MII. The (G)MII Rx clock input (clk_rx_i) is required for the loopback to work properly. This is because the Tx clock is not internally looped back. 0x0 (DISABLE): Loopback is disabled. 0x1 (ENABLE): Loopback is enabled.
11	0h RW	**Enable Carrier Sense Before Transmission in Full-Duplex Mode (ECRSFD):** When this bit is set, the MAC transmitter checks the CRS signal before packet transmission in the full-duplex mode. The MAC starts the transmission only when the CRS signal is low. When this bit is reset, the MAC transmitter ignores the status of the CRS signal. 0x0 (DISABLE): ECRSFD is disabled. 0x1 (ENABLE): ECRSFD is enabled.
10	0h RW	**Disable Receive Own (DO):** When this bit is set, the MAC disables the reception of packets when the GMII signal TX_EN is asserted in the half-duplex mode. When this bit is reset, the MAC receives all packets given by the PHY. This bit is not applicable in the full-duplex mode. 0x0 (ENABLE): Enable Receive Own. 0x1 (DISABLE): Disable Receive Own.
9	0h RW	**Disable Carrier Sense During Transmission (DCRS):** When this bit is set, the MAC transmitter ignores the (G)MII CRS signal during packet transmission in the half-duplex mode. As a result, no errors are generated because of Loss of Carrier or No Carrier during transmission. When this bit is reset, the MAC transmitter generates errors because of Carrier Sense. The MAC can even abort the transmission. 0x0 (ENABLE): Enable Carrier Sense During Transmission. 0x1 (DISABLE): Disable Carrier Sense During Transmission.
8	0h RW	**Disable Retry (DR):** When this bit is set, the MAC attempts only one transmission. When a collision occurs on the GMII or MII interface, the MAC ignores the current packet transmission and reports a Packet Abort with excessive collision error in the Tx packet status. When this bit is reset, the MAC retries based on the settings of the BL field. This bit is applicable only in the half-duplex mode. 0x0 (ENABLE): Enable Retry. 0x1 (DISABLE): Disable Retry.
7	0h RO	**Reserved**
6:5	0h RW	**Back-Off Limit (BL):** The back-off limit determines the random integer number (r) of slot time delays (4,096 bit times for 1000/2500 Mbps; 512 bit times for 10/100 Mbps) for which the MAC waits before rescheduling a transmission attempt during retries after a collision. n = retransmission attempt. The random integer r takes the value in the range 0 <= r < 2^k This bit is applicable only in the half-duplex mode. 0x0 (MIN_N_10): k = min(n,10). 0x1 (MIN_N_8): k = min(n,8). 0x2 (MIN_N_4): k = min(n,4). 0x3 (MIN_N_1): k = min(n,1).

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Deferral Check (DC):** When this bit is set, the deferral check function is enabled in the MAC. The MAC issues a Packet Abort status, along with the excessive deferral error bit set in the Tx packet status, when the Tx state machine is deferred for more than 24,288 bit times in 10 or 100 Mbps mode. If the MAC is configured for 1000/2500 Mbps operation, the threshold for deferral is 155,680 bits times. Deferral begins when the transmitter is ready to transmit, but it is prevented because of an active carrier sense signal (CRS) on GMII or MII. The defer time is not cumulative. For example, if the transmitter defers for 10,000 bit times because the CRS signal is active and the CRS signal becomes inactive, the transmitter transmits and collision happens. Because of collision, the transmitter needs to back off and then defer again after back off completion. In such a scenario, the deferral timer is reset to 0, and it is restarted. When this bit is reset, the deferral check function is disabled and the MAC defers until the CRS signal goes inactive. This bit is applicable only in the half-duplex mode. 0x0 (DISABLE): Deferral check function is disabled. 0x1 (ENABLE): Deferral check function is enabled.
3:2	0h RW	**Preamble Length for Transmit packets (PRELEN):** These bits control the number of preamble bytes that are added to the beginning of every Tx packet. The preamble reduction occurs only when the MAC is operating in the full-duplex mode. 0x0 (M_7BYTES): 7 bytes of preamble. 0x1 (M_5BYTES): 5 bytes of preamble. 0x2 (M_3BYTES): 3 bytes of preamble. 0x3 (RESERVED): Reserved.
1	0h RW	**Transmitter Enable (TE):** When this bit is set, the Tx state machine of the MAC is enabled for transmission on the GMII or MII interface. When this bit is reset, the MAC Tx state machine is disabled after it completes the transmission of the current packet. The Tx state machine does not transmit any more packets. 0x0 (DISABLE): Transmitter is disabled. 0x1 (ENABLE): Transmitter is enabled.
0	0h RW	**Receiver Enable (RE):** When this bit is set, the Rx state machine of the MAC is enabled for receiving packets from the GMII or MII interface. When this bit is reset, the MAC Rx state machine is disabled after it completes the reception of the current packet. The Rx state machine does not receive any more packets from the GMII or MII interface. 0x0 (DISABLE): Receiver is disabled. 0x1 (ENABLE): Receiver is enabled.

10.2.2 MAC_EXT_CONFIGURATION — Offset 4h

The MAC Extended Configuration Register establishes the operating mode of the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RW	**ARP Packet Drop if IP Mismatch (APDIM):** When set, Packet for which Target Protocol Address does not match IPv4 address is dropped in the MTL layer. When reset, when target Protocol Address does not match, packet is forwarded to MTL maintaining backward compatibility. 0x0 (DISABLE): mux select to drop the arp packet if Trgt prot address mismatches IPv4 address disabled. 0x1 (ENABLE): mux select to drop the arp packet if Trgt prot address mismatches IPv4 address enabled.
29:25	00h RW	**Extended Inter-Packet Gap (EIPG):** The value in this field is applicable when the EIPGEN bit is set. This field (as Most Significant bits), along with IPG field in MAC_Configuration register, gives the minimum IPG greater than 96 bit times in steps of 8 bit times: {EIPG, IPG} 8'h00 - 104 bit times 8'h01 - 112 bit times 8'h02 - 120 bit times ---------- 8'hFF - 2144 bit times
24	0h RW	**Extended Inter-Packet Gap Enable (EIPGEN):** When this bit is set, the MAC interprets EIPG field and IPG field in MAC_Configuration register together as minimum IPG greater than 96 bit times in steps of 8 bit times. When this bit is reset, the MAC ignores EIPG field and interprets IPG field in MAC_Configuration register as minimum IPG less than or equal to 96 bit times in steps of 8 bit times. Note: The extended Inter-Packet Gap feature must be enabled when operating in Full-Duplex mode only. There might be undesirable effects on back-pressure function and frame transmission if it is enabled in Half-Duplex mode. 0x0 (DISABLE): Extended Inter-Packet Gap is disabled. 0x1 (ENABLE): Extended Inter-Packet Gap is enabled.
23	0h RO	**Reserved**
22:20	0h RW	**Maximum Size for Splitting the Header Data (HDSMS):** These bits indicate the maximum header size allowed for splitting the header data in the received packet. 0x0 (M_64BYTES): Maximum Size for Splitting the Header Data is 64 bytes. 0x1 (M_128BYTES): Maximum Size for Splitting the Header Data is 128 bytes. 0x2 (M_256BYTES): Maximum Size for Splitting the Header Data is 256 bytes. 0x3 (M_512BYTES): Maximum Size for Splitting the Header Data is 512 bytes. 0x4 (M_1024BYTES): Maximum Size for Splitting the Header Data is 1024 bytes. 0x5 (RSVD): Reserved.
19	0h RW	**Packet Duplication Control (PDC):** When this bit is set, the received packet with Multicast/Broadcast Destination address is routed to multiple Receive DMA Channels. The Receive DMA Channels is identified by the DCS field of MAC_Address(#i)_High register corresponding to the MAC Address register that matches the Multicast/Broadcast Destination address in the received packet. The DCS field is interpreted to be a one-hot value, each bit corresponding to the Receive DMA Channel. When this bit is reset, the received packet is routed to single Receive DMA Channel. The Receive DMA Channel is identified by the DCS field of MAC_Address(#i)_High register corresponding to the MAC Address register that matches the Destination address in the received packet. The DCS field is interpreted as a binary value. 0x0 (DISABLE): Packet Duplication Control is disabled. 0x1 (ENABLE): Packet Duplication Control is enabled.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**Unicast Slow Protocol Packet Detect (USP):** When this bit is set, the MAC detects the Slow Protocol packets with unicast address of the station specified in the MAC_Address0_High and MAC_Address0_Low registers. The MAC also detects the Slow Protocol packets with the Slow Protocols multicast address (01-80-C2-00-00-02). When this bit is reset, the MAC detects only Slow Protocol packets with the Slow Protocol multicast address specified in the IEEE 802.3-2015, Section 5. 0x0 (DISABLE): Unicast Slow Protocol Packet Detection is disabled. 0x1 (ENABLE): Unicast Slow Protocol Packet Detection is enabled.
17	0h RW	**Slow Protocol Detection Enable (SPEN):** When this bit is set, MAC processes the Slow Protocol packets (Ether Type 0x8809) and provides the Slow Protocol Sub-Type and Code fields in Rx status. When this bit is reset, the MAC forwards all error-free Slow Protocol packets to the application. The MAC considers such packets as normal Type packets. 0x0 (DISABLE): Slow Protocol Detection is disabled. 0x1 (ENABLE): Slow Protocol Detection is enabled.
16	0h RW	**Disable CRC Checking for Received Packets (DCRCC):** When this bit is set, the MAC receiver does not check the CRC field in the received packets. When this bit is reset, the MAC receiver always checks the CRC field in the received packets. 0x0 (ENABLE): CRC Checking is enabled. 0x1 (DISABLE): CRC Checking is disabled.
15:14	0h RO	**Reserved**
13:0	0000h RW	**Giant Packet Size Limit (GPSL):** If the received packet size is greater than the value programmed in this field in units of bytes, the MAC declares the received packet as Giant packet. The value programmed in this field must be greater than or equal to 1,518 bytes. Any other programmed value is considered as 1,518 bytes. For VLAN tagged packets, the MAC adds 4 bytes to the programmed value. When the Enable Double VLAN Processing option is selected, the MAC adds 8 bytes to the programmed value for double VLAN tagged packets. The value in this field is applicable when the GPSLCE bit is set in MAC_Configuration register.

10.2.3 MAC_PACKET_FILTER — Offset 8h

The MAC Packet Filter register contains the filter controls for receiving packets. Some of the controls from this register go to the address check block of the MAC which performs the first level of address filtering. The second level of filtering is performed on the incoming packet based on other controls such as Pass Bad Packets and Pass Control Packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Receive All (RA):** When this bit is set, the MAC Receiver module passes all received packets to the application, irrespective of whether they pass the address filter or not. The result of the SA or DA filtering is updated (pass or fail) in the corresponding bit in the Rx Status Word. When this bit is reset, the Receiver module passes only those packets to the application that pass the SA or DA address filter. 0x0 (DISABLE): Receive All is disabled. 0x1 (ENABLE): Receive All is enabled.
30:22	0h RO	**Reserved**
21	0h RW	**Drop Non-TCP/UDP over IP Packets (DNTU):** When this bit is set, the MAC drops the non-TCP or UDP over IP packets. The MAC forward only those packets that are processed by the Layer 4 filter. When this bit is reset, the MAC forwards all non-TCP or UDP over IP packets. 0x0 (FWD): Forward Non-TCP/UDP over IP Packets. 0x1 (DROP): Drop Non-TCP/UDP over IP Packets.
20	0h RW	**Layer 3 and Layer 4 Filter Enable (IPFE):** When this bit is set, the MAC drops packets that do not match the enabled Layer 3 and Layer 4 filters. If Layer 3 or Layer 4 filters are not enabled for matching, this bit does not have any effect. When this bit is reset, the MAC forwards all packets irrespective of the match status of the Layer 3 and Layer 4 fields. 0x0 (DISABLE): Layer 3 and Layer 4 Filters are disabled. 0x1 (ENABLE): Layer 3 and Layer 4 Filters are enabled.
19:17	0h RO	**Reserved**
16	0h RW	**VLAN Tag Filter Enable (VTFE):** When this bit is set, the MAC drops the VLAN tagged packets that do not match the VLAN Tag. When this bit is reset, the MAC forwards all packets irrespective of the match status of the VLAN Tag. 0x0 (DISABLE): VLAN Tag Filter is disabled. 0x1 (ENABLE): VLAN Tag Filter is enabled.
15:11	0h RO	**Reserved**
10	0h RW	**Hash or Perfect Filter (HPF):** When this bit is set, the address filter passes a packet if it matches either the perfect filtering or hash filtering as set by the HMC or HUC bit. When this bit is reset and the HUC or HMC bit is set, the packet is passed only if it matches the Hash filter. 0x0 (DISABLE): Hash or Perfect Filter is disabled. 0x1 (ENABLE): Hash or Perfect Filter is enabled.
9	0h RW	**Source Address Filter Enable (SAF):** When this bit is set, the MAC compares the SA field of the received packets with the values programmed in the enabled SA registers. If the comparison fails, the MAC drops the packet. When this bit is reset, the MAC forwards the received packet to the application with updated SAF bit of the Rx Status depending on the SA address comparison. Note: According to the IEEE specification, Bit 47 of the SA is reserved. However, in GbE Controller, the MAC compares all 48 bits. The software driver should take this into consideration while programming the MAC address registers for SA. 0x0 (DISABLE): SA Filtering is disabled. 0x1 (ENABLE): SA Filtering is enabled.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**SA Inverse Filtering (SAIF):** When this bit is set, the Address Check block operates in the inverse filtering mode for SA address comparison. If the SA of a packet matches the values programmed in the SA registers, it is marked as failing the SA Address filter. When this bit is reset, if the SA of a packet does not match the values programmed in the SA registers, it is marked as failing the SA Address filter. 0x0 (DISABLE): SA Inverse Filtering is disabled. 0x1 (ENABLE): SA Inverse Filtering is enabled.
7:6	0h RW	**Pass Control Packets (PCF):** These bits control the forwarding of all control packets (including unicast and multicast Pause packets). 0x0 (FLTR_ALL): MAC filters all control packets from reaching the application. 0x1 (FW_XCPT_PAU): MAC forwards all control packets except Pause packets to the application even if they fail the Address filter. 0x2 (FW_ALL): MAC forwards all control packets to the application even if they fail the Address filter. 0x3 (FW_PASS): MAC forwards the control packets that pass the Address filter.
5	0h RW	**Disable Broadcast Packets (DBF):** When this bit is set, the AFM module blocks all incoming broadcast packets. In addition, it overrides all other filter settings. When this bit is reset, the AFM module passes all received broadcast packets. 0x0 (ENABLE): Enable Broadcast Packets. 0x1 (DISABLE): Disable Broadcast Packets.
4	0h RW	**Pass All Multicast (PM):** When this bit is set, it indicates that all received packets with a multicast destination address (first bit in the destination address field is '1') are passed. When this bit is reset, filtering of multicast packet depends on HMC bit. 0x0 (DISABLE): Pass All Multicast is disabled. 0x1 (ENABLE): Pass All Multicast is enabled.
3	0h RW	**DA Inverse Filtering (DAIF):** When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast packets. When this bit is reset, normal filtering of packets is performed. 0x0 (DISABLE): DA Inverse Filtering is disabled. 0x1 (ENABLE): DA Inverse Filtering is enabled.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Hash Multicast (HMC):** When this bit is set, the MAC performs the destination address filtering of received multicast packets according to the hash table. When this bit is reset, the MAC performs the perfect destination address filtering for multicast packets, that is, it compares the DA field with the values programmed in DA registers. 0x0 (DISABLE): Hash Multicast is disabled. 0x1 (ENABLE): Hash Multicast is enabled.
1	0h RW	**Hash Unicast (HUC):** When this bit is set, the MAC performs the destination address filtering of unicast packets according to the hash table. When this bit is reset, the MAC performs a perfect destination address filtering for unicast packets, that is, it compares the DA field with the values programmed in DA registers. 0x0 (DISABLE): Hash Unicast is disabled. 0x1 (ENABLE): Hash Unicast is enabled.
0	0h RW	**Promiscuous Mode (PR):** When this bit is set, the Address Filtering module passes all incoming packets irrespective of the destination or source address. The SA or DA Filter Fails status bits of the Rx Status Word are always cleared when PR is set. 0x0 (DISABLE): Promiscuous Mode is disabled. 0x1 (ENABLE): Promiscuous Mode is enabled.

10.2.4 MAC_WATCHDOG_TIMEOUT — Offset Ch

The Watchdog Timeout register controls the watchdog timeout for received packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Programmable Watchdog Enable (PWE):** When this bit is set and the WD bit of the MAC_Configuration register is reset, the WTO field is used as watchdog timeout for a received packet. When this bit is cleared, the watchdog timeout for a received packet is controlled by setting of WD and JE bits in MAC_Configuration register. 0x0 (DISABLE): Programmable Watchdog is disabled. 0x1 (ENABLE): Programmable Watchdog is enabled.
7:4	0h RO	**Reserved**
3:0	0h RW	**Watchdog Timeout (WTO):** When the PWE bit is set and the WD bit of the MAC_Configuration register is reset, this field is used as watchdog timeout for a received packet. If the length of a received packet exceeds the value of this field, such packet is terminated and declared as an error packet. Note: When the PWE bit is set, the value in this field should be more than 1,522 (0x05F2). Otherwise, the IEEE 802.3-specified valid tagged packets are declared as error packets and then dropped. 0x0 (M_2KBYTES): 2 KB. 0x1 (M_3KBYTES): 3 KB. 0x2 (M_4KBYTES): 4 KB. 0x3 (M_5KBYTES): 5 KB. 0x4 (M_6KBYTES): 6 KB. 0x5 (M_7KBYTES): 7 KB. 0x6 (M_8KBYTES): 8 KB. 0x7 (M_9KBYTES): 9 KB. 0x08 (M_10KBYTES): 10 KB. 0x09 (M_11KBYTES): 11 KB. 0x0A (M_12KBYTES): 12 KB. 0x0B (M_13KBYTES): 13 KB. 0x0C (M_14KBYTES): 14 KB. 0x0D (M_15KBYTES): 15 KB. 0x0E (M_16383BYTES): 16383 Bytes. 0x0F (RESERVED): Reserved.

10.2.5 MAC_HASH_TABLE_REG0 — Offset 10h

The Hash Table Register 0 contains the first 32 bits of the hash table, when the width of the hash table is 128 or 256 bits. This design has set the Hash Table Size (width of the hash table) to 64.

The Hash table is used for group address filtering. For hash filtering, the content of the destination address in the incoming packet is passed through the CRC logic and the upper six (seven in 128-bit Hash or eight in 256-bit Hash) bits of the CRC register are used to index the content of the Hash table. The most significant bits determines the register to be used (Hash Table Register X), and the least significant five bits determine the bit within the register. For example, a hash value of 6'b100000 (in 64-bit Hash) selects Bit 0 of the Hash Table Register 1, a value of 7b'1110000 (in 128-bit Hash) selects Bit 16 of the Hash Table Register 3 and a value of 8b'10111111 (in 256-bit Hash) selects Bit 31 of the Hash Table Register 5.

The hash value of the destination address is calculated in the following way:

- Calculate the 32-bit CRC for the DA (See IEEE 802.3, Section 3.2.8 for the steps to calculate CRC32).

- Perform bitwise reversal for the value obtained in Step 1.

- Take the upper 6 (or 7 or 8) bits from the value obtained in Step 2.

If the corresponding bit value of the register is 1'b1, the packet is accepted. Otherwise, it is rejected. If the PM bit is set in MAC_Packet_Filter, all multicast packets are accepted regardless of the multicast hash values.

If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] of the Hash Table Register X registers are written.

If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MAC Hash Table First 32 Bits (HT31T0):** This field contains the first 32 Bits [31:0] of the Hash table.

10.2.6 MAC_HASH_TABLE_REG1 — Offset 14h

The Hash Table Register 1 contains the second 32 bits of the hash table.

The Hash table is used for group address filtering. For hash filtering, the content of the destination address in the incoming packet is passed through the CRC logic and the upper six (seven in 128-bit Hash or eight in 256-bit Hash) bits of the CRC register are used to index the content of the Hash table. The most significant bits determines the register to be used (Hash Table Register X), and the least significant five bits determine the bit within the register. For example, a hash value of 6'b100000 (in 64-bit Hash) selects Bit 0 of the Hash Table Register 1, a value of 7b'1110000 (in 128-bit Hash) selects Bit 16 of the Hash Table Register 3 and a value of 8b'10111111 (in 256-bit Hash) selects Bit 31 of the Hash Table Register 5.

The hash value of the destination address is calculated in the following way:

- Calculate the 32-bit CRC for the DA (See IEEE 802.3, Section 3.2.8 for the steps to calculate CRC32).

- Perform bitwise reversal for the value obtained in Step 1.

- Take the upper 6 (or 7 or 8) bits from the value obtained in Step 2.

If the corresponding bit value of the register is 1'b1, the packet is accepted. Otherwise, it is rejected. If the PM bit is set in MAC_Packet_Filter, all multicast packets are accepted regardless of the multicast hash values.

If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] of the Hash Table Register X registers are written.

If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MAC Hash Table Second 32 Bits (HT63T32):** This field contains the second 32 Bits [63:32] of the Hash table.

10.2.7 MAC_VLAN_TAG_CTRL — Offset 50h

This register is the redefined format of the MAC VLAN Tag Register. It is used for indirect addressing. It contains the address offset, command type and Busy Bit for CSR access of the Per VLAN Tag registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Inner VLAN Tag in Rx Status (EIVLRXS):** When this bit is set, the MAC provides the inner VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the inner VLAN Tag in Rx status. 0x0 (DISABLE): Inner VLAN Tag in Rx status is disabled. 0x1 (ENABLE): Inner VLAN Tag in Rx status is enabled.
30	0h RO	**Reserved**
29:28	0h RW	**Enable Inner VLAN Tag Stripping on Receive (EIVLS):** This field indicates the stripping operation on inner VLAN Tag in received packet. 0x0 (DONOT): Do not strip. 0x1 (IFPASS): Strip if VLAN filter passes. 0x2 (IFFAIL): Strip if VLAN filter fails. 0x3 (ALWAYS): Always strip.
27	0h RW	**Enable Inner VLAN Tag Comparison (ERIVLT):** When this bit, VTHM bit and the EDVLP field are set, the MAC receiver enables VLAN Hash filtering operation on the inner VLAN Tag (if present). When this bit is reset and VTHM bit is set, the MAC receiver enables VLAN Hash filtering operation on the outer VLAN Tag (if present). The ERSVLM bit and DOVLTC bit determines which VLAN type is enabled for filtering. 0x0 (DISABLE): Inner VLAN tag is disabled. 0x1 (ENABLE): Inner VLAN tag is enabled.
26	0h RW	**Enable Double VLAN Processing (EDVLP):** When this bit is set, the MAC enables processing of up to two VLAN Tags on Tx and Rx (if present). When this bit is reset, the MAC enables processing of up to one VLAN Tag on Tx and Rx (if present). 0x0 (DISABLE): Double VLAN Processing is disabled. 0x1 (ENABLE): Double VLAN Processing is enabled.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RW	**VLAN Tag Hash Table Match Enable (VTHM):** When this bit is set, the most significant four bits of CRC of VLAN Tag are used to index the content of the MAC_VLAN_Hash_Table register. A value of 1 in the VLAN Hash Table register, corresponding to the index, indicates that the packet matched the VLAN hash table. When the ETV bit is set, the CRC of the 12-bit VLAN Identifier (VID) is used for comparison. When the ETV bit is reset, the CRC of the 16-bit VLAN tag is used for comparison. When this bit is reset, the VLAN Hash Match operation is not performed. 0x0 (DISABLE): VLAN Tag Hash Table Match is disabled. 0x1 (ENABLE): VLAN Tag Hash Table Match is enabled.
24	0h RW	**Enable VLAN Tag in Rx status (EVLRXS):** When this bit is set, MAC provides the outer VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the outer VLAN Tag in Rx status. 0x0 (DISABLE): VLAN Tag in Rx status is disabled. 0x1 (ENABLE): VLAN Tag in Rx status is enabled.
23	0h RO	**Reserved**
22:21	0h RW	**Enable VLAN Tag Stripping on Receive (EVLS):** This field indicates the stripping operation on the outer VLAN Tag in received packet. 0x0 (DONOT): Do not strip. 0x1 (IFPASS): Strip if VLAN filter passes. 0x2 (IFFAIL): Strip if VLAN filter fails. 0x3 (ALWAYS): Always strip.
20	0h RW	**Disable VLAN Type Check for VLAN Hash Filtering (DOVLTC):** When this bit is set, the MAC VLAN Hash Filter does not check whether the VLAN Tag specified by the ERIVLT bit is of type S-VLAN or C-VLAN. When this bit is reset, the MAC VLAN Hash Filter filters or matches the VLAN Tag specified by the ERIVLT bit only when VLAN Tag type is similar to the one specified by the ERSVLM bit. 0x0 (ENABLE): VLAN Type Check is enabled. 0x1 (DISABLE): VLAN Type Check is disabled.
19	0h RW	**Enable Receive S-VLAN Match for VLAN Hash Filtering (ERSVLM):** When this bit is set, the MAC receiver enables VLAN Hash filtering or matching for S-VLAN (Type = 0x88A8) packets. When this bit is reset, the MAC receiver enables VLAN Hash filtering or matching for C-VLAN (Type = 0x8100) packets. The ERIVLT bit determines the VLAN tag position considered for VLAN Hash filtering or matching. 0x0 (DISABLE): Receive S-VLAN Match is disabled. 0x1 (ENABLE): Receive S-VLAN Match is enabled.
18	0h RW	**Enable S-VLAN (ESVL):** When this bit is set, the MAC transmitter and receiver consider the S-VLAN packets (Type = 0x88A8) as valid VLAN tagged packets. 0x0 (DISABLE): S-VLAN is disabled. 0x1 (ENABLE): S-VLAN is enabled.
17	0h RW	**VLAN Tag Inverse Match Enable (VTIM):** When this bit is set, this bit enables the VLAN Tag inverse matching. The packets without matching VLAN Tag are marked as matched. When reset, this bit enables the VLAN Tag perfect matching. The packets with matched VLAN Tag are marked as matched. 0x0 (DISABLE): VLAN Tag Inverse Match is disabled. 0x1 (ENABLE): VLAN Tag Inverse Match is enabled.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Enable 12-Bit VLAN Tag Comparison for VLAN Hash Filtering (ETV):** When this bit is set, a 12-bit VLAN identifier is used for VLAN Hash filtering instead of the complete 16-bit VLAN tag. Bits[11:0] of VLAN tag in the received VLAN-tagged packet are used for hash-based VLAN filtering. When this bit is reset, all 16 bits of the 15th and 16th bytes of the received VLAN packet are used for VLAN hash filtering. 0x0 (DISABLE): 12-Bit VLAN Tag Comparison is disabled. 0x1 (ENABLE): 12-Bit VLAN Tag Comparison is enabled.
15:5	0h RO	**Reserved**
4:2	0h RW	**OFS:** This field holds the address offset of the MAC VLAN Tag Filter Register which the application is trying to access. The width of the field depends on the number of MAC VLAN Tag Registers enabled.
1	0h RW	**Command Type (CT):** This bit indicates if the current register access is a read or a write. When set, it indicate a read operation. When reset, it indicates a write operation. 0x0 (WRITE): Write operation. 0x1 (READ): Read operation.
0	0h RW	**Operation Busy (OB):** This bit is set along with a read or write command for initiating the indirect access to per VLAN Tag Filter register. This bit is reset when the read or write command to per VLAN Tag Filter indirect access register is complete. The next indirect register access can be initiated only after this bit is reset. During a write operation, the bit is reset only after the data has been written into the Per VLAN Tag register. During a read operation, the data should be read from the MAC_VLAN_Tag_Data register only after this bit is reset. 0x0 (DISABLE): Operation Busy is disabled. 0x1 (ENABLE): Operation Busy is enabled.

10.2.8 MAC_VLAN_TAG_DATA — Offset 54h

This register holds the read/write data for Indirect Access of the Per VLAN Tag registers. During the read access, this field contains valid read data only after the OB bit is reset.

During the write access, this field should be valid prior to setting the OB bit in the MAC_VLAN_Tag_Ctrl Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 54h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:25	0h RW	**DMA Channel Number (DMACHN):** The DMA Channel number to which the VLAN Tagged Frame is to be routed if it passes this VLAN Tag Filter is programmed in this field. If the Routing based on VLAN Tag Filter is not necessary, this field need not be programmed.
24	0h RW	**DMA Channel Number Enable (DMACHEN):** This bit is the Enable for the DMA Channel Number value programmed in the field DMACH. When this bit is reset, the Routing does not occur based on VLAN Filter result. The frame is routed based on DA Based DMA Channel Routing. 0x0 (DISABLE): DMA Channel Number is disabled. 0x1 (ENABLE): DMA Channel Number is enabled.
23:21	0h RO	**Reserved**
20	0h RW	**Enable Inner VLAN Tag Comparison (ERIVLT):** This bit is valid only when Double VLAN Tag Enable of the Filter is set. When this bit and the EDVLP field are set, the MAC receiver enables operation on the inner VLAN Tag (if present). When this bit is reset, the MAC receiver enables operation on the outer VLAN Tag (if present). 0x0 (DISABLE): Inner VLAN tag comparison is disabled. 0x1 (ENABLE): Inner VLAN tag comparison is enabled.
19	0h RW	**Enable S-VLAN Match for received Frames (ERSVLM):** This bit is valid only when VLAN Tag Enable of the Filter is set. When this bit is set, the MAC receiver enables filtering or matching for S-VLAN (Type = 0x88A8) packets. When this bit is reset, the MAC receiver enables filtering or matching for C-VLAN (Type = 0x8100) packets. 0x0 (DISABLE): Receive S-VLAN Match is disabled. 0x1 (ENABLE): Receive S-VLAN Match is enabled.
18	0h RW	**Disable VLAN Type Comparison (DOVLTC):** This bit is valid only when VLAN Tag Enable of the Filter is set. When this bit is set, the MAC does not check whether the VLAN Tag specified by the Enable Inner VLAN Tag Comparison bit is of type S-VLAN or C-VLAN. When this bit is reset, the MAC filters or matches the VLAN Tag specified by the Enable Inner VLAN Tag Comparison bit only when VLAN Tag type is similar to the one specified by the Enable S-VLAN Match for received Frames bit. 0x0 (ENABLE): VLAN type comparison is enabled. 0x1 (DISABLE): VLAN type comparison is disabled.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**12bits or 16bits VLAN comparison (ETV):** This bit is valid only when VEN of the Filter is set. When this bit is set, a 12-bit VLAN identifier is used for comparing and filtering instead of the complete 16-bit VLAN tag. Bits [11:0] of VLAN tag are compared with the corresponding field in the received VLAN-tagged packet. 0x0 (M_16BIT): 16 bit VLAN comparison. 0x1 (M_12BIT): 12 bit VLAN comparison.
16	0h RW	**VLAN Tag Enable (VEN):** This bit is used to enable or disable the VLAN Tag. When this bit is set, the MAC compares the VLAN Tag of received packet with the VLAN Tag ID. When this bit is reset, no comparison is performed irrespective of the programming of the other fields. 0x0 (DISABLE): VLAN Tag is disabled. 0x1 (ENABLE): VLAN Tag is enabled.
15:0	0000h RW	**VLAN Tag ID (VID):** This field holds the VLAN Tag value which is used by the MAC for perfect comparison. It is valid when VLAN Tag Enable is set.

10.2.9 MAC_VLAN_HASH_TABLE — Offset 58h

When VTHM bit of the MAC_VLAN_Tag register is set, the 16-bit VLAN Hash Table register is used for group address filtering based on the VLAN tag. For hash filtering, the content of the 16-bit VLAN tag or 12-bit VLAN ID (based on the ETV bit of MAC_VLAN_Tag Register) in the incoming packet is passed through the CRC logic. The upper four bits of the calculated hash value are used to index the contents of the VLAN Hash table. For example, hash value of 4b'1000 selects Bit 8 of the VLAN Hash table.

The hash value of the destination address is calculated in the following way:

- Calculate the 32-bit CRC for the VLAN tag or ID (For steps to calculate CRC32, see Section 3.2.8 of IEEE 802.3).

- Perform bitwise reversal for the value obtained in step 1.

- Take the upper four bits from the value obtained in step 2.

If the VLAN hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[15:8] of this register are written.

- If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**VLAN Hash Table (VLHT):** This field contains the 16-bit VLAN Hash Table.

10.2.10 MAC_VLAN_INCL — Offset 60h

The VLAN Tag Inclusion or Replacement register contains the VLAN tag for insertion or replacement in the Transmit packets. It also contains the VLAN tag insertion controls.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**BUSY:** This bit indicates the status of the read/write operation of indirect access to the queue/channel specific VLAN inclusion register. For write operation write to a register is complete when this bit is reset. For read operation the read data is valid when the bit is reset. The application must make sure that this bit is reset before attempting subsequent access to this register. 0x0 (INACTIVE): Busy status not detected. 0x1 (ACTIVE): Busy status detected.
30	0h RW	**Read write control (RDWR):** This bit controls the read or write operation for indirectly accessing the queue/channel specific VLAN Inclusion register. When set indicates write operation and when reset indicates read operation. This does not have any effect when CBTI is reset. 0x0 (READ): Read operation of indirect access. 0x1 (WRITE): Write operation of indirect access.
29:27	0h RO	**Reserved**
26:24	0h RW	**ADDR:** This field selects one of the queue/channel specific VLAN Inclusion register for read/write access. This does not have any effect when CBTI is reset.
23:22	0h RO	**Reserved**
21	0h RW	**Channel based tag insertion (CBTI):** When this bit is set, outer VLAN tag is inserted for every packets transmitted by the MAC. The tag value is taken from the queue/channel specific VLAN tag register. The VLTI, VLP, VLC, and VLT fields of this register are ignored when this bit is set. When this bit is set, a write operation to byte 3 of this register initiates the read/write access to the indirect register. When reset, outer VLAN operation is based on the setting of VLTI, VLP, VLC and VLT fields of this register. 0x0 (DISABLE): Channel based tag insertion is disabled. 0x1 (ENABLE): Channel based tag insertion is enabled.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**VLAN Tag Input (VLTI):** When this bit is set, it indicates that the VLAN tag to be inserted or replaced in Tx packet should be taken from: - The Tx descriptor 0x0 (DISABLE): VLAN Tag Input is disabled. 0x1 (ENABLE): VLAN Tag Input is enabled.
19	0h RW	**C-VLAN or S-VLAN (CSVL):** When this bit is set, S-VLAN type (0x88A8) is inserted in the 13th and 14th bytes of transmitted packets. When this bit is reset, C-VLAN type (0x8100) is inserted in the 13th and 14th bytes of transmitted packets. 0x0 (C_VLAN): C-VLAN type (0x8100) is inserted. 0x1 (S_VLAN): S-VLAN type (0x88A8) is inserted.
18	0h RW	**VLAN Priority Control (VLP):** When this bit is set, the control bits[17:16] are used for VLAN deletion, insertion, or replacement. When this bit is reset, the mti_vlan_ctrl_i control input is used and bits[17:16] are ignored. 0x0 (DISABLE): VLAN Priority Control is disabled. 0x1 (ENABLE): VLAN Priority Control is enabled.
17:16	0h RW	**VLC:** VLAN Tag Control in Transmit Packets - 2'b00: No VLAN tag deletion, insertion, or replacement - 2'b01: VLAN tag deletion The MAC removes the VLAN type (bytes 13 and 14) and VLAN tag (bytes 15 and 16) of all transmitted packets with VLAN tags. - 2'b10: VLAN tag insertion The MAC inserts VLT in bytes 15 and 16 of the packet after inserting the Type value (0x8100 or 0x88a8) in bytes 13 and 14. This operation is performed on all transmitted packets, irrespective of whether they already have a VLAN tag. - 2'b11: VLAN tag replacement The MAC replaces VLT in bytes 15 and 16 of all VLAN-type transmitted packets (Bytes 13 and 14 are 0x8100 or 0x88a8). Note: Changes to this field take effect only on the start of a packet. If you write this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value. 0x0 (NONE): No VLAN tag deletion, insertion, or replacement. 0x1 (DELETE): VLAN tag deletion. 0x2 (INSERT): VLAN tag insertion. 0x3 (REPLACE): VLAN tag replacement.
15:0	0000h RW	**VLAN Tag for Transmit Packets (VLT):** This field contains the value of the VLAN tag to be inserted. The value must only be changed when the transmit lines are inactive or during the initialization phase. Bits[15:13] are the User Priority field, Bit 12 is the CFI/DEI field, and Bits[11:0] are the VID field in the VLAN tag. The following list describes the bits of this field: - Bits[15:13]: User Priority - Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) - Bits[11:0]: VLAN Identifier (VID) field of VLAN tag

10.2.11 MAC_INNER_VLAN_INCL — Offset 64h

The Inner VLAN Tag Inclusion or Replacement register contains the inner VLAN tag to be inserted or replaced in the Transmit packet. It also contains the inner VLAN tag insertion controls.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RW	**VLAN Tag Input (VLTI):** When this bit is set, it indicates that the VLAN tag to be inserted or replaced in Tx packet should be taken from: - The Tx descriptor 0x0 (DISABLE): VLAN Tag Input is disabled. 0x1 (ENABLE): VLAN Tag Input is enabled.
19	0h RW	**C-VLAN or S-VLAN (CSVL):** When this bit is set, S-VLAN type (0x88A8) is inserted or replaced in the 17th and 18th bytes of transmitted packets. When this bit is reset, C-VLAN type (0x8100) is inserted or replaced in the 17th and 18th bytes of transmitted packets. 0x0 (C_VLAN): C-VLAN type (0x8100) is inserted. 0x1 (S_VLAN): S-VLAN type (0x88A8) is inserted.
18	0h RW	**VLAN Priority Control (VLP):** When this bit is set, the VLC field is used for VLAN deletion, insertion, or replacement. When this bit is reset, the mti_vlan_ctrl_i control input is used and the VLC field is ignored. 0x0 (DISABLE): VLAN Priority Control is disabled. 0x1 (ENABLE): VLAN Priority Control is enabled.
17:16	0h RW	**VLC:** VLAN Tag Control in Transmit Packets - 2'b00: No VLAN tag deletion, insertion, or replacement - 2'b01: VLAN tag deletion The MAC removes the VLAN type (bytes 17 and 18) and VLAN tag (bytes 19 and 20) of all transmitted packets with VLAN tags. - 2'b10: VLAN tag insertion The MAC inserts VLT in bytes 19 and 20 of the packet after inserting the Type value (0x8100 or 0x88a8) in bytes 17 and 18. This operation is performed on all transmitted packets, irrespective of whether they already have a VLAN tag. - 2'b11: VLAN tag replacement The MAC replaces VLT in bytes 19 and 20 of all VLAN-type transmitted packets (Bytes 17 and 18 are 0x8100 or 0x88a8). Note: Changes to this field take effect only on the start of a packet. If you write this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value. 0x0 (NONE): No VLAN tag deletion, insertion, or replacement. 0x1 (DELETE): VLAN tag deletion. 0x2 (INSERT): VLAN tag insertion. 0x3 (REPLACE): VLAN tag replacement.
15:0	0000h RW	**VLAN Tag for Transmit Packets (VLT):** This field contains the value of the VLAN tag to be inserted or replaced. The value must only be changed when the transmit lines are inactive or during the initialization phase. Bits[15:13] are the User Priority field, Bit 12 is the CFI/DEI field, and Bits[11:0] are the VID field in the VLAN tag. The following list describes the bits of this field: - Bits[15:13]: User Priority - Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) - Bits[11:0]: VLAN Identifier (VID) field of VLAN tag

10.2.12 MAC_Q0_TX_FLOW_CTRL — Offset 70h

The Flow Control register controls the generation and reception of the Control (Pause Command) packets by the Flow control module of the MAC. A Write to a register with the Busy bit set to 1 triggers the Flow Control block to generate a Pause packet. The fields of the control packet are selected as specified in the 802.3x specification, and the Pause Time value from this register is used in the Pause Time field of the control packet. The Busy bit remains set until the control packet is transferred onto the cable. The application must make sure that the Busy bit is cleared before writing to the register.

When the PFCE bit in the MAC_Rx_Flow_Ctrl register is enabled, this register controls the generation of Priority Flow Control (PFC) frames with priorities mapped according to PSRQ0 in the MAC_RxQ_Ctrl2 register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Pause Time (PT):** This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	**Reserved**
7	0h RW	**Disable Zero-Quanta Pause (DZPQ):** When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.
6:4	0h RW	**Pause Low Threshold (PLT):** This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Transmit Flow Control Enable (TFE):** Full-Duplex Mode: In the full-duplex mode, when this bit is set, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. Half-Duplex Mode: In the half-duplex mode, when this bit is set, the MAC enables the backpressure operation. When this bit is reset, the backpressure feature is disabled. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	**Flow Control Busy or Backpressure Activate (FCB_BPA):** This bit initiates a Pause packet in the full-duplex mode and activates the backpressure function in the half-duplex mode if the TFE bit is set. Full-Duplex Mode: In the full-duplex mode, this bit should be read as 1'b0 before writing to this register. To initiate a Pause packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When Pause packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Half-Duplex Mode: When this bit is set (and TFE bit is set) in the half-duplex mode, the MAC asserts the backpressure. During backpressure, when the MAC receives a new packet, the transmitter starts sending a JAM pattern resulting in a collision. This control register bit is logically ORed with the mti_flowctrl_i input signal for the backpressure function. When the MAC is configured for the full-duplex mode, the BPA is automatically disabled. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.

10.2.13 MAC_Q1_TX_FLOW_CTRL — Offset 74h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 74h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Pause Time (PT):** This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	**Reserved**
7	0h RW	**Disable Zero-Quanta Pause (DZPQ):** When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.
6:4	0h RW	**Pause Low Threshold (PLT):** This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.
3:2	0h RO	**Reserved**
1	0h RW	**Transmit Flow Control Enable (TFE):** When this bit is set in full-duplex mode, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	**Flow Control Busy (FCB_BPA):** This bit initiates a PFC packet if the TFE bit is set. To initiate a PFC packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When PFC packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.

10.2.14 MAC_Q2_TX_FLOW_CTRL — Offset 78h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 78h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Pause Time (PT):** This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	**Reserved**
7	0h RW	**Disable Zero-Quanta Pause (DZPQ):** When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.
6:4	0h RW	**Pause Low Threshold (PLT):** This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Transmit Flow Control Enable (TFE):** When this bit is set in full-duplex mode, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	**Flow Control Busy (FCB_BPA):** This bit initiates a PFC packet if the TFE bit is set. To initiate a PFC packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When PFC packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.

10.2.15 MAC_Q3_TX_FLOW_CTRL — Offset 7Ch

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Pause Time (PT):** This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	**Reserved**
7	0h RW	**Disable Zero-Quanta Pause (DZPQ):** When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.

Bit Range	Default & Access	Field Name (ID): Description
6:4	0h RW	**Pause Low Threshold (PLT):** This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.
3:2	0h RO	**Reserved**
1	0h RW	**Transmit Flow Control Enable (TFE):** When this bit is set in full-duplex mode, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	**Flow Control Busy (FCB_BPA):** This bit initiates a PFC packet if the TFE bit is set. To initiate a PFC packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When PFC packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.

10.2.16 MAC_Q4_TX_FLOW_CTRL — Offset 80h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Pause Time (PT):** This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	**Reserved**
7	0h RW	**Disable Zero-Quanta Pause (DZPQ):** When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.
6:4	0h RW	**Pause Low Threshold (PLT):** This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.
3:2	0h RO	**Reserved**
1	0h RW	**Transmit Flow Control Enable (TFE):** When this bit is set in full-duplex mode, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	**Flow Control Busy (FCB_BPA):** This bit initiates a PFC packet if the TFE bit is set. To initiate a PFC packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When PFC packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.

10.2.17 MAC_Q5_TX_FLOW_CTRL — Offset 84h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Pause Time (PT):** This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	**Reserved**
7	0h RW	**Disable Zero-Quanta Pause (DZPQ):** When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.
6:4	0h RW	**Pause Low Threshold (PLT):** This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Transmit Flow Control Enable (TFE):** When this bit is set in full-duplex mode, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	**Flow Control Busy (FCB_BPA):** This bit initiates a PFC packet if the TFE bit is set. To initiate a PFC packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When PFC packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.

10.2.18 MAC_Q6_TX_FLOW_CTRL — Offset 88h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Pause Time (PT):** This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	**Reserved**
7	0h RW	**Disable Zero-Quanta Pause (DZPQ):** When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.

Bit Range	Default & Access	Field Name (ID): Description
6:4	0h RW	**Pause Low Threshold (PLT):** This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.
3:2	0h RO	**Reserved**
1	0h RW	**Transmit Flow Control Enable (TFE):** When this bit is set in full-duplex mode, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	**Flow Control Busy (FCB_BPA):** This bit initiates a PFC packet if the TFE bit is set. To initiate a PFC packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When PFC packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.

10.2.19 MAC_Q7_TX_FLOW_CTRL — Offset 8Ch

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Pause Time (PT):** This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	**Reserved**
7	0h RW	**Disable Zero-Quanta Pause (DZPQ):** When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.
6:4	0h RW	**Pause Low Threshold (PLT):** This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.
3:2	0h RO	**Reserved**
1	0h RW	**Transmit Flow Control Enable (TFE):** When this bit is set in full-duplex mode, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	**Flow Control Busy (FCB_BPA):** This bit initiates a PFC packet if the TFE bit is set. To initiate a PFC packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When PFC packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.

10.2.20 MAC_RX_FLOW_CTRL — Offset 90h

The Receive Flow Control register controls the pausing of MAC Transmit based on the received Pause packet.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**Priority Based Flow Control Enable (PFCE):** When this bit is set, it enables generation and reception of priority-based flow control (PFC) packets. When this bit is reset, it enables generation and reception of 802.3x Pause control packets. 0x0 (DISABLE): Priority Based Flow Control is disabled. 0x1 (ENABLE): Priority Based Flow Control is enabled.
7:2	0h RO	**Reserved**
1	0h RW	**Unicast Pause Packet Detect (UP):** A pause packet is processed when it has the unique multicast address specified in the IEEE 802.3. When this bit is set, the MAC can also detect Pause packets with unicast address of the station. This unicast address should be as specified in MAC_Address0_High and MAC_Address0_Low. When this bit is reset, the MAC only detects Pause packets with unique multicast address. Note: The MAC does not process a Pause packet if the multicast address is different from the unique multicast address. This is also applicable to the received PFC packet when the Priority Flow Control (PFC) is enabled. The unique multicast address (0x01_80_C2_00_00_01) is as specified in IEEE 802.1 Qbb-2011. 0x0 (DISABLE): Unicast Pause Packet Detect disabled. 0x1 (ENABLE): Unicast Pause Packet Detect enabled.
0	0h RW	**Receive Flow Control Enable (RFE):** When this bit is set and the MAC is operating in full-duplex mode, the MAC decodes the received Pause packet and disables its transmitter for a specified (Pause) time. When this bit is reset or the MAC is operating in half-duplex mode, the decode function of the Pause packet is disabled. When PFC is enabled, flow control is enabled for PFC packets. The MAC decodes the received PFC packet and disables the Transmit queue, with matching priorities, for a duration of received Pause time. 0x0 (DISABLE): Receive Flow Control is disabled. 0x1 (ENABLE): Receive Flow Control is enabled.

10.2.21 MAC_RXQ_CTRL4 — Offset 94h

The Receive Queue Control 4 register controls the routing of unicast and multicast packets that fail the Destination or Source address filter to the Rx queues.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:17	0h RW	**VLAN Tag Filter Fail Packets Queue (VFFQ):** This field holds the Rx queue number to which the tagged packets failing the Destination or Source Address filter (and UFFQE/MFFQE not enabled) or failing the VLAN tag filter must be routed to. This field is valid only when the VFFQE bit is set.
16	0h RW	**VLAN Tag Filter Fail Packets Queuing Enable (VFFQE):** When this bit is set, the tagged packets which fail the Destination or Source address filter or fail the VLAN tag filter, are routed to the Rx Queue Number programmed in the VFFQ. When this bit is reset, the tagged packets which fail the Destination or Source address filter or fail the VLAN tag filter are routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set. 0x0 (DISABLE): VLAN tag Filter Fail Packets Queuing is disabled. 0x1 (ENABLE): VLAN tag Filter Fail Packets Queuing is enabled.
15:12	0h RO	**Reserved**
11:9	0h RW	**Multicast Address Filter Fail Packets Queue. (MFFQ):** This field holds the Rx queue number to which the Multicast packets failing the Destination or Source Address filter are routed to. This field is valid only when the MFFQE bit is set.
8	0h RW	**Multicast Address Filter Fail Packets Queuing Enable. (MFFQE):** When this bit is set, the Multicast packets which fail the Destination or Source address filter is routed to the Rx Queue Number programmed in the MFFQ. When this bit is reset, the Multicast packets which fail the Destination or Source address filter is routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set. 0x0 (DISABLE): Multicast Address Filter Fail Packets Queuing is disabled. 0x1 (ENABLE): Multicast Address Filter Fail Packets Queuing is enabled.
7:4	0h RO	**Reserved**
3:1	0h RW	**Unicast Address Filter Fail Packets Queue. (UFFQ):** This field holds the Rx queue number to which the Unicast packets failing the Destination or Source Address filter are routed to. This field is valid only when the UFFQE bit is set.
0	0h RW	**Unicast Address Filter Fail Packets Queuing Enable. (UFFQE):** When this bit is set, the Unicast packets which fail the Destination or Source address filter is routed to the Rx Queue Number programmed in the UFFQ. When this bit is reset, the Unicast packets which fail the Destination or Source address filter is routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set. 0x0 (DISABLE): Unicast Address Filter Fail Packets Queuing is disabled. 0x1 (ENABLE): Unicast Address Filter Fail Packets Queuing is enabled.

10.2.22 MAC_TXQ_PRTY_MAP0 — Offset 98h

The Transmit Queue Priority Mapping 0 register contains the priority values assigned to Tx Queue 0 through Tx Queue 3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**Priorities Selected in Transmit Queue 3 (PSTQ3):** This bit is similar to the PSTQ0 bit.
23:16	00h RW	**Priorities Selected in Transmit Queue 2 (PSTQ2):** This bit is similar to the PSTQ0 bit.
15:8	00h RW	**Priorities Selected in Transmit Queue 1 (PSTQ1):** This bit is similar to the PSTQ0 bit.
7:0	00h RW	**Priorities Selected in Transmit Queue 0 (PSTQ0):** This field holds the priorities assigned to Tx Queue 0 by the software. This field determines if Tx Queue 0 should be blocked from transmitting specified pause time when a PFC packet is received with priorities matching the priorities programmed in this field. If the content of this field is not mutually exclusive to corresponding fields of other Transmit queues, that is, same priority is mapped to multiple Tx queues, the MAC blocks all queues with matching priority for specified time.

10.2.23 MAC_TXQ_PRTY_MAP1 — Offset 9Ch

The Transmit Queue Priority Mapping 1 register contains the priority values assigned to Tx Queue 4 through Tx Queue 7.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**Priorities Selected in Transmit Queue 7 (PSTQ7):** This bit is similar to the PSTQ4 bit.
23:16	00h RW	**Priorities Selected in Transmit Queue 6 (PSTQ6):** This bit is similar to the PSTQ4 bit.
15:8	00h RW	**Priorities Selected in Transmit Queue 5 (PSTQ5):** This bit is similar to the PSTQ4 bit.
7:0	00h RW	**Priorities Selected in Transmit Queue 4 (PSTQ4):** This field holds the priorities assigned to Tx Queue 4 by the software. This field determines if Tx Queue 4 should be blocked from transmitting specified pause time when a PFC packet is received with priorities matching the priorities programmed in this field. If the content of this field is not mutually exclusive to corresponding fields of other Transmit queues, that is, same priority is mapped to multiple Tx queues, the MAC blocks all queues with matching priority for specified time.

10.2.24 MAC_RXQ_CTRL0 — Offset A0h

The Receive Queue Control 0 register controls the queue management in the MAC Receiver.

Note: In multiple Rx queues configuration, all the queues are disabled by default. Enable the Rx queue by programming the corresponding field in this register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:14	0h RW	**Receive Queue 7 Enable (RXQ7EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
13:12	0h RW	**Receive Queue 6 Enable (RXQ6EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
11:10	0h RW	**Receive Queue 5 Enable (RXQ5EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
9:8	0h RW	**Receive Queue 4 Enable (RXQ4EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
7:6	0h RW	**Receive Queue 3 Enable (RXQ3EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Receive Queue 2 Enable (RXQ2EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
3:2	0h RW	**Receive Queue 1 Enable (RXQ1EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
1:0	0h RW	**Receive Queue 0 Enable (RXQ0EN):** This field indicates whether Rx Queue 0 is enabled for AV or DCB. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.

10.2.25 MAC_RXQ_CTRL1 — Offset A4h

The Receive Queue Control 1 register controls the routing of multicast, broadcast, AV, DCB, and untagged packets to the Rx queues.

Type	Size	Offset	Default
MMIO	32 bit	BAR + A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**OMCBCQ:** 0x0 (DISABLE): overriding MCBCQ priority disabled. 0x1 (ENABLE): overriding MCBCQ priority enabled.
27	0h RO	**Reserved**
26:24	0h RW	**Frame Preemption Residue Queue (FPRQ):** This field holds the Rx queue number to which the residual preemption frames must be forwarded. Preemption frames that are tagged and pass the SA/DA/VLAN filtering are routed based on PSRQ and all other frames are treated as residual frames and is routed to the queue number mentioned in this field. The Queue-0 is used as a default queue for express frames, so this field cannot be programmed to a value 0.

Bit Range	Default & Access	Field Name (ID): Description
23:22	0h RW	**Tagged PTP over Ethernet Packets Queuing Control. (TPQC):** This field controls the routing of the VLAN Tagged PTPoE packets. The following programmable options are allowed. - 2'b00: VLAN Tagged PTPoE packets are routed as generic VLAN Tagged packet (based on PSRQ for only non-AV enabled Rx Queues). - 2'b01: VLAN Tagged PTPoE packets are routed to Rx Queue specified by PTPQ field (That Rx Queue can be enabled for AV or non-AV traffic). - 2'b10: VLAN Tagged PTPoE packets are routed to only AV enabled Rx Queues based on PSRQ. - 2'b11: Reserved
21	0h RW	**Tagged AV Control Packets Queuing Enable. (TACPQE):** When set, the MAC routes the received Tagged AV Control packets to the Rx queue specified by AVCPQ field. When reset, the MAC routes the received Tagged AV Control packets based on the tag priority matching the PSRQ fields in MAC_RxQ_Ctrl2 and MAC_RxQ_Ctrl3 registers. 0x0 (DISABLE): Tagged AV Control Packets Queuing is disabled. 0x1 (ENABLE): Tagged AV Control Packets Queuing is enabled.
20	0h RW	**Multicast and Broadcast Queue Enable (MCBCQEN):** This bit specifies that Multicast or Broadcast packets routing to the Rx Queue is enabled and the Multicast or Broadcast packets must be routed to Rx Queue specified in MCBCQ field. 0x0 (DISABLE): Multicast and Broadcast Queue is disabled. 0x1 (ENABLE): Multicast and Broadcast Queue is enabled.
19	0h RO	**Reserved**
18:16	0h RW	**Multicast and Broadcast Queue (MCBCQ):** This field specifies the Rx Queue onto which Multicast or Broadcast Packets are routed. Any Rx Queue enabled for Generic/DCB/AV traffic can be used to route the Multicast or Broadcast Packets. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.
15	0h RO	**Reserved**
14:12	0h RW	**Untagged Packet Queue (UPQ):** This field indicates the Rx Queue to which Untagged Packets are to be routed. Any Rx Queue enabled for Generic/DCB/AV traffic can be used to route the Untagged Packets. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.
11	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**DCB Control Packets Queue (DCBCPQ):** This field specifies the Rx queue on which the received DCB control packets are routed. The DCB data packets are routed based on the PSRQ field of the Transmit Flow Control Register of corresponding queue. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.
7	0h RO	**Reserved**
6:4	0h RW	**PTP Packets Queue (PTPQ):** This field specifies the Rx queue on which the PTP packets sent over the Ethernet payload (not over IPv4 or IPv6) are routed. When the AV8021ASMEN bit of MAC_Timestamp_Control register is set, only untagged PTP over Ethernet packets are routed on an Rx Queue. If the bit is not set, then based on programming of TPQC field, both tagged and untagged PTPoE packets can be routed to this Rx Queue. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.
3	0h RO	**Reserved**
2:0	0h RW	**AV Untagged Control Packets Queue (AVCPQ):** This field specifies the Receive queue on which the received AV tagged and untagged control packets are routed. The AV tagged (when TACPQE bit is set) and untagged control packets are routed to Receive queue specified by this field. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.

10.2.26 MAC_RXQ_CTRL2 — Offset A8h

This register controls the routing of tagged packets based on the USP (user Priority) field of the received packets to the RxQueues 0 to 3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**Priorities Selected in the Receive Queue 3 (PSRQ3):** This field decides the priorities assigned to Rx Queue 3. All packets with priorities that match the values set in this field are routed to Rx Queue 3. For example, if PSRQ3[6, 3] are set, packets with USP field equal to 3 or 6 are routed to Rx Queue 3. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 3 crosses the flow control threshold settings.
23:16	00h RW	**Priorities Selected in the Receive Queue 2 (PSRQ2):** This field decides the priorities assigned to Rx Queue 2. All packets with priorities that match the values set in this field are routed to Rx Queue 2. For example, if PSRQ2[1, 0] are set, packets with USP field equal to 1 or 0 are routed to Rx Queue 2. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 2 crosses the flow control threshold settings.
15:8	00h RW	**Priorities Selected in the Receive Queue 1 (PSRQ1):** This field decides the priorities assigned to Rx Queue 1. All packets with priorities that match the values set in this field are routed to Rx Queue 1. For example, if PSRQ1[4] is set, packets with USP field equal to 4 are routed to Rx Queue 1. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 1 crosses the flow control threshold settings.
7:0	00h RW	**Priorities Selected in the Receive Queue 0 (PSRQ0):** This field decides the priorities assigned to Rx Queue 0. All packets with priorities that match the values set in this field are routed to Rx Queue 0. For example, if PSRQ0[5] is set, packets with USP field equal to 5 are routed to Rx Queue 0. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 0 crosses the flow control threshold settings.

10.2.27 MAC_RXQ_CTRL3 — Offset ACh

This register controls the routing of tagged packets based on the USP (user Priority) field of the received packets to the RxQueues 4 to 7.

Type	Size	Offset	Default
MMIO	32 bit	BAR + ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**Priorities Selected in the Receive Queue 7 (PSRQ7):** This field decides the priorities assigned to Rx Queue 7. All packets with priorities that match the values set in this field are routed to Rx Queue 7. For example, if PSRQ7[7, 4] are set, packets with USP field equal to 7 or 4 are routed to Rx Queue 7. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 7 crosses the flow control threshold settings.
23:16	00h RW	**Priorities Selected in the Receive Queue 6 (PSRQ6):** This field decides the priorities assigned to Rx Queue 6. All packets with priorities that match the values set in this field are routed to Rx Queue 6. For example, if PSRQ6[5] are set, packets with USP field equal to 5 are routed to Rx Queue 6. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 6 crosses the flow control threshold settings.
15:8	00h RW	**Priorities Selected in the Receive Queue 5 (PSRQ5):** This field decides the priorities assigned to Rx Queue 5. All packets with priorities that match the values set in this field are routed to Rx Queue 5. For example, if PSRQ5[6] is set, packets with USP field equal to 6 are routed to Rx Queue 5. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 5 crosses the flow control threshold settings.
7:0	00h RW	**Priorities Selected in the Receive Queue 4 (PSRQ4):** This field decides the priorities assigned to Rx Queue 4. All packets with priorities that match the values set in this field are routed to Rx Queue 4. For example, if PSRQ4[7:4] is set, packets with USP field equal to 7, 6, 5, or 4 are routed to Rx Queue 4. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 4 crosses the flow control threshold settings.

10.2.28 MAC_INTERRUPT_STATUS — Offset B0h

The Interrupt Status register contains the status of interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**MMC FPE Receive Interrupt Status (MFRIS):** This bit is set high when an interrupt is generated in the MMC FPE Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option along with FPE support. 0x0 (INACTIVE): MMC FPE Receive Interrupt status not active. 0x1 (ACTIVE): MMC FPE Receive Interrupt status active.
19	0h RO	**MMC FPE Transmit Interrupt Status (MFTIS):** This bit is set high when an interrupt is generated in the MMC FPE Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option along with FPE support. 0x0 (INACTIVE): MMC FPE Transmit Interrupt status not active. 0x1 (ACTIVE): MMC FPE Transmit Interrupt status active.
18	0h RO	**MDIO Interrupt Status (MDIOIS):** This bit indicates an interrupt event after the completion of MDIO operation. To reset this bit, the application has to read this bit/Write 1 to this bit when RCWE bit of MAC_CSR_SW_Ctrl register is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): MDIO Interrupt status not active. 0x1 (ACTIVE): MDIO Interrupt status active.
17	0h RO	**Frame Preemption Interrupt Status (FPEIS):** This bit indicates an interrupt event during the operation of Frame Preemption (Bits[19:16] of MAC_FPE_CTRL_STS register is set). To reset this bit, the application must clear the event in MAC_FPE_CTRL_STS that has caused the Interrupt. 0x0 (INACTIVE): Frame Preemption Interrupt status not active. 0x1 (ACTIVE): Frame Preemption Interrupt status active.
16	0h RO	**Reserved**
15	0h RO	**GPI Interrupt Status (GPIIS):** When the GPIO feature is enabled, this bit is set when any active event (LL or LH) occurs on the GPIS field of the MAC_GPIO_Status register and the corresponding GPIE bit is enabled in the MAC_GPIO_Control register. This bit is cleared on reading lane 0 (GPIS) of the MAC_GPIO_Status register. 0x0 (INACTIVE): GPI Interrupt status not active. 0x1 (ACTIVE): GPI Interrupt status active.
14	0h RO	**Receive Status Interrupt (RXSTSIS):** This bit indicates the status of received packets. This bit is set when the RWT bit is set in the MAC_Rx_Tx_Status register. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register. 0x0 (INACTIVE): Receive Interrupt status not active. 0x1 (ACTIVE): Receive Interrupt status active.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**Transmit Status Interrupt (TXSTSIS):** This bit indicates the status of transmitted packets. This bit is set when any of the following bits is set in the MAC_Rx_Tx_Status register: - Excessive Collision (EXCOL) - Late Collision (LCOL) - Excessive Deferral (EXDEF) - Loss of Carrier (LCARR) - No Carrier (NCARR) - Jabber Timeout (TJT) This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register. 0x0 (INACTIVE): Transmit Interrupt status not active. 0x1 (ACTIVE): Transmit Interrupt status active.
12	0h RO	**Timestamp Interrupt Status (TSIS):** If the Timestamp feature is enabled, this bit is set when any of the following conditions is true: - The system time value is equal to or exceeds the value specified in the Target Time High and Low registers. - There is an overflow in the Seconds register. - The Target Time Error occurred, that is, programmed target time already elapsed. If the Auxiliary Snapshot feature is enabled, this bit is set when the auxiliary snapshot trigger is asserted. In configurations other than EQOS_CORE, when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and Mac_TxTimestamp_Status_Seconds registers. When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers, for PTO generated Delay Request and Pdelay request packets. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Timestamp_Status register. 0x0 (INACTIVE): Timestamp Interrupt status not active. 0x1 (ACTIVE): Timestamp Interrupt status active.
11	0h RO	**MMC Receive Checksum Offload Interrupt Status (MMCRXIPIS):** This bit is set high when an interrupt is generated in the MMC Receive Checksum Offload Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) and Enable Receive TCP/IP Checksum Check options. 0x0 (INACTIVE): MMC Receive Checksum Offload Interrupt status not active. 0x1 (ACTIVE): MMC Receive Checksum Offload Interrupt status active.
10	0h RO	**MMC Transmit Interrupt Status (MMCTXIS):** This bit is set high when an interrupt is generated in the MMC Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. 0x0 (INACTIVE): MMC Transmit Interrupt status not active. 0x1 (ACTIVE): MMC Transmit Interrupt status active.
9	0h RO	**MMC Receive Interrupt Status (MMCRXIS):** This bit is set high when an interrupt is generated in the MMC Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. 0x0 (INACTIVE): MMC Receive Interrupt status not active. 0x1 (ACTIVE): MMC Receive Interrupt status active.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**MMC Interrupt Status (MMCIS):** This bit is set high when Bit 11, Bit 10, or Bit 9 is set high. This bit is cleared only when all these bits are low. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. 0x0 (INACTIVE): MMC Interrupt status not active. 0x1 (ACTIVE): MMC Interrupt status active.
7:6	0h RO	**Reserved**
5	0h RO	**LPI Interrupt Status (LPIIS):** When the Energy Efficient Ethernet feature is enabled, this bit is set for any LPI state entry or exit in the MAC Transmitter or Receiver. This bit is cleared when the corresponding interrupt source bit of MAC_LPI_Control_Status register is read (or corresponding interrupt source bit of MAC_LPI_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). 0x0 (INACTIVE): LPI Interrupt status not active. 0x1 (ACTIVE): LPI Interrupt status active.
4	0h RO	**PMT Interrupt Status (PMTIS):** This bit is set when a Magic packet or Wake-on-LAN packet is received in the power-down mode (RWKPRCVD and MGKPRCVD bits in MAC_PMT_Control_Status register). This bit is cleared when corresponding interrupt source bit are cleared because of a Read operation to the MAC_PMT_Control_Status register (or corresponding interrupt source bit of MAC_PMT_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the Enable Power Management option. 0x0 (INACTIVE): PMT Interrupt status not active. 0x1 (ACTIVE): PMT Interrupt status active.
3	0h RO	**PHY Interrupt (PHYIS):** This bit is set when rising edge is detected on the phy_intr_i input. This bit is cleared when this register is read (or this bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). 0x0 (INACTIVE): PHY Interrupt not detected. 0x1 (ACTIVE): PHY Interrupt detected.
2:1	0h RO	**Reserved**
0	0h RO	**RGMII or SMII Interrupt Status (RGSMIIIS):** This bit is set because of any change in value of the Link Status of RGMII or SMII interface (LNKSTS bit in MAC_PHYIF_Control_Status register). This bit is cleared when the MAC_PHYIF_Control_Status register is read (or LNKSTS bit of MAC_PHYIF_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the optional RGMII or SMII PHY interface. 0x0 (INACTIVE): RGMII or SMII Interrupt Status is not active. 0x1 (ACTIVE): RGMII or SMII Interrupt Status is active.

10.2.29 MAC_INTERRUPT_ENABLE — Offset B4h

The Interrupt Enable register contains the masks for generating the interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW	**MDIO Interrupt Enable (MDIOIE):** When this bit is set, it enables the assertion of the interrupt when MDIOIS field is set in the MAC_Interrupt_Status register. 0x0 (DISABLE): MDIO Interrupt is disabled. 0x1 (ENABLE): MDIO Interrupt is enabled.
17	0h RW	**Frame Preemption Interrupt Enable (FPEIE):** When this bit is set, it enables the assertion of the interrupt when FPEIS field is set in the MAC_Interrupt_Status register. 0x0 (DISABLE): Frame Preemption Interrupt is disabled. 0x1 (ENABLE): Frame Preemption Interrupt is enabled.
16:15	0h RO	**Reserved**
14	0h RW	**Receive Status Interrupt Enable (RXSTSIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of RXSTSIS bit in the MAC_Interrupt_Status register. 0x0 (DISABLE): Receive Status Interrupt is disabled. 0x1 (ENABLE): Receive Status Interrupt is enabled.
13	0h RW	**Transmit Status Interrupt Enable (TXSTSIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of TXSTSIS bit in the MAC_Interrupt_Status register. 0x0 (DISABLE): Timestamp Status Interrupt is disabled. 0x1 (ENABLE): Timestamp Status Interrupt is enabled.
12	0h RW	**Timestamp Interrupt Enable (TSIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of TSIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): Timestamp Interrupt is disabled. 0x1 (ENABLE): Timestamp Interrupt is enabled.
11:6	0h RO	**Reserved**
5	0h RW	**LPI Interrupt Enable (LPIIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of LPIIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): LPI Interrupt is disabled. 0x1 (ENABLE): LPI Interrupt is enabled.
4	0h RW	**PMT Interrupt Enable (PMTIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of PMTIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): PMT Interrupt is disabled. 0x1 (ENABLE): PMT Interrupt is enabled.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**PHY Interrupt Enable (PHYIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of PHYIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): PHY Interrupt is disabled. 0x1 (ENABLE): PHY Interrupt is enabled.
2:1	0h RO	**Reserved**
0	0h RW	**RGMII or SMII Interrupt Enable (RGSMIIIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of RGSMIIIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): RGMII or SMII Interrupt is disabled. 0x1 (ENABLE): RGMII or SMII Interrupt is enabled.

10.2.30 MAC_RX_TX_STATUS — Offset B8h

The Receive Transmit Status register contains the Receive and Transmit Error status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RO	**Receive Watchdog Timeout (RWT):** This bit is set when a packet with length greater than 2,048 bytes is received (10,240 bytes when Jumbo Packet mode is enabled) and the WD bit is reset in the MAC_Configuration register. This bit is set when a packet with length greater than 16,383 bytes is received and the WD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No receive watchdog timeout. 0x1 (ACTIVE): Receive watchdog timed out.
7:6	0h RO	**Reserved**
5	0h RO	**Excessive Collisions (EXCOL):** When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the transmission aborted after 16 successive collisions while attempting to transmit the current packet. If the DR bit is set in the MAC_Configuration register, this bit is set after the first collision and the packet transmission is aborted. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No collision. 0x1 (ACTIVE): Excessive collision is sensed.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**Late Collision (LCOL):** When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the packet transmission aborted because a collision occurred after the collision window (64 bytes including Preamble in MII mode; 512 bytes including Preamble and Carrier Extension in GMII mode). This bit is not valid if the Underflow error occurs. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No collision. 0x1 (ACTIVE): Late collision is sensed.
3	0h RO	**Excessive Deferral (EXDEF):** When the DTXSTS bit is set in the MTL_Operation_Mode register and the DC bit is set in the MAC_Configuration register, this bit indicates that the transmission ended because of excessive deferral of over 24,288 bit times (155,680 in 1000/2500 Mbps mode or when Jumbo packet is enabled). Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No Excessive deferral. 0x1 (ACTIVE): Excessive deferral.
2	0h RO	**Loss of Carrier (LCARR):** When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the loss of carrier occurred during packet transmission, that is, the phy_crs_i signal was inactive for one or more transmission clock periods during packet transmission. This bit is valid only for packets transmitted without collision. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Carrier is present. 0x1 (ACTIVE): Loss of carrier.
1	0h RO	**No Carrier (NCARR):** When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the carrier signal from the PHY is not present at the end of preamble transmission. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Carrier is present. 0x1 (ACTIVE): No carrier.
0	0h RO	**Transmit Jabber Timeout (TJT):** This bit indicates that the Transmit Jabber Timer expired which happens when the packet size exceeds 2,048 bytes (10,240 bytes when the Jumbo packet is enabled) and JD bit is reset in the MAC_Configuration register. This bit is set when the packet size exceeds 16,383 bytes and the JD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No Transmit Jabber Timeout. 0x1 (ACTIVE): Transmit Jabber Timeout occurred.

10.2.31 MAC_PMT_CONTROL_STATUS — Offset C0h

The PMT Control and Status Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Remote Wake-Up Packet Filter Register Pointer Reset (RWKFILTRST):** When this bit is set, the remote wake-up packet filter register pointer is reset to 3'b000. It is automatically cleared after 1 clock cycle. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Remote Wake-Up Packet Filter Register Pointer is not Reset. 0x1 (ENABLE): Remote Wake-Up Packet Filter Register Pointer is Reset.
30:29	0h RO	**Reserved**
28:24	00h RO	**Remote Wake-up FIFO Pointer (RWKPTR):** This field gives the current value (0 to 7, 15, or 31 when 4, 8, or 16 Remote Wake-up Packet Filters are selected) of the Remote Wake-up Packet Filter register pointer. When the value of this pointer is equal to maximum for the selected number of Remote Wake-up Packet Filters, the contents of the Remote Wake-up Packet Filter Register are transferred to the clk_rx_i domain when a Write occurs to that register.
23:11	0h RO	**Reserved**
10	0h RW	**Remote Wake-up Packet Forwarding Enable (RWKPFE):** When this bit is set along with RWKPKTEN, the MAC receiver drops all received frames until it receives the expected Wake-up frame. All frames after that event including the received wake-up frame are forwarded to application. This bit is then self-cleared on receiving the wake-up packet. The application can also clear this bit before the expected wake-up frame is received. In such cases, the MAC reverts to the default behavior where packets received are forwarded to the application. This bit must only be set when RWKPKTEN is set high and PWRDWN is set low. The setting of this bit has no effect when PWRDWN is set high. Note: If Magic Packet Enable and Wake-Up Frame Enable are both set along with setting of this bit and Magic Packet is received prior to wake-up frame, this bit is self-cleared on receiving Magic Packet, the received Magic packet is dropped, and all frames after received Magic Packet are forwarded to application. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Remote Wake-up Packet Forwarding is disabled. 0x1 (ENABLE): Remote Wake-up Packet Forwarding is enabled.
9	0h RW	**Global Unicast (GLBLUCAST):** When this bit set, any unicast packet filtered by the MAC (DAF) address recognition is detected as a remote wake-up packet. 0x0 (DISABLE): Global unicast is disabled. 0x1 (ENABLE): Global unicast is enabled.
8:7	0h RO	**Reserved**
6	0h RO	**Remote Wake-Up Packet Received (RWKPRCVD):** When this bit is set, it indicates that the power management event is generated because of the reception of a remote wake-up packet. This bit is cleared when this register is read. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Remote wake-up packet is received. 0x1 (ACTIVE): Remote wake-up packet is received.
5	0h RO	**Magic Packet Received (MGKPRCVD):** When this bit is set, it indicates that the power management event is generated because of the reception of a magic packet. This bit is cleared when this register is read. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No Magic packet is received. 0x1 (ACTIVE): Magic packet is received.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RO	**Reserved**
2	0h RW	**Remote Wake-Up Packet Enable (RWKPKTEN):** When this bit is set, a power management event is generated when the MAC receives a remote wake-up packet. 0x0 (DISABLE): Remote wake-up packet is disabled. 0x1 (ENABLE): Remote wake-up packet is enabled.
1	0h RW	**Magic Packet Enable (MGKPKTEN):** When this bit is set, a power management event is generated when the MAC receives a magic packet. 0x0 (DISABLE): Magic Packet is disabled. 0x1 (ENABLE): Magic Packet is enabled.
0	0h RW	**Power Down (PWRDWN):** When this bit is set, the MAC receiver drops all received packets until it receives the expected magic packet or remote wake-up packet. This bit is then self-cleared and the power-down mode is disabled. The software can clear this bit before the expected magic packet or remote wake-up packet is received. The packets received by the MAC after this bit is cleared are forwarded to the application. This bit must only be set when the Magic Packet Enable, Global Unicast, or Remote Wake-Up Packet Enable bit is set high. Note: You can gate-off the CSR clock during the power-down mode. However, when the CSR clock is gated-off, you cannot perform any read or write operations on this register. Therefore, the Software cannot clear this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Power down is disabled. 0x1 (ENABLE): Power down is enabled.

10.2.32 MAC_RWK_PACKET_FILTER — Offset C4h

The TSN-GbE implements a filter lookup table programmed through the MAC_RWK_Packet_Filter register in which CRC, offset, and byte mask of the pattern embedded in the remote wakeup packet, and the filter-operation commands are programmed.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**RWK Packet Filter (WKUPFRMFTR):** This field contains the various controls of RWK Packet filter.

10.2.33 MAC_LPI_CONTROL_STATUS — Offset D0h

The LPI Control and Status Register controls the LPI functions and provides the LPI interrupt status. The status bits are cleared when this register is read.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW	**LPI Tx Clock Stop Enable (LPITCSE):** When this bit is set, the MAC indicates that the Tx clock to MAC can be stopped. When this bit is reset, the MAC does not indicate that the Tx clock to MAC can be stopped after it enters Tx LPI mode. If RGMII Interface is selected, the Tx clock is required for transmitting the LPI pattern. The Tx Clock cannot be gated and so the LPITCSE bit cannot be programmed. 0x0 (DISABLE): LPI Tx Clock Stop is disabled. 0x1 (ENABLE): LPI Tx Clock Stop is enabled.
20	0h RW	**LPI Timer Enable (LPIATE):** This bit controls the automatic entry of the MAC Transmitter into and exit out of the LPI state. When LPIATE, LPITXA and LPIEN bits are set, the MAC Transmitter enters LPI state only when the complete MAC TX data path is IDLE for a period indicated by the MAC_LPI_Entry_Timer register. After entering LPI state, if the data path becomes non-IDLE (due to a new packet being accepted for transmission), the Transmitter exits LPI state but does not clear LPIEN bit. This enables the re-entry into LPI state when it is IDLE again. When LPIATE is 0, the LPI Auto timer is disabled and MAC Transmitter enters LPI state based on the settings of LPITXA and LPIEN bit descriptions. 0x0 (DISABLE): LPI Timer is disabled. 0x1 (ENABLE): LPI Timer is enabled.
19	0h RW	**LPI Tx Automate (LPITXA):** This bit controls the behavior of the MAC when it is entering or coming out of the LPI mode on the Transmit side. This bit is not functional in the EQOS-CORE configurations in which the Tx clock gating is done during the LPI mode. If the LPITXA and LPIEN bits are set to 1, the MAC enters the LPI mode only after all outstanding packets (in the core) and pending packets (in the application interface) have been transmitted. The MAC comes out of the LPI mode when the application sends any packet for transmission or the application issues a Tx FIFO Flush command. In addition, the MAC automatically clears the LPIEN bit when it exits the LPI state. If Tx FIFO Flush is set in the FTQ bit of MTL_TxQ0_Operation_Mode register, when the MAC is in the LPI mode, it exits the LPI mode. When this bit is 0, the LPIEN bit directly controls behavior of the MAC when it is entering or coming out of the LPI mode. 0x0 (DISABLE): LPI Tx Automate is disabled. 0x1 (ENABLE): LPI Tx Automate is enabled.
18	0h RW	**PHY Link Status Enable (PLSEN):** This bit enables the link status received on the RGMII, SGMII, or SMII Receive paths to be used for activating the LPI LS TIMER. When this bit is set, the MAC uses the link-status bits of the MAC_PHYIF_Control_Status register and the PLS bit for the LPI LS Timer trigger. When this bit is reset, the MAC ignores the link-status bits of the MAC_PHYIF_Control_Status register and takes only the PLS bit. 0x0 (DISABLE): PHY Link Status is disabled. 0x1 (ENABLE): PHY Link Status is enabled.
17	0h RW	**PHY Link Status (PLS):** This bit indicates the link status of the PHY. The MAC Transmitter asserts the LPI pattern only when the link status is up (OKAY) at least for the time indicated by the LPI LS TIMER. When this bit is set, the link is considered to be okay (UP) and when this bit is reset, the link is considered to be down. 0x0 (DISABLE): link is down. 0x1 (ENABLE): link is okay (UP).

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**LPI Enable (LPIEN):** When this bit is set, it instructs the MAC Transmitter to enter the LPI state. When this bit is reset, it instructs the MAC to exit the LPI state and resume normal transmission. This bit is cleared when the LPITXA bit is set and the MAC exits the LPI state because of the arrival of a new packet for transmission. 0x0 (DISABLE): LPI state is disabled. 0x1 (ENABLE): LPI state is enabled.
15:10	0h RO	**Reserved**
9	0h RO	**Receive LPI State (RLPIST):** When this bit is set, it indicates that the MAC is receiving the LPI pattern on the GMII or MII interface. 0x0 (INACTIVE): Receive LPI state not detected. 0x1 (ACTIVE): Receive LPI state detected.
8	0h RO	**Transmit LPI State (TLPIST):** When this bit is set, it indicates that the MAC is transmitting the LPI pattern on the GMII or MII interface. 0x0 (INACTIVE): Transmit LPI state not detected. 0x1 (ACTIVE): Transmit LPI state detected.
7:4	0h RO	**Reserved**
3	0h RO	**Receive LPI Exit (RLPIEX):** When this bit is set, it indicates that the MAC Receiver has stopped receiving the LPI pattern on the GMII or MII interface, exited the LPI state, and resumed the normal reception. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Note: This bit might not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock. 0x0 (INACTIVE): Receive LPI exit not detected. 0x1 (ACTIVE): Receive LPI exit detected.
2	0h RO	**Receive LPI Entry (RLPIEN):** When this bit is set, it indicates that the MAC Receiver has received an LPI pattern and entered the LPI state. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Note: This bit might not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock. 0x0 (INACTIVE): Receive LPI entry not detected. 0x1 (ACTIVE): Receive LPI entry detected.
1	0h RO	**Transmit LPI Exit (TLPIEX):** When this bit is set, it indicates that the MAC transmitter exited the LPI state after the application cleared the LPIEN bit and the LPI TW Timer has expired. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). 0x0 (INACTIVE): Transmit LPI exit not detected. 0x1 (ACTIVE): Transmit LPI exit detected.
0	0h RO	**Transmit LPI Entry (TLPIEN):** When this bit is set, it indicates that the MAC Transmitter has entered the LPI state because of the setting of the LPIEN bit. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). 0x0 (INACTIVE): Transmit LPI entry not detected. 0x1 (ACTIVE): Transmit LPI entry detected.

10.2.34 MAC_LPI_TIMERS_CONTROL — Offset D4h

The LPI Timers Control register controls the timeout values in the LPI states. It specifies the time for which the MAC transmits the LPI pattern and also the time for which the MAC waits before resuming the normal transmission.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D4h	03E80000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:16	3E8h RW	**LPI LS Timer (LST):** This field specifies the minimum time (in milliseconds) for which the link status from the PHY should be up (OKAY) before the LPI pattern can be transmitted to the PHY. The MAC does not transmit the LPI pattern even when the LPIEN bit is set unless the LPI LS Timer reaches the programmed terminal count. The default value of the LPI LS Timer is 1000 (1 sec) as defined in the IEEE standard.
15:0	0000h RW	**LPI TW Timer (TWT):** This field specifies the minimum time (in microseconds) for which the MAC waits after it stops transmitting the LPI pattern to the PHY and before it resumes the normal transmission. The TLPIEX status bit is set after the expiry of this timer.

10.2.35 MAC_LPI_ENTRY_TIMER — Offset D8h

This register controls the Tx LPI entry timer. This counter is enabled only when bit[20](LPITE) bit of MAC_LPI_Control_Status is set to 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:3	00000h RW	**LPI Entry Timer (LPIET):** This field specifies the time in microseconds the MAC waits to enter LPI mode, after it has transmitted all the frames. This field is valid and used only when LPITE and LPITXA are set to 1. Bits [2:0] are read-only so that the granularity of this timer is in steps of 8 micro-seconds.
2:0	0h RO	**Reserved**

10.2.36 MAC_1US_TIC_COUNTER — Offset DCh

This register controls the generation of the Reference time (1 microsecond tic) for all the LPI timers. This timer has to be programmed by the software initially.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DCh	00000063h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	063h RW	**1US TIC Counter (TIC_1US_CNTR):** The application must program this counter so that the number of clock cycles of CSR clock is 1us. (Subtract 1 from the value before programming). For example if the CSR clock is 100MHz then this field needs to be programmed to value 100 - 1 = 99 (which is 0x63). This is required to generate the 1US events that are used to update some of the EEE related counters.

10.2.37 MAC_PHYIF_CONTROL_STATUS — Offset F8h

The PHY Interface Control and Status register indicates the status signals received by the SGMII or RGMII interface (selected at reset) from the PHY. This register is optional.

Type	Size	Offset	Default
MMIO	32 bit	BAR + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RO	**Link Status (LNKSTS):** This bit indicates whether the link is up (1'b1) or down (1'b0). 0x0 (INACTIVE): Link down. 0x1 (ACTIVE): Link up.
18:17	0h RO	**Link Speed (LNKSPEED):** This bit indicates the current speed of the link. 0x0 (M_2500K): 2.5 MHz. 0x1 (M_25M): 25 MHz. 0x2 (M_125M): 125 MHz. 0x3 (RSVD): Reserved.
16	0h RO	**Link Mode (LNKMOD):** This bit indicates the current mode of operation of the link. 0x0 (HDUPLX): Half-duplex mode. 0x1 (FDUPLX): Full-duplex mode.

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**
1	0h RW	**Link Up or Down (LUD):** This bit indicates whether the link is up or down during transmission of configuration in the RGMII or SGMII interface. 0x0 (LINKDOWN): Link down. 0x1 (LINKUP): Link up.
0	0h RW	**Transmit Configuration in RGMII or SGMII (TC):** When set, this bit enables the transmission of duplex mode, link speed, and link up or down information to the PHY in the RGMII or SGMII port. When this bit is reset, no such information is driven to the PHY. The details of this feature are provided in the following sections: - "Reduced Gigabit Media Independent Interface" - "Serial Media Independent Interface" - "Serial Gigabit Media Independent Interface" 0x0 (DISABLE): Disable Transmit Configuration in RGMII or SGMII. 0x1 (ENABLE): Enable Transmit Configuration in RGMII or SGMII.

10.2.38 MAC_VERSION — Offset 110h

The version register identifies the version of the GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 110h	00005152h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	51h RO	**USERVER:** Version code
7:0	52h RO	**SNPSVER:** Version code

10.2.39 MAC_DEBUG — Offset 114h

The Debug register provides the debug status of various MAC blocks.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 114h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18:17	0h RO	**MAC Transmit Packet Controller Status (TFCSTS):** This field indicates the state of the MAC Transmit Packet Controller module. 0x0 (IDLE): Idle state. 0x1 (WAITING): Waiting for one of the following: Status of the previous packet OR IPG or back off period to be over. 0x2 (GEN_TX_PAU): Generating and transmitting a Pause control packet (in full-duplex mode). 0x3 (TRNSFR): Transferring input packet for transmission.
16	0h RO	**MAC GMII or MII Transmit Protocol Engine Status (TPESTS):** When this bit is set, it indicates that the MAC GMII or MII transmit protocol engine is actively transmitting data, and it is not in the Idle state. 0x0 (INACTIVE): MAC GMII or MII Transmit Protocol Engine Status not detected. 0x1 (ACTIVE): MAC GMII or MII Transmit Protocol Engine Status detected.
15:3	0h RO	**Reserved**
2:1	0h RO	**MAC Receive Packet Controller FIFO Status (RFCFCSTS):** When this bit is set, this field indicates the active state of the small FIFO Read and Write controllers of the MAC Receive Packet Controller module.
0	0h RO	**MAC GMII or MII Receive Protocol Engine Status (RPESTS):** When this bit is set, it indicates that the MAC GMII or MII receive protocol engine is actively receiving data, and it is not in the Idle state. 0x0 (INACTIVE): MAC GMII or MII Receive Protocol Engine Status not detected. 0x1 (ACTIVE): MAC GMII or MII Receive Protocol Engine Status detected.

10.2.40 MAC_HW_FEATURE0 — Offset 11Ch

This register indicates the presence of first set of the optional features or functions of the GbE Controller. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11Ch	0EFD73F7h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	0h RO	**Active PHY Selected (ACTPHYSEL):** When you have multiple PHY interfaces in your configuration, this field indicates the sampled value of phy_intf_sel_i during reset de-assertion. 0x0 (GMII_MII): GMII or MII. 0x1 (RGMII): RGMII. 0x2 (SGMII): SGMII. 0x3 (TBI): TBI. 0x4 (RMII): RMII. 0x5 (RTBI): RTBI. 0x6 (SMII): SMII. 0x7 (REVMIII): RevMII.
27	1h RO	**Source Address or VLAN Insertion Enable (SAVLANINS):** This bit is set to 1 when the Enable SA and VLAN Insertion on Tx option is selected 0x0 (INACTIVE): Source Address or VLAN Insertion Enable option is not selected. 0x1 (ACTIVE): Source Address or VLAN Insertion Enable option is selected.
26:25	3h RO	**Timestamp System Time Source (TSSTSSEL):** This bit indicates the source of the Timestamp system time: This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected 0x0 (INTRNL): Internal. 0x1 (EXTRNL): External. 0x2 (BOTH): Both. 0x3 (RSVD): Reserved.
24	0h RO	**MAC Addresses 64-127 Selected (MACADR64SEL):** This bit is set to 1 when the Enable Additional 64 MAC Address Registers (64-127) option is selected 0x0 (INACTIVE): MAC Addresses 64-127 Select option is not selected. 0x1 (ACTIVE): MAC Addresses 64-127 Select option is selected.
23	1h RO	**MAC Addresses 32-63 Selected (MACADR32SEL):** This bit is set to 1 when the Enable Additional 32 MAC Address Registers (32-63) option is selected 0x0 (INACTIVE): MAC Addresses 32-63 Select option is not selected. 0x1 (ACTIVE): MAC Addresses 32-63 Select option is selected.
22:18	1Fh RO	**MAC Addresses 1-31 Selected (ADDMACADRSEL):** This bit is set to 1 when the non-zero value is selected for Enable Additional 1-31 MAC Address Registers option
17	0h RO	**Reserved**
16	1h RO	**Receive Checksum Offload Enabled (RXCOESEL):** This bit is set to 1 when the Enable Receive TCP/IP Checksum Check option is selected 0x0 (INACTIVE): Receive Checksum Offload Enable option is not selected. 0x1 (ACTIVE): Receive Checksum Offload Enable option is selected.
15	0h RO	**Reserved**
14	1h RO	**Transmit Checksum Offload Enabled (TXCOESEL):** This bit is set to 1 when the Enable Transmit TCP/IP Checksum Insertion option is selected 0x0 (INACTIVE): Transmit Checksum Offload Enable option is not selected. 0x1 (ACTIVE): Transmit Checksum Offload Enable option is selected.

Bit Range	Default & Access	Field Name (ID): Description
13	1h RO	**Energy Efficient Ethernet Enabled (EEESEL):** This bit is set to 1 when the Enable Energy Efficient Ethernet (EEE) option is selected 0x0 (INACTIVE): Energy Efficient Ethernet Enable option is not selected. 0x1 (ACTIVE): Energy Efficient Ethernet Enable option is selected.
12	1h RO	**IEEE 1588-2008 Timestamp Enabled (TSSEL):** This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected 0x0 (INACTIVE): IEEE 1588-2008 Timestamp Enable option is not selected. 0x1 (ACTIVE): IEEE 1588-2008 Timestamp Enable option is selected.
11:10	0h RO	**Reserved**
9	1h RO	**ARP Offload Enabled (ARPOFFSEL):** This bit is set to 1 when the Enable IPv4 ARP Offload option is selected 0x0 (INACTIVE): ARP Offload Enable option is not selected. 0x1 (ACTIVE): ARP Offload Enable option is selected.
8	1h RO	**RMON Module Enable (MMCSEL):** This bit is set to 1 when the Enable MAC Management Counters (MMC) option is selected 0x0 (INACTIVE): RMON Module Enable option is not selected. 0x1 (ACTIVE): RMON Module Enable option is selected.
7	1h RO	**PMT Magic Packet Enable (MGKSEL):** This bit is set to 1 when the Enable Magic Packet Detection option is selected 0x0 (INACTIVE): PMT Magic Packet Enable option is not selected. 0x1 (ACTIVE): PMT Magic Packet Enable option is selected.
6	1h RO	**PMT Remote Wake-up Packet Enable (RWKSEL):** This bit is set to 1 when the Enable Remote Wake-Up Packet Detection option is selected 0x0 (INACTIVE): PMT Remote Wake-up Packet Enable option is not selected. 0x1 (ACTIVE): PMT Remote Wake-up Packet Enable option is selected.
5	1h RO	**SMA (MDIO) Interface (SMASEL):** This bit is set to 1 when the Enable Station Management (MDIO Interface) option is selected 0x0 (INACTIVE): SMA (MDIO) Interface not selected. 0x1 (ACTIVE): SMA (MDIO) Interface selected.
4	1h RO	**VLAN Hash Filter Selected (VLHASH):** This bit is set to 1 when the Enable VLAN Hash Table Based Filtering option is selected 0x0 (INACTIVE): VLAN Hash Filter not selected. 0x1 (ACTIVE): VLAN Hash Filter selected.
3	0h RO	**PCS Registers (TBI, SGMII, or RTBI PHY interface) (PCSSEL):** This bit is set to 1 when the TBI, SGMII, or RTBI PHY interface option is selected 0x0 (INACTIVE): No PCS Registers (TBI, SGMII, or RTBI PHY interface). 0x1 (ACTIVE): PCS Registers (TBI, SGMII, or RTBI PHY interface).

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO	**Half-duplex Support (HDSEL):** This bit is set to 1 when the half-duplex mode is selected 0x0 (INACTIVE): No Half-duplex support. 0x1 (ACTIVE): Half-duplex support.
1	1h RO	**1000 Mbps Support (GMIISEL):** This bit is set to 1 when 1000 Mbps is selected as the Mode of Operation 0x0 (INACTIVE): No 1000 Mbps support. 0x1 (ACTIVE): 1000 Mbps support.
0	1h RO	**10 or 100 Mbps Support (MIISEL):** This bit is set to 1 when 10/100 Mbps is selected as the Mode of Operation 0x0 (INACTIVE): No 10 or 100 Mbps support. 0x1 (ACTIVE): 10 or 100 Mbps support.

10.2.41 MAC_HW_FEATURE1 — Offset 120h

This register indicates the presence of second set of the optional features or functions of the GbE Controller. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 120h	119F7A28h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:27	2h RO	**Total number of L3 or L4 Filters (L3L4FNUM):** This field indicates the total number of L3 or L4 filters: 0x0 (NOFILT): No L3 or L4 Filter. 0x1 (M_1FILT): 1 L3 or L4 Filter. 0x2 (M_2FILT): 2 L3 or L4 Filters. 0x3 (M_3FILT): 3 L3 or L4 Filters. 0x4 (M_4FILT): 4 L3 or L4 Filters. 0x5 (M_5FILT): 5 L3 or L4 Filters. 0x6 (M_6FILT): 6 L3 or L4 Filters. 0x7 (M_7FILT): 7 L3 or L4 Filters. 0x08 (M_8FILT): 8 L3 or L4 Filters.
26	0h RO	**Reserved**
25:24	1h RO	**Hash Table Size (HASHTBLSZ):** This field indicates the size of the hash table: 0x0 (NO_HT): No hash table. 0x1 (M_64): 64. 0x2 (M_128): 128. 0x3 (M_256): 256.

Bit Range	Default & Access	Field Name (ID): Description
23	1h RO	**One Step for PTP over UDP/IP Feature Enable (POUOST):** This bit is set to 1 when the Enable One step timestamp for PTP over UDP/IP feature is selected. 0x0 (INACTIVE): One Step for PTP over UDP/IP Feature is not selected. 0x1 (ACTIVE): One Step for PTP over UDP/IP Feature is selected.
22	0h RO	**Reserved**
21	0h RO	**Rx Side Only AV Feature Enable (RAVSEL):** This bit is set to 1 when the Enable Audio Video Bridging option on Rx Side Only is selected. 0x0 (INACTIVE): Rx Side Only AV Feature is not selected. 0x1 (ACTIVE): Rx Side Only AV Feature is selected.
20	1h RO	**AV Feature Enable (AVSEL):** This bit is set to 1 when the Enable Audio Video Bridging option is selected. 0x0 (INACTIVE): AV Feature is not selected. 0x1 (ACTIVE): AV Feature is selected.
19	1h RO	**DMA Debug Registers Enable (DBGMEMA):** This bit is set to 1 when the Debug Mode Enable option is selected 0x0 (INACTIVE): DMA Debug Registers option is not selected. 0x1 (ACTIVE): DMA Debug Registers option is selected.
18	1h RO	**TCP Segmentation Offload Enable (TSOEN):** This bit is set to 1 when the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected 0x0 (INACTIVE): TCP Segmentation Offload Feature is not selected. 0x1 (ACTIVE): TCP Segmentation Offload Feature is selected.
17	1h RO	**Split Header Feature Enable (SPHEN):** This bit is set to 1 when the Enable Split Header Structure option is selected 0x0 (INACTIVE): Split Header Feature is not selected. 0x1 (ACTIVE): Split Header Feature is selected.
16	1h RO	**DCB Feature Enable (DCBEN):** This bit is set to 1 when the Enable Data Center Bridging option is selected 0x0 (INACTIVE): DCB Feature is not selected. 0x1 (ACTIVE): DCB Feature is selected.
15:14	1h RO	**Address Width. (ADDR64):** This field indicates the configured address width: 0x0 (M_32): 32. 0x1 (M_40): 40. 0x2 (M_48): 48. 0x3 (RSVD): Reserved.
13	1h RO	**IEEE 1588 High Word Register Enable (ADVTHWORD):** This bit is set to 1 when the Add IEEE 1588 Higher Word Register option is selected 0x0 (INACTIVE): IEEE 1588 High Word Register option is not selected. 0x1 (ACTIVE): IEEE 1588 High Word Register option is selected.
12	1h RO	**PTP Offload Enable (PTOEN):** This bit is set to 1 when the Enable PTP Timestamp Offload Feature is selected. 0x0 (INACTIVE): PTP Offload feature is not selected. 0x1 (ACTIVE): PTP Offload feature is selected.
11	1h RO	**One-Step Timestamping Enable (OSTEN):** This bit is set to 1 when the Enable One-Step Timestamp Feature is selected. 0x0 (INACTIVE): One-Step Timestamping feature is not selected. 0x1 (ACTIVE): One-Step Timestamping feature is selected.

Bit Range	Default & Access	Field Name (ID): Description
10:6	08h RO	**MTL Transmit FIFO Size (TXFIFOSIZE):** This field contains the configured value of MTL Tx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(TXFIFO_SIZE) -7: 0x0 (M_128B): 128 bytes. 0x1 (M_256B): 256 bytes. 0x2 (M_512B): 512 bytes. 0x3 (M_1024B): 1024 bytes. 0x4 (M_2048B): 2048 bytes. 0x5 (M_4096B): 4096 bytes. 0x6 (M_8192B): 8192 bytes. 0x7 (M_16384B): 16384 bytes. 0x08 (M_32KB): 32 KB. 0x09 (M_64KB): 64 KB. 0x0A (M_128KB): 128 KB. 0x0B (RSVD): Reserved.
5	1h RO	**Single Port RAM Enable (SPRAM):** This bit is set to 1 when the Use single port RAM Feature is selected. 0x0 (INACTIVE): Single Port RAM feature is not selected. 0x1 (ACTIVE): Single Port RAM feature is selected.
4:0	08h RO	**MTL Receive FIFO Size (RXFIFOSIZE):** This field contains the configured value of MTL Rx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(RXFIFO_SIZE) -7: 0x0 (M_128B): 128 bytes. 0x1 (M_256B): 256 bytes. 0x2 (M_512B): 512 bytes. 0x3 (M_1024B): 1024 bytes. 0x4 (M_2048B): 2048 bytes. 0x5 (M_4096B): 4096 bytes. 0x6 (M_8192B): 8192 bytes. 0x7 (M_16384B): 16384 bytes. 0x08 (M_32KB): 32 KB. 0x09 (M_64KB): 64 KB. 0x0A (M_128KB): 128 KB. 0x0B (M_256KB): 256 KB. 0x0C (RSVD): Reserved.

10.2.42 MAC_HW_FEATURE2 — Offset 124h

This register indicates the presence of third set of the optional features or functions of the GbE Controller. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 124h	22DF71C7h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	2h RO	**Number of Auxiliary Snapshot Inputs (AUXSNAPNUM):** This field indicates the number of auxiliary snapshot inputs: 0x0 (NO_AUXI): No auxiliary input. 0x1 (M_1_AUXI): 1 auxiliary input. 0x2 (M_2_AUXI): 2 auxiliary input. 0x3 (M_3_AUXI): 3 auxiliary input. 0x4 (M_4_AUXI): 4 auxiliary input. 0x5 (RSVD): Reserved.
27	0h RO	**Reserved**
26:24	2h RO	**Number of PPS Outputs (PPSOUTNUM):** This field indicates the number of PPS outputs: 0x0 (NO_PPSO): No PPS output. 0x1 (M_1_PPSO): 1 PPS output. 0x2 (M_2_PPSO): 2 PPS output. 0x3 (M_3_PPSO): 3 PPS output. 0x4 (M_4_PPSO): 4 PPS output. 0x5 (RSVD): Reserved.
23:22	3h RO	**Tx DMA Descriptor Cache Size in terms of 16 bytes descriptors: (TDCSZ):** 00 - Cache Not configured 01 - 4 16 bytes descriptor 10 - 8 16 bytes descriptor 11 - 16 16 bytes descriptor
21:18	7h RO	**Number of DMA Transmit Channels (TXCHCNT):** This field indicates the number of DMA Transmit channels: 0x0 (M_1TXCH): 1 MTL Tx Channel. 0x0 (NO_DCACHE): Desc Cache not configured. 0x1 (M_1TDCSZ): 4. 0x1 (M_2TXCH): 2 MTL Tx Channels. 0x2 (M_2TDCSZ): 8. 0x2 (M_3TXCH): 3 MTL Tx Channels. 0x3 (M_3TDCSZ): 16. 0x3 (M_4TXCH): 4 MTL Tx Channels. 0x4 (M_5TXCH): 5 MTL Tx Channels. 0x5 (M_6TXCH): 6 MTL Tx Channels. 0x6 (M_7TXCH): 7 MTL Tx Channels. 0x7 (M_8TXCH): 8 MTL Tx Channels.
17:16	3h RO	**Rx DMA Descriptor Cache Size in terms of 16 bytes descriptors: (RDCSZ):** 00 - Cache Not configured 01 - 4 16 bytes descriptor 10 - 8 16 bytes descriptor 11 - 16 16 bytes descriptor

Bit Range	Default & Access	Field Name (ID): Description
15:12	7h RO	**Number of DMA Receive Channels (RXCHCNT):** This field indicates the number of DMA Receive channels: 0x0 (M_1RXCH): 1 MTL Rx Channel. 0x0 (NO_DCACHE): Desc Cache not configured. 0x1 (M_1RDCSZ): 4. 0x1 (M_2RXCH): 2 MTL Rx Channels. 0x2 (M_2RDCSZ): 8. 0x2 (M_3RXCH): 3 MTL Rx Channels. 0x3 (M_3RDCSZ): 16. 0x3 (M_4RXCH): 4 MTL Rx Channels. 0x4 (M_5RXCH): 5 MTL Rx Channels. 0x5 (M_6RXCH): 6 MTL Rx Channels. 0x6 (M_7RXCH): 7 MTL Rx Channels. 0x7 (M_8RXCH): 8 MTL Rx Channels.
11:10	0h RO	**Reserved**
9:6	7h RO	**Number of MTL Transmit Queues (TXQCNT):** This field indicates the number of MTL Transmit queues: 0x0 (M_1TXQ): 1 MTL Tx Queue. 0x1 (M_2TXQ): 2 MTL Tx Queues. 0x2 (M_3TXQ): 3 MTL Tx Queues. 0x3 (M_4TXQ): 4 MTL Tx Queues. 0x4 (M_5TXQ): 5 MTL Tx Queues. 0x5 (M_6TXQ): 6 MTL Tx Queues. 0x6 (M_7TXQ): 7 MTL Tx Queues. 0x7 (M_8TXQ): 8 MTL Tx Queues.
5:4	0h RO	**Reserved**
3:0	7h RO	**Number of MTL Receive Queues (RXQCNT):** This field indicates the number of MTL Receive queues: 0x0 (M_1RXQ): 1 MTL Rx Queue. 0x1 (M_2RXQ): 2 MTL Rx Queues. 0x2 (M_3RXQ): 3 MTL Rx Queues. 0x3 (M_4RXQ): 4 MTL Rx Queues. 0x4 (M_5RXQ): 5 MTL Rx Queues. 0x5 (M_6RXQ): 6 MTL Rx Queues. 0x6 (M_7RXQ): 7 MTL Rx Queues. 0x7 (M_8RXQ): 8 MTL Rx Queues.

10.2.43 MAC_HW_FEATURE3 — Offset 128h

This register indicates the presence of fourth set the optional features or functions of the GbE Controller. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 128h	2C395632h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	2h RO	**Automotive Safety Package (ASP):** Following are the encoding for the different Safety features 0x0 (NONE): No Safety features selected. 0x1 (ECC_ONLY): Only "ECC protection for external memory" feature is selected. 0x2 (AS_NPPE): All the Automotive Safety features are selected without the "Parity Port Enable for external interface" feature. 0x3 (AS_PPE): All the Automotive Safety features are selected with the "Parity Port Enable for external interface" feature.
27	1h RO	**Time Based Scheduling Enable (TBSSEL):** This bit is set to 1 when the Time Based Scheduling feature is selected. 0x0 (INACTIVE): Time Based Scheduling Enable feature is not selected. 0x1 (ACTIVE): Time Based Scheduling Enable feature is selected.
26	1h RO	**Frame Preemption Enable (FPESEL):** This bit is set to 1 when the Enable Frame preemption feature is selected. 0x0 (INACTIVE): Frame Preemption Enable feature is not selected. 0x1 (ACTIVE): Frame Preemption Enable feature is selected.
25:22	0h RO	**Reserved**
21:20	3h RO	**Width of the Time Interval field in the Gate Control List (ESTWID):** This field indicates the width of the Configured Time Interval Field 0x0 (NOWIDTH): Width not configured. 0x1 (WIDTH16): 16. 0x2 (WIDTH20): 20. 0x3 (WIDTH24): 24.
19:17	4h RO	**Depth of the Gate Control List (ESTDEP):** This field indicates the depth of Gate Control list expressed as Log2(512)-5 0x0 (NODEPTH): No Depth configured. 0x1 (DEPTH64): 64. 0x2 (DEPTH128): 128. 0x3 (DEPTH256): 256. 0x4 (DEPTH512): 512. 0x5 (DEPTH1024): 1024. 0x6 (RSVD): Reserved.
16	1h RO	**Enhancements to Scheduling Traffic Enable (ESTSEL):** This bit is set to 1 when the Enable Enhancements to Scheduling Traffic feature is selected. 0x0 (INACTIVE): Enable Enhancements to Scheduling Traffic feature is not selected. 0x1 (ACTIVE): Enable Enhancements to Scheduling Traffic feature is selected.
15	0h RO	**Reserved**
14:13	2h RO	**Flexible Receive Parser Table Entries size (FRPES):** This field indicates the Max Number of Parser Entries supported by Flexible Receive Parser. 0x0 (M_64ENTR): 64 Entries. 0x1 (M_128ENTR): 128 Entries. 0x2 (M_256ENTR): 256 Entries. 0x3 (RSVD): Reserved.

Bit Range	Default & Access	Field Name (ID): Description
12:11	2h RO	**Flexible Receive Parser Buffer size (FRPBS):** This field indicates the supported Max Number of bytes of the packet data to be Parsed by Flexible Receive Parser. 0x0 (M_64BYTES): 64 Bytes. 0x1 (M_128BYTES): 128 Bytes. 0x2 (M_256BYTES): 256 Bytes. 0x3 (RSVD): Reserved.
10	1h RO	**Flexible Receive Parser Selected (FRPSEL):** This bit is set to 1 when the Enable Flexible Programmable Receive Parser option is selected. 0x0 (INACTIVE): Flexible Receive Parser feature is not selected. 0x1 (ACTIVE): Flexible Receive Parser feature is selected.
9	1h RO	**Broadcast/Multicast Packet Duplication (PDUPSEL):** This bit is set to 1 when the Broadcast/Multicast Packet Duplication feature is selected. 0x0 (INACTIVE): Broadcast/Multicast Packet Duplication feature is not selected. 0x1 (ACTIVE): Broadcast/Multicast Packet Duplication feature is selected.
8:6	0h RO	**Reserved**
5	1h RO	**Double VLAN Tag Processing Selected (DVLAN):** This bit is set to 1 when the Enable Double VLAN Processing Feature is selected. 0x0 (INACTIVE): Double VLAN option is not selected. 0x1 (ACTIVE): Double VLAN option is selected.
4	1h RO	**Queue/Channel based VLAN tag insertion on Tx Enable (CBTISEL):** This bit is set to 1 when the Enable Queue/Channel based VLAN tag insertion on Tx Feature is selected. 0x0 (INACTIVE): Enable Queue/Channel based VLAN tag insertion on Tx feature is not selected. 0x1 (ACTIVE): Enable Queue/Channel based VLAN tag insertion on Tx feature is selected.
3	0h RO	**Reserved**
2:0	2h RO	**Number of Extended VLAN Tag Filters Enabled (NRVF):** This field indicates the Number of Extended VLAN Tag Filters selected: 0x0 (NO_ERVLAN): No Extended Rx VLAN Filters. 0x1 (M_4_ERVLAN): 4 Extended Rx VLAN Filters. 0x2 (M_8_ERVLAN): 8 Extended Rx VLAN Filters. 0x3 (M_16_ERVLAN): 16 Extended Rx VLAN Filters. 0x4 (M_24_ERVLAN): 24 Extended Rx VLAN Filters. 0x5 (M_32_ERVLAN): 32 Extended Rx VLAN Filters. 0x6 (RSVD): Reserved.

10.2.44 MAC_DPP_FSM_INTERRUPT_STATUS — Offset 140h

This register contains the status of Automotive Safety related Data Path Parity Errors, Interface Timeout Errors, FSM State Parity Errors and FSM State Timeout Errors. All the non-Reserved bits are cleared on read.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 140h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**FSM State Parity Error Status (FSMPES):** This field when set indicates one of the FSMs State registers has a parity error detected. 0x0 (INACTIVE): FSM State Parity Error Status not detected. 0x1 (ACTIVE): FSM State Parity Error Status detected.
23:18	0h RO	**Reserved**
17	0h RW	**Slave Read/Write Timeout Error Status (SLVTES):** This field when set indicates that an Application/CSR Timeout has occurred on the AXI slave interface. 0x0 (INACTIVE): Slave Read/Write Timeout Error Status not detected. 0x1 (ACTIVE): Slave Read/Write Timeout Error Status detected.
16	0h RW	**Master Read/Write Timeout Error Status (MSTTES):** This field when set indicates that an Application/CSR Timeout has occurred on the master (AXI/AHB/ARI/ATI) interface. 0x0 (INACTIVE): Master Read/Write Timeout Error Status not detected. 0x1 (ACTIVE): Master Read/Write Timeout Error Status detected.
15:13	0h RO	**Reserved**
12	0h RW	**PTP FSM Timeout Error Status (PTES):** This field when set indicates that one of the PTP FSM Timeout has occurred. 0x0 (INACTIVE): PTP FSM Timeout Error Status not detected. 0x1 (ACTIVE): PTP FSM Timeout Error Status detected.
11	0h RW	**APP FSM Timeout Error Status (ATES):** This field when set indicates that one of the APP FSM Timeout has occurred. 0x0 (INACTIVE): APP FSM Timeout Error Status not detected. 0x1 (ACTIVE): APP FSM Timeout Error Status detected.
10	0h RW	**CSR FSM Timeout Error Status (CTES):** This field when set indicates that one of the CSR FSM Timeout has occurred. 0x0 (INACTIVE): CSR FSM Timeout Error Status not detected. 0x1 (ACTIVE): CSR FSM Timeout Error Status detected.
9	0h RW	**Rx FSM Timeout Error Status (RTES):** This field when set indicates that one of the Rx FSM Timeout has occurred. 0x0 (INACTIVE): Rx FSM Timeout Error Status not detected. 0x1 (ACTIVE): Rx FSM Timeout Error Status detected.
8	0h RW	**Tx FSM Timeout Error Status (TTES):** This field when set indicates that one of the Tx FSM Timeout has occurred. 0x0 (INACTIVE): Tx FSM Timeout Error Status not detected. 0x1 (ACTIVE): Tx FSM Timeout Error Status detected.
7	0h RW	**AXI Slave Read data path Parity checker Error Status (ASRPES):** This bit when set indicates that parity error is detected at the AXI Slave read data interface. 0x0 (INACTIVE): AXI Slave Read data path Parity checker Error Status not detected. 0x1 (ACTIVE): AXI Slave Read data path Parity checker Error Status detected.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**CSR Write data path Parity checker Error Status (CWPES):** This bit when set indicates that parity error is detected at the CSR write data interface on mci_wdata_i (or at PC8 checker as shown in AXI slave Interface Data path parity protection diagram). When EPSI bit of MTL_DPP_Control register is set and if any parity mis-match is detected on the input slave parity ports (or at PC7 checker in the AXI slave Interface Data path parity protection diagram) sets this bit to one. 0x0 (INACTIVE): CSR Write data path Parity checker Error Status not detected. 0x1 (ACTIVE): CSR Write data path Parity checker Error Status detected.
5	0h RW	**Application Receive interface data path Parity Error Status (ARPES):** This bit when set indicates that a parity error is detected by the hardware internally at the interface with the application. 0x0 (INACTIVE): Application Receive interface data path Parity Error Status not detected. 0x1 (ACTIVE): Application Receive interface data path Parity Error Status detected.
4	0h RW	**MTL TX Status data path Parity checker Error Status (MTSPES):** This filed when set indicates that, parity error is detected on the MTL TX Status data on ati interface (or at PC5 as shown in Transmit data path parity protection diagram). 0x0 (INACTIVE): MTL TX Status data path Parity checker Error Status not detected. 0x1 (ACTIVE): MTL TX Status data path Parity checker Error Status detected.
3	0h RW	**MTL data path Parity checker Error Status (MPES):** This bit when set indicates that a parity error is detected at the MTL transmit write controller parity checker (or at PC4 as shown in Transmit data path parity protection diagram). 0x0 (INACTIVE): MTL data path Parity checker Error Status not detected. 0x1 (ACTIVE): MTL data path Parity checker Error Status detected.
2	0h RW	**Read Descriptor Parity checker Error Status (RDPES):** This bit when set indicates that a parity error is detected at the DMA Read descriptor parity checker (or at PC3 as shown in Transmit data path parity protection diagram). 0x0 (INACTIVE): Read Descriptor Parity checker Error Status not detected. 0x1 (ACTIVE): Read Descriptor Parity checker Error Status detected.
1	0h RW	**TSO data path Parity checker Error Status (TPES):** This bit when set indicates that a parity error is detected at the DMA TSO parity checker (or at PC2 as shown in Transmit data path parity protection diagram). 0x0 (INACTIVE): TSO data path Parity checker Error Status not detected. 0x1 (ACTIVE): TSO data path Parity checker Error Status detected.
0	0h RO	**Reserved**

10.2.45 MAC_AXI_SLV_DPE_ADDR_STATUS — Offset 144h

This register indicates the CSR address corresponding to the CSR write data on which parity error occured.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 144h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:0	0000h RO	**AXI Slave data path Parity Error Address Status (ASPEAS):** This field holds the CSR address for which parity error is detected on the CSR write data. This field holds the first address for which parity error is detected on the write data and is cleared on read.

10.2.46 MAC_FSM_CONTROL — Offset 148h

This register is used to control the FSM State parity and timeout error injection in Debug mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 148h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**PTP Large/Normal Mode Select (PLGRNML):** This field when set indicates that large mode tic generation is used for PTP domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for PTP domain. 0x1 (ENABLE): large mode tic generation is used for PTP domain.
27	0h RW	**APP Large/Normal Mode Select (ALGRNML):** This field when set indicates that large mode tic generation is used for APP domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for APP domain. 0x1 (ENABLE): large mode tic generation is used for APP domain.
26	0h RW	**CSR Large/Normal Mode Select (CLGRNML):** This field when set indicates that large mode tic generation is used for CSR domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for CSR domain. 0x1 (ENABLE): large mode tic generation is used for CSR domain.
25	0h RW	**Rx Large/Normal Mode Select (RLGRNML):** This field when set indicates that large mode tic generation is used for Rx domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for Rx domain. 0x1 (ENABLE): large mode tic generation is used for Rx domain.
24	0h RW	**Tx Large/Normal Mode Select (TLGRNML):** This field when set indicates that large mode tic generation is used for Tx domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for Tx domain. 0x1 (ENABLE): large mode tic generation is used for Tx domain.
23:21	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**PTP FSM Parity Error Injection (PPEIN):** This field when set indicates that Error Injection for PTP FSM Parity is enabled. 0x0 (DISABLE): PTP FSM Parity Error Injection is disabled. 0x1 (ENABLE): PTP FSM Parity Error Injection is enabled.
19	0h RW	**APP FSM Parity Error Injection (APEIN):** This field when set indicates that Error Injection for APP FSM Parity is enabled. 0x0 (DISABLE): APP FSM Parity Error Injection is disabled. 0x1 (ENABLE): APP FSM Parity Error Injection is enabled.
18	0h RW	**CSR FSM Parity Error Injection (CPEIN):** This field when set indicates that Error Injection for CSR Parity is enabled. 0x0 (DISABLE): CSR FSM Parity Error Injection is disabled. 0x1 (ENABLE): CSR FSM Parity Error Injection is enabled.
17	0h RW	**Rx FSM Parity Error Injection (RPEIN):** This field when set indicates that Error Injection for RX FSM Parity is enabled. 0x0 (DISABLE): Rx FSM Parity Error Injection is disabled. 0x1 (ENABLE): Rx FSM Parity Error Injection is enabled.
16	0h RW	**Tx FSM Parity Error Injection (TPEIN):** This field when set indicates that Error Injection for TX FSM Parity is enabled. 0x0 (DISABLE): Tx FSM Parity Error Injection is disabled. 0x1 (ENABLE): Tx FSM Parity Error Injection is enabled.
15:13	0h RO	**Reserved**
12	0h RW	**PTP FSM Timeout Error Injection (PTEIN):** This field when set indicates that Error Injection for PTP FSM timeout is enabled. 0x0 (DISABLE): PTP FSM Timeout Error Injection is disabled. 0x1 (ENABLE): PTP FSM Timeout Error Injection is enabled.
11	0h RW	**APP FSM Timeout Error Injection (ATEIN):** This field when set indicates that Error Injection for APP FSM timeout is enabled. 0x0 (DISABLE): APP FSM Timeout Error Injection is disabled. 0x1 (ENABLE): APP FSM Timeout Error Injection is enabled.
10	0h RW	**CSR FSM Timeout Error Injection (CTEIN):** This field when set indicates that Error Injection for CSR timeout is enabled. 0x0 (DISABLE): CSR FSM Timeout Error Injection is disabled. 0x1 (ENABLE): CSR FSM Timeout Error Injection is enabled.
9	0h RW	**Rx FSM Timeout Error Injection (RTEIN):** This field when set indicates that Error Injection for RX FSM timeout is enabled. 0x0 (DISABLE): Rx FSM Timeout Error Injection is disabled. 0x1 (ENABLE): Rx FSM Timeout Error Injection is enabled.
8	0h RW	**Tx FSM Timeout Error Injection (TTEIN):** This field when set indicates that Error Injection for TX FSM timeout is enabled. 0x0 (DISABLE): Tx FSM Timeout Error Injection is disabled. 0x1 (ENABLE): Tx FSM Timeout Error Injection is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW	**PRTYEN:** This bit when set indicates that the FSM parity feature is enabled. 0x0 (DISABLE): FSM Parity feature is disabled. 0x1 (ENABLE): FSM Parity feature is enabled.
0	0h RW	**TMOUTEN:** This bit when set indicates that the FSM timeout feature is enabled. 0x0 (DISABLE): FSM timeout feature is disabled. 0x1 (ENABLE): FSM timeout feature is enabled.

10.2.47 MAC_FSM_ACT_TIMER — Offset 14Ch

This register is used to select the FSM and Interface Timeout values.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**LTMRMD:** This field provides the mode value to be used for large mode FSM and other interface time outs. The timeout duration based on the mode value is given below 0x0 (DISABLE): Timer disabled. 0x1 (M_1MICRO_SEC): 1us. 0x2 (M_4MILLI_SEC): 1.024ms (~4ms). 0x3 (M_16MILLI_SEC): 16.384ms (~16ms). 0x4 (M_64MILLI_SEC): 65.536ms (~64ms). 0x5 (M_256MILLI_SEC): 262.144ms (~256ms). 0x6 (M_1SEC): 1.048sec (~1sec). 0x7 (M_4SEC): 4.194sec (~4sec). 0x08 (M_16SEC): 16.777sec (~16sec). 0x09 (M_32SEC): 33.554sec (~32sec). 0x0A (M_64SEC): 67.108sec (~64sec). 0x0B (RSVD): Reserved.
19:16	0h RW	**NTMRMD:** This field provides the value to be used for normal mode FSM and other interface time outs. The timeout duration based on the mode value is given below 0x0 (DISABLE): Timer disabled. 0x1 (M_1MICRO_SEC): 1us. 0x2 (M_4MILLI_SEC): 1.024ms (~4ms). 0x3 (M_16MILLI_SEC): 16.384ms (~16ms). 0x4 (M_64MILLI_SEC): 65.536ms (~64ms). 0x5 (M_256MILLI_SEC): 262.144ms (~256ms). 0x6 (M_1SEC): 1.048sec (~1sec). 0x7 (M_4SEC): 4.194sec (~4sec). 0x08 (M_16SEC): 16.777sec (~16sec). 0x09 (M_32SEC): 33.554sec (~32sec). 0x0A (M_64SEC): 67.108sec (~64sec). 0x0B (RSVD): Reserved.
15:10	0h RO	**Reserved**
9:0	000h RW	**TMR:** This field indicates the number of CSR clocks required to generate 1us tic.

10.2.48 SNPS_SCS_REG1 — Offset 150h

Reserved

Type	Size	Offset	Default
MMIO	32 bit	BAR + 150h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Reserved**

10.2.49 MAC_MDIO_ADDRESS — Offset 200h

The MDIO Address register controls the management cycles to external PHY through a management interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 200h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RW	**Preamble Suppression Enable (PSE):** When this bit is set, the SMA suppresses the 32-bit preamble and transmits MDIO frames with only 1 preamble bit. When this bit is 0, the MDIO frame always has 32 bits of preamble as defined in the IEEE specifications. 0x0 (DISABLE): Preamble Suppression disabled. 0x1 (ENABLE): Preamble Suppression enabled.
26	0h RW	**Back to Back transactions (BTB):** When this bit is set and the NTC has value greater than 0, then the MAC informs the completion of a read or write command at the end of frame transfer (before the trailing clocks are transmitted). The software can thus initiate the next command which is executed immediately irrespective of the number trailing clocks generated for the previous frame. When this bit is reset, then the read/write command completion (GB is cleared) only after the trailing clocks are generated. In this mode, it is ensured that the NTC is always generated after each frame. This bit must not be set when NTC=0. 0x0 (DISABLE): Back to Back transactions disabled. 0x1 (ENABLE): Back to Back transactions enabled.
25:21	00h RW	**Physical Layer Address (PA):** This field indicates which Clause 22 PHY devices (out of 32 devices) the MAC is accessing. This field indicates which Clause 45 capable PHYs (out of 32 PHYs) the MAC is accessing.
20:16	00h RW	**Register/Device Address (RDA):** These bits select the PHY register in selected Clause 22 PHY device. These bits select the Device (MMD) in selected Clause 45 capable PHY.
15	0h RO	**Reserved**
14:12	0h RW	**Number of Trailing Clocks (NTC):** This field controls the number of trailing clock cycles generated on the MDIO Clock (MDC) after the end of transmission of MDIO frame. The valid values can be from 0 to 7. Programming the value to 3'h3 indicates that there are additional three clock cycles on the MDC line after the end of MDIO frame transfer.

Bit Range	Default & Access	Field Name (ID): Description
11:8	0h RW	**CSR Clock Range (CR):** The CSR Clock Range selection determines the frequency of the MDC clock according to the CSR clock frequency used in your design: - 0000: CSR clock = 60-100 MHz; MDC clock = CSR clock/42 - 0001: CSR clock = 100-150 MHz; MDC clock = CSR clock/62 - 0010: CSR clock = 20-35 MHz; MDC clock = CSR clock/16 - 0011: CSR clock = 35-60 MHz; MDC clock = CSR clock/26 - 0100: CSR clock = 150-250 MHz; MDC clock = CSR clock/102 - 0101: CSR clock = 250-300 MHz; MDC clock = CSR clock/124 - 0110: CSR clock = 300-500 MHz; MDC clock = CSR clock/204 - 0111: CSR clock = 500-800 MHz; MDC clock = CSR clock/324 The suggested range of CSR clock frequency applicable for each value (when Bit 11 = 0) ensures that the MDC clock is approximately between 1.0 MHz to 2.5 MHz freqency range. When Bit 11 is set, you can achieve a higher frequency of the MDC clock than the frequency limit of 2.5 MHz (specified in the IEEE 802.3) and program a clock divider of lower value. For example, when CSR clock is of 100 MHz frequency and you program these bits as 1010, the resultant MDC clock is of 12.5 MHz which is above the range specified in IEEE 802.3. Program the following values only if the interfacing chips support faster MDC clocks: - 1000: CSR clock/4 - 1001: CSR clock/6 - 1010: CSR clock/8 - 1011: CSR clock/10 - 1100: CSR clock/12 - 1101: CSR clock/14 - 1110: CSR clock/16 - 1111: CSR clock/18
7:5	0h RO	**Reserved**
4	0h RW	**Skip Address Packet (SKAP):** When this bit is set, the SMA does not send the address packets before read, write, or post-read increment address packets. This bit is valid only when C45E is set. 0x0 (DISABLE): Skip Address Packet is disabled. 0x1 (ENABLE): Skip Address Packet is enabled.
3	0h RW	**GMII Operation Command 1 (GOC_1):** This bit is higher bit of the operation command to the PHY or GOC_1 and GOC_O are encoded as follows: - 00: Reserved - 01: Write - 10: Post Read Increment Address for Clause 45 PHY - 11: Read When Clause 22 PHY is enabled, only Write and Read commands are valid. 0x0 (DISABLE): GMII Operation Command 1 is disabled. 0x1 (ENABLE): GMII Operation Command 1 is enabled.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GMII Operation Command 0 (GOC_0):** This is the lower bit of the operation command to the PHY or RevMII. When in SMA mode (MDIO master) this bit along with GOC_1 determines the operation to be performed to the PHY. 0x0 (DISABLE): GMII Operation Command 0 is disabled. 0x1 (ENABLE): GMII Operation Command 0 is enabled.
1	0h RW	**Clause 45 PHY Enable (C45E):** When this bit is set, Clause 45 capable PHY is connected to MDIO. When this bit is reset, Clause 22 capable PHY is connected to MDIO. 0x0 (DISABLE): Clause 45 PHY is disabled. 0x1 (ENABLE): Clause 45 PHY is enabled.
0	0h RW	**GMII Busy (GB):** The application sets this bit to instruct the SMA to initiate a Read or Write access to the MDIO slave. The MAC clears this bit after the MDIO frame transfer is completed. Hence the software must not write or change any of the fields in MAC_MDIO_Address and MAC_MDIO_Data registers as long as this bit is set. For write transfers, the application must first write 16-bit data in the GDI field (and also RA field when C45E is set) in MAC_MDIO_Data register before setting this bit. When C45E is set, it should also write into the RA field of MAC_MDIO_Data register before initiating a read transfer. When a read transfer is completed (GB=0), the data read from the PHY register is valid in the GD field of the MAC_MDIO_Data register. Note: Even if the addressed PHY is not present, there is no change in the functionality of this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): GMII Busy is disabled. 0x1 (ENABLE): GMII Busy is enabled.

10.2.50 MAC_MDIO_DATA — Offset 204h

The MDIO Data register stores the Write data to be written to the PHY register located at the address specified in MAC_MDIO_Address. This register also stores the Read data from the PHY register located at the address specified by MDIO Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 204h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Register Address (RA):** This field is valid only when C45E is set. It contains the Register Address in the PHY to which the MDIO frame is intended for.
15:0	0000h RW	**GMII Data (GD):** This field contains the 16-bit data value read from the PHY or RevMII after a Management Read operation or the 16-bit data value to be written to the PHY or RevMII before a Management Write operation.

10.2.51 MAC_GPIO_CONTROL — Offset 208h

The GPIO Control register controls the GPIO.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 208h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

10.2.52 MAC_GPIO_STATUS — Offset 20Ch

The General Purpose IO register provides the control to drive the following: up to 16 bits of output ports (GPO) and status of up to 16 input ports (GPIS).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 20Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RW	**Trigger Snapshot (GPO1)**: Active-high signal. The rising edge of this signal triggers snapshot of current PMC ART and System timer values. The system timer value is stored into AUX FIFO. An interrupt is generated upon snapshotting. The PMC ART timer values is stored in 4x 16-bit ART snapshot register and is read through MDIO registers.
16	0h RW	**P2P Clock Selector (GPO0):** Used for selecting the P2P clock 1 -> 19.2MHz Local Clock Always Running Timer (ART) 0 -> 204.8MHz application clock
15:0	0h RO	**Reversed**

10.2.53 MAC_ARP_ADDRESS — Offset 210h

The ARP Address register contains the IPv4 Destination Address of the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 210h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**ARP Protocol Address (ARPPA):** This field contains the IPv4 Destination Address of the MAC. This address is used for perfect match with the Protocol Address of Target field in the received ARP packet. This field is available only when the Enable IPv4 ARP Offload option is selected.

10.2.54 MAC_CSR_SW_CTRL — Offset 230h

This register contains SW programmable controls for changing the CSR access response and status bits clearing.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 230h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**Slave Error Response Enable (SEEN):** When this bit is set, the MAC responds with Slave Error for accesses to reserved registers in CSR space. When this bit is reset, the MAC responds with Okay response to any register accessed from CSR space. 0x0 (DISABLE): Slave Error Response is disabled. 0x1 (ENABLE): Slave Error Response is enabled.
7:1	0h RO	**Reserved**
0	0h RW	**Register Clear on Write 1 Enable (RCWE):** When this bit is set, the access mode of some register fields changes to Clear on Write 1, the application needs to set that respective bit to 1 to clear it. When this bit is reset, the access mode of these register fields remain as Clear on Read. 0x0 (DISABLE): Register Clear on Write 1 is disabled. 0x1 (ENABLE): Register Clear on Write 1 is enabled.

10.2.55 MAC_FPE_CTRL_STS — Offset 234h

This register controls the operation of Frame Preemption.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 234h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RW	**Transmitted Respond Frame (TRSP):** Set when a Respond mPacket is transmitted (triggered by setting SRSP field). An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Not transmitted Respond Frame. 0x1 (ACTIVE): transmitted Respond Frame.
18	0h RW	**Transmitted Verify Frame (TVER):** Set when a Verify mPacket is transmitted (triggered by setting SVER field). An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Not transmitted Verify Frame. 0x1 (ACTIVE): transmitted Verify Frame.
17	0h RW	**Received Respond Frame (RRSP):** Set when a Respond mPacket is received. An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Not received Respond Frame. 0x1 (ACTIVE): Received Respond Frame.
16	0h RW	**Received Verify Frame (RVER):** Set when a Verify mPacket is received. An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Not received Verify Frame. 0x1 (ACTIVE): Received Verify Frame.
15:4	0h RO	**Reserved**
3	0h RW	**Reserved**
2	0h RW	**Send Respond mPacket (SRSP):** When set indicates hardware to send a Respond mPacket. Reset by hardware after sending the Respond mPacket. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Send Respond mPacket is disabled. 0x1 (ENABLE): Send Respond mPacket is enabled.
1	0h RW	**Send Verify mPacket (SVER):** When set indicates hardware to send a verify mPacket. Reset by hardware after sending the Verify mPacket. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Send Verify mPacket is disabled. 0x1 (ENABLE): Send Verify mPacket is enabled.
0	0h RW	**Enable Tx Frame Preemption (EFPE):** When set Frame Preemption Tx functionality is enabled. 0x0 (DISABLE): Tx Frame Preemption is disabled. 0x1 (ENABLE): Tx Frame Preemption is enabled.

10.2.56 MAC_EXT_CFG1 — Offset 238h

This register contains Split mode control field and offset field for Split Header feature.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 238h	00000002h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:8	0h RW	**Split Mode (SPLM):** These bits indicate the mode of splitting the incoming Rx packets. They are 0x0 (L3L4): Split at L3/L4 header. 0x1 (L2OFST): Split at L2 header with an offset. Always Split at SPLOFST bytes from the beginning of Length/Type field of the Frame. 0x2 (COMBN): Combination mode: Split similar to SPLM=00 for IP packets that are untagged or tagged and VLAN stripped. 0x3 (RSVD): Reserved.
7	0h RO	**Reserved**
6:0	02h RW	**Split Offset (SPLOFST):** These bits indicate the value of offset from the beginning of Length/Type field at which header split should take place when the appropriate SPLM is selected. The reset value of this field is 2 bytes indicating a split at L2 header. Value is in terms of bytes.

10.2.57 MAC_PRESN_TIME_NS — Offset 240h

This register contains the 32-bit binary rollover equivalent time of the PTP System Time in ns.

DWC_EQOS_FLEXI_PPS_OUT_EN=1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 240h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MAC 1722 Presentation Time in ns (MPTN):** These bits indicate the value of the 32-bit binary rollover equivalent time of the PTP System Time in ns

10.2.58 MAC_PRESN_TIME_UPDT — Offset 244h

This field holds the 32-bit value of MAC 1722 Presentation Time in ns, that should be added to the Current Presentation Time Counter value. Init happens when TSINIT is set, and update happens when the TSUPDT bit is set (TSINIT and TSINIT defined in MAC_Timestamp_ Control register).

DWC_EQOS_FLEXI_PPS_OUT_EN=1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 244h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MAC 1722 Presentation Time Update (MPTU):** This field holds the init value or the update value for the presentation time. When used for update, this field holds the 32-bit value in ns, that should be added to the Current Presentation Time Counter value. Init happens when TSINIT is set, and update happens when the TSUPDT bit is set (TSINIT and TSINIT defined in MAC_Timestamp_ Control register). When ADDSUB field of MAC_System_Time_Nanoseconds_Update is set, this value is directly used for subtraction

10.2.59 MAC_ADDRESS0_HIGH — Offset 300h

The MAC Address0 High register holds the upper 16 bits of the first 6-byte MAC address of the station. The first DA byte that is received on the (G)MII interface corresponds to the LS byte (Bits [7:0]) of the MAC Address Low register. For example, if 0x112233445566 is received (0x11 in lane 0 of the first column) on the (G)MII as the destination address, then the MacAddress0 Register [47:0] is compared with 0x665544332211.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, then the synchronization is triggered only when Bits[31:24] of the MAC Address0 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 300h	8000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**Address Enable (AE):** This bit is always set to 1. 0x0 (DISABLE): INVALID : This bit must be always set to 1. 0x1 (ENABLE): This bit is always set to 1.

Bit Range	Default & Access	Field Name (ID): Description
30:24	0h RO	**Reserved**
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address0 content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address0 content is routed.
15:0	FFFFh RW	**MAC Address0[47:32] (ADDRHI):** This field contains the upper 16 bits [47:32] of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

10.2.60 MAC_ADDRESS0_LOW — Offset 304h

The MAC Address0 Low register holds the lower 32 bits of the 6-byte first MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 304h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address0[31:0] (ADDRLO):** This field contains the lower 32 bits of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

10.2.61 MAC_ADDRESS1_HIGH — Offset 308h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 308h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.62 MAC_ADDRESS1_LOW — Offset 30Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 30Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.63 MAC_ADDRESS2_HIGH — Offset 310h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 310h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.64 MAC_ADDRESS2_LOW — Offset 314h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 314h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.65 MAC_ADDRESS3_HIGH — Offset 318h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 318h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.

Bit Range	Default & Access	Field Name (ID): Description
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.66 MAC_ADDRESS3_LOW — Offset 31Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 31Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.67 MAC_ADDRESS4_HIGH — Offset 320h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 320h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.68 MAC_ADDRESS4_LOW — Offset 324h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 324h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.69 MAC_ADDRESS5_HIGH — Offset 328h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 328h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.70 MAC_ADDRESS5_LOW — Offset 32Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 32Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.71 MAC_ADDRESS6_HIGH — Offset 330h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 330h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.

Bit Range	Default & Access	Field Name (ID): Description
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.72 MAC_ADDRESS6_LOW — Offset 334h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 334h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.73 MAC_ADDRESS7_HIGH — Offset 338h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 338h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.74 MAC_ADDRESS7_LOW — Offset 33Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 33Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.75 MAC_ADDRESS8_HIGH — Offset 340h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 340h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.76 MAC_ADDRESS8_LOW — Offset 344h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 344h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.77 MAC_ADDRESS9_HIGH — Offset 348h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 348h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.

Bit Range	Default & Access	Field Name (ID): Description
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.78 MAC_ADDRESS9_LOW — Offset 34Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 34Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.79 MAC_ADDRESS10_HIGH — Offset 350h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 350h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.80 MAC_ADDRESS10_LOW — Offset 354h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 354h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.81 MAC_ADDRESS11_HIGH — Offset 358h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 358h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.82 MAC_ADDRESS11_LOW — Offset 35Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 35Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.83 MAC_ADDRESS12_HIGH — Offset 360h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 360h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.

Bit Range	Default & Access	Field Name (ID): Description
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.84 MAC_ADDRESS12_LOW — Offset 364h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 364h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.85 MAC_ADDRESS13_HIGH — Offset 368h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 368h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.86 MAC_ADDRESS13_LOW — Offset 36Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 36Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.87 MAC_ADDRESS14_HIGH — Offset 370h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 370h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.88 MAC_ADDRESS14_LOW — Offset 374h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 374h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.89 MAC_ADDRESS15_HIGH — Offset 378h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 378h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.

Bit Range	Default & Access	Field Name (ID): Description
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.90 MAC_ADDRESS15_LOW — Offset 37Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 37Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.91 MAC_ADDRESS16_HIGH — Offset 380h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 380h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.92 MAC_ADDRESS16_LOW — Offset 384h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 384h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.93 MAC_ADDRESS17_HIGH — Offset 388h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 388h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.94 MAC_ADDRESS17_LOW — Offset 38Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 38Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.95 MAC_ADDRESS18_HIGH — Offset 390h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 390h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.

Bit Range	Default & Access	Field Name (ID): Description
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.96 MAC_ADDRESS18_LOW — Offset 394h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 394h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.97 MAC_ADDRESS19_HIGH — Offset 398h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 398h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.98 MAC_ADDRESS19_LOW — Offset 39Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 39Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.99 MAC_ADDRESS20_HIGH — Offset 3A0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3A0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.100 MAC_ADDRESS20_LOW — Offset 3A4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3A4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.101 MAC_ADDRESS21_HIGH — Offset 3A8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3A8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.

Bit Range	Default & Access	Field Name (ID): Description
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.102 MAC_ADDRESS21_LOW — Offset 3ACh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3ACh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.103 MAC_ADDRESS22_HIGH — Offset 3B0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3B0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.104 MAC_ADDRESS22_LOW — Offset 3B4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3B4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.105 MAC_ADDRESS23_HIGH — Offset 3B8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3B8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.106 MAC_ADDRESS23_LOW — Offset 3BCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3BCh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.107 MAC_ADDRESS24_HIGH — Offset 3C0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3C0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.

Bit Range	Default & Access	Field Name (ID): Description
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.108 MAC_ADDRESS24_LOW — Offset 3C4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3C4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.109 MAC_ADDRESS25_HIGH — Offset 3C8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3C8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.110 MAC_ADDRESS25_LOW — Offset 3CCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3CCh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.111 MAC_ADDRESS26_HIGH — Offset 3D0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3D0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.112 MAC_ADDRESS26_LOW — Offset 3D4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3D4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.113 MAC_ADDRESS27_HIGH — Offset 3D8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3D8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.

Bit Range	Default & Access	Field Name (ID): Description
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.114 MAC_ADDRESS27_LOW — Offset 3DCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3DCh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.115 MAC_ADDRESS28_HIGH — Offset 3E0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3E0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.116 MAC_ADDRESS28_LOW — Offset 3E4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3E4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.117 MAC_ADDRESS29_HIGH — Offset 3E8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3E8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.118 MAC_ADDRESS29_LOW — Offset 3ECh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3ECh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.119 MAC_ADDRESS30_HIGH — Offset 3F0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3F0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.

Bit Range	Default & Access	Field Name (ID): Description
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.120 MAC_ADDRESS30_LOW — Offset 3F4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3F4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.121 MAC_ADDRESS31_HIGH — Offset 3F8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3F8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

10.2.122 MAC_ADDRESS31_LOW — Offset 3FCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3FCh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

10.2.123 MAC_ADDRESS32_HIGH — Offset 400h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 400h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.124 MAC_ADDRESS32_LOW — Offset 404h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 404h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.125 MAC_ADDRESS33_HIGH — Offset 408h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 408h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.126 MAC_ADDRESS33_LOW — Offset 40Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 40Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.127 MAC_ADDRESS34_HIGH — Offset 410h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 410h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.128 MAC_ADDRESS34_LOW — Offset 414h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 414h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.129 MAC_ADDRESS35_HIGH — Offset 418h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 418h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.130 MAC_ADDRESS35_LOW — Offset 41Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 41Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.131 MAC_ADDRESS36_HIGH — Offset 420h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 420h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.132 MAC_ADDRESS36_LOW — Offset 424h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 424h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.133 MAC_ADDRESS37_HIGH — Offset 428h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 428h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.134 MAC_ADDRESS37_LOW — Offset 42Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 42Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.135 MAC_ADDRESS38_HIGH — Offset 430h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 430h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.136 MAC_ADDRESS38_LOW — Offset 434h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 434h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.137 MAC_ADDRESS39_HIGH — Offset 438h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 438h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.138 MAC_ADDRESS39_LOW — Offset 43Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 43Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.139 MAC_ADDRESS40_HIGH — Offset 440h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 440h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.140 MAC_ADDRESS40_LOW — Offset 444h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 444h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.141 MAC_ADDRESS41_HIGH — Offset 448h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 448h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.142 MAC_ADDRESS41_LOW — Offset 44Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 44Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.143 MAC_ADDRESS42_HIGH — Offset 450h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 450h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.144 MAC_ADDRESS42_LOW — Offset 454h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 454h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.145 MAC_ADDRESS43_HIGH — Offset 458h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 458h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.146 MAC_ADDRESS43_LOW — Offset 45Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 45Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.147 MAC_ADDRESS44_HIGH — Offset 460h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 460h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.148 MAC_ADDRESS44_LOW — Offset 464h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 464h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.149 MAC_ADDRESS45_HIGH — Offset 468h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 468h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.150 MAC_ADDRESS45_LOW — Offset 46Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 46Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.151 MAC_ADDRESS46_HIGH — Offset 470h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 470h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.152 MAC_ADDRESS46_LOW — Offset 474h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 474h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.153 MAC_ADDRESS47_HIGH — Offset 478h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 478h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.154 MAC_ADDRESS47_LOW — Offset 47Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 47Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.155 MAC_ADDRESS48_HIGH — Offset 480h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 480h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.156 MAC_ADDRESS48_LOW — Offset 484h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 484h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.157 MAC_ADDRESS49_HIGH — Offset 488h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 488h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.158 MAC_ADDRESS49_LOW — Offset 48Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.159 MAC_ADDRESS50_HIGH — Offset 490h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 490h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.160 MAC_ADDRESS50_LOW — Offset 494h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 494h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.161 MAC_ADDRESS51_HIGH — Offset 498h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 498h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.162 MAC_ADDRESS51_LOW — Offset 49Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 49Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.163 MAC_ADDRESS52_HIGH — Offset 4A0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4A0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.164 MAC_ADDRESS52_LOW — Offset 4A4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4A4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.165 MAC_ADDRESS53_HIGH — Offset 4A8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4A8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.166 MAC_ADDRESS53_LOW — Offset 4ACh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4ACh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.167 MAC_ADDRESS54_HIGH — Offset 4B0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4B0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.168 MAC_ADDRESS54_LOW — Offset 4B4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4B4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.169 MAC_ADDRESS55_HIGH — Offset 4B8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4B8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.170 MAC_ADDRESS55_LOW — Offset 4BCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4BCh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.171 MAC_ADDRESS56_HIGH — Offset 4C0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4C0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.172 MAC_ADDRESS56_LOW — Offset 4C4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4C4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.173 MAC_ADDRESS57_HIGH — Offset 4C8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4C8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.174 MAC_ADDRESS57_LOW — Offset 4CCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4CCh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.175 MAC_ADDRESS58_HIGH — Offset 4D0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4D0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.176 MAC_ADDRESS58_LOW — Offset 4D4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4D4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.177 MAC_ADDRESS59_HIGH — Offset 4D8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4D8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.178 MAC_ADDRESS59_LOW — Offset 4DCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4DCh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.179 MAC_ADDRESS60_HIGH — Offset 4E0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4E0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.180 MAC_ADDRESS60_LOW — Offset 4E4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4E4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.181 MAC_ADDRESS61_HIGH — Offset 4E8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4E8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.182 MAC_ADDRESS61_LOW — Offset 4ECh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4ECh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.183 MAC_ADDRESS62_HIGH — Offset 4F0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4F0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.184 MAC_ADDRESS62_LOW — Offset 4F4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4F4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.185 MAC_ADDRESS63_HIGH — Offset 4F8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4F8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

10.2.186 MAC_ADDRESS63_LOW — Offset 4FCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4FCh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

10.2.187 MMC_CONTROL — Offset 700h

This register establishes the operating mode of MAC Management Counters.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 700h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**Update MMC Counters for Dropped Broadcast Packets (UCDBC):** Note: The CNTRST bit has a higher priority than the CNTPRST bit. Therefore, when the software tries to set both bits in the same write cycle, all counters are cleared and the CNTPRST bit is not set. When set, the MAC updates all related MMC Counters for Broadcast packets that are dropped because of the setting of the DBF bit of MAC_Packet_Filter register. When reset, the MMC Counters are not updated for dropped Broadcast packets. 0x0 (DISABLE): Update MMC Counters for Dropped Broadcast Packets is disabled. 0x1 (ENABLE): Update MMC Counters for Dropped Broadcast Packets is enabled.
7:6	0h RO	**Reserved**
5	0h RW	**Full-Half Preset (CNTPRSTLVL):** When this bit is low and the CNTPRST bit is set, all MMC counters get preset to almost-half value. All octet counters get preset to 0x7FFF_F800 (Half 2KBytes) and all packet-counters gets preset to 0x7FFF_FFF0 (Half 16). When this bit is high and the CNTPRST bit is set, all MMC counters get preset to almost-full value. All octet counters get preset to 0xFFFF_F800 (Full 2KBytes) and all packet-counters gets preset to 0xFFFF_FFF0 (Full 16). For 16-bit counters, the almost-half preset values are 0x7800 and 0x7FF0 for the respective octet and packet counters. Similarly, the almost-full preset values for the 16-bit counters are 0xF800 and 0xFFF0. 0x0 (DISABLE): Full-Half Preset is disabled. 0x1 (ENABLE): Full-Half Preset is enabled.
4	0h RW	**Counters Preset (CNTPRST):** When this bit is set, all counters are initialized or preset to almost full or almost half according to the CNTPRSTLVL bit. This bit is cleared automatically after 1 clock cycle. This bit, along with the CNTPRSTLVL bit, is useful for debugging and testing the assertion of interrupts because of MMC counter becoming half-full or full. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): Counters Preset is disabled. 0x1 (ENABLE): Counters Preset is enabled.
3	0h RW	**MMC Counter Freeze (CNTFREEZ):** When this bit is set, it freezes all MMC counters to their current value. Until this bit is reset to 0, no MMC counter is updated because of any transmitted or received packet. If any MMC counter is read with the Reset on Read bit set, then that counter is also cleared in this mode. 0x0 (DISABLE): MMC Counter Freeze is disabled. 0x1 (ENABLE): MMC Counter Freeze is enabled.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Reset on Read (RSTONRD):** When this bit is set, the MMC counters are reset to zero after Read (self-clearing after reset). The counters are cleared when the least significant byte lane (Bits[7:0]) is read. 0x0 (DISABLE): Reset on Read is disabled. 0x1 (ENABLE): Reset on Read is enabled.
1	0h RW	**Counter Stop Rollover (CNTSTOPRO):** When this bit is set, the counter does not roll over to zero after reaching the maximum value. 0x0 (DISABLE): Counter Stop Rollover is disabled. 0x1 (ENABLE): Counter Stop Rollover is enabled.
0	0h RW	**Counters Reset (CNTRST):** When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): Counters are not reset. 0x1 (ENABLE): All counters are reset.

10.2.188 MMC_RX_INTERRUPT — Offset 704h

This register maintains the interrupts generated from all Receive statistics counters.

The MMC Receive Interrupt register maintains the interrupts that are generated when the following occur:

- Receive statistic counters reach half of their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter).

- Receive statistic counters cross their maximum values (0xFFFF_FFFF for 32 bit counter and 0xFFFF for 16 bit counter).

When the Counter Stop Rollover is set, interrupts are set but the counter remains at all-ones. The MMC Receive Interrupt register

is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit.

Note: R_SS_RC means that this register bit is set internally, and it is cleared when the Counter register is read.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 704h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**MMC Receive LPI transition counter interrupt status (RXLPITRCIS):** This bit is set when the Rx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive LPI transition Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive LPI transition Counter Interrupt Status detected.
26	0h RO	**MMC Receive LPI microsecond counter interrupt status (RXLPIUSCIS):** This bit is set when the Rx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive LPI microsecond Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive LPI microsecond Counter Interrupt Status detected.
25	0h RO	**MMC Receive Control Packet Counter Interrupt Status (RXCTRLPIS):** This bit is set when the rxctrlpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Control Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Control Packet Counter Interrupt Status detected.
24	0h RO	**MMC Receive Error Packet Counter Interrupt Status (RXRCVERRPIS):** This bit is set when the rxrcverror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Error Packet Counter Interrupt Status detected.
23	0h RO	**MMC Receive Watchdog Error Packet Counter Interrupt Status (RXWDOGPIS):** This bit is set when the rxwatchdog error counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Watchdog Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Watchdog Error Packet Counter Interrupt Status detected.
22	0h RO	**MMC Receive VLAN Good Bad Packet Counter Interrupt Status (RXVLANGBPIS):** This bit is set when the rxvlanpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive VLAN Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive VLAN Good Bad Packet Counter Interrupt Status detected.
21	0h RO	**MMC Receive FIFO Overflow Packet Counter Interrupt Status (RXFOVPIS):** This bit is set when the rxfifooverflow counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive FIFO Overflow Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive FIFO Overflow Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**MMC Receive Pause Packet Counter Interrupt Status (RXPAUSPIS):** This bit is set when the rxpausepackets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Pause Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Pause Packet Counter Interrupt Status detected.
19	0h RO	**MMC Receive Out Of Range Error Packet Counter Interrupt Status. (RXORANGEPIS):** This bit is set when the rxoutofrangetype counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Out Of Range Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Out Of Range Error Packet Counter Interrupt Status detected.
18	0h RO	**MMC Receive Length Error Packet Counter Interrupt Status (RXLENERPIS):** This bit is set when the rxlengtherror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Length Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Length Error Packet Counter Interrupt Status detected.
17	0h RO	**MMC Receive Unicast Good Packet Counter Interrupt Status (RXUCGPIS):** This bit is set when the rxunicastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Unicast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Unicast Good Packet Counter Interrupt Status detected.
16	0h RO	**MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status (RX1024TMAXOCTGBPIS):** This bit is set when the rx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status detected.
15	0h RO	**MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Status (RX512T1023OCTGBPIS):** This bit is set when the rx512to1023octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Status detected.
14	0h RO	**MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Status (RX256T511OCTGBPIS):** This bit is set when the rx256to511octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Status (RX128T255OCTGBPIS):** This bit is set when the rx128to255octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Status detected.
12	0h RO	**MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Status (RX65T127OCTGBPIS):** This bit is set when the rx65to127octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Status detected.
11	0h RO	**MMC Receive 64 Octet Good Bad Packet Counter Interrupt Status (RX64OCTGBPIS):** This bit is set when the rx64octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Status detected.
10	0h RO	**MMC Receive Oversize Good Packet Counter Interrupt Status (RXOSIZEGPIS):** This bit is set when the rxoversize_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Oversize Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Oversize Good Packet Counter Interrupt Status detected.
9	0h RO	**MMC Receive Undersize Good Packet Counter Interrupt Status (RXUSIZEGPIS):** This bit is set when the rxundersize_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Undersize Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Undersize Good Packet Counter Interrupt Status detected.
8	0h RO	**MMC Receive Jabber Error Packet Counter Interrupt Status (RXJABERPIS):** This bit is set when the rxjabbererror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Jabber Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Jabber Error Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**MMC Receive Runt Packet Counter Interrupt Status (RXRUNTPIS):** This bit is set when the rxrunterror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Runt Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Runt Packet Counter Interrupt Status detected.
6	0h RO	**MMC Receive Alignment Error Packet Counter Interrupt Status (RXALGNERPIS):** This bit is set when the rxalignmenterror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Alignment Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Alignment Error Packet Counter Interrupt Status detected.
5	0h RO	**MMC Receive CRC Error Packet Counter Interrupt Status (RXCRCERPIS):** This bit is set when the rxcrcerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive CRC Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive CRC Error Packet Counter Interrupt Status detected.
4	0h RO	**MMC Receive Multicast Good Packet Counter Interrupt Status (RXMCGPIS):** This bit is set when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Multicast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Multicast Good Packet Counter Interrupt Status detected.
3	0h RO	**MMC Receive Broadcast Good Packet Counter Interrupt Status (RXBCGPIS):** This bit is set when the rxbroadcastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Broadcast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Broadcast Good Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**MMC Receive Good Octet Counter Interrupt Status (RXGOCTIS):** This bit is set when the rxoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Good Octet Counter Interrupt Status detected.
1	0h RO	**MMC Receive Good Bad Octet Counter Interrupt Status (RXGBOCTIS):** This bit is set when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Good Bad Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Good Bad Octet Counter Interrupt Status detected.
0	0h RO	**MMC Receive Good Bad Packet Counter Interrupt Status (RXGBPKTIS):** This bit is set when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Good Bad Packet Counter Interrupt Status detected.

10.2.189 MMC_TX_INTERRUPT — Offset 708h

This register maintains the interrupts generated from all Transmit statistics counters.

The MMC Transmit Interrupt register maintains the interrupts generated when transmit statistic counters reach half their maximum values

(0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32-bit counter and 0xFFFF for 16-bit counter).

When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones.

The MMC Transmit Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read.

The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 708h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**MMC Transmit LPI transition counter interrupt status (TXLPITRCIS):** This bit is set when the Tx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit LPI transition Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit LPI transition Counter Interrupt Status detected.
26	0h RO	**MMC Transmit LPI microsecond counter interrupt status (TXLPIUSCIS):** This bit is set when the Tx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit LPI microsecond Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit LPI microsecond Counter Interrupt Status detected.
25	0h RO	**MMC Transmit Oversize Good Packet Counter Interrupt Status (TXOSIZEGPIS):** This bit is set when the txoversize_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Oversize Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Oversize Good Packet Counter Interrupt Status detected.
24	0h RO	**MMC Transmit VLAN Good Packet Counter Interrupt Status (TXVLANGPIS):** This bit is set when the txvlanpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit VLAN Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit VLAN Good Packet Counter Interrupt Status detected.
23	0h RO	**MMC Transmit Pause Packet Counter Interrupt Status (TXPAUSPIS):** This bit is set when the txpausepacketserror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Pause Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Pause Packet Counter Interrupt Status detected.
22	0h RO	**MMC Transmit Excessive Deferral Packet Counter Interrupt Status (TXEXDEFPIS):** This bit is set when the txexcessdef counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Excessive Deferral Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Excessive Deferral Packet Counter Interrupt Status detected.
21	0h RO	**MMC Transmit Good Packet Counter Interrupt Status (TXGPKTIS):** This bit is set when the txpacketcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Good Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**MMC Transmit Good Octet Counter Interrupt Status (TXGOCTIS):** This bit is set when the txoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Good Octet Counter Interrupt Status detected.
19	0h RO	**MMC Transmit Carrier Error Packet Counter Interrupt Status (TXCARERPIS):** This bit is set when the txcarriererror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Carrier Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Carrier Error Packet Counter Interrupt Status detected.
18	0h RO	**MMC Transmit Excessive Collision Packet Counter Interrupt Status (TXEXCOLPIS):** This bit is set when the txexesscol counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Excessive Collision Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Excessive Collision Packet Counter Interrupt Status detected.
17	0h RO	**MMC Transmit Late Collision Packet Counter Interrupt Status (TXLATCOLPIS):** This bit is set when the txlatecol counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Late Collision Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Late Collision Packet Counter Interrupt Status detected.
16	0h RO	**MMC Transmit Deferred Packet Counter Interrupt Status (TXDEFPIS):** This bit is set when the txdeferred counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Deferred Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Deferred Packet Counter Interrupt Status detected.
15	0h RO	**MMC Transmit Multiple Collision Good Packet Counter Interrupt Status (TXMCOLGPIS):** This bit is set when the txmulticol_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Multiple Collision Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Multiple Collision Good Packet Counter Interrupt Status detected.
14	0h RO	**MMC Transmit Single Collision Good Packet Counter Interrupt Status (TXSCOLGPIS):** This bit is set when the txsinglecol_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Single Collision Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Single Collision Good Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**MMC Transmit Underflow Error Packet Counter Interrupt Status (TXUFLOWERPIS):** This bit is set when the txunderflowerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Underflow Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Underflow Error Packet Counter Interrupt Status detected.
12	0h RO	**MMC Transmit Broadcast Good Bad Packet Counter Interrupt Status (TXBCGBPIS):** This bit is set when the txbroadcastpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Broadcast Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Broadcast Good Bad Packet Counter Interrupt Status detected.
11	0h RO	**MMC Transmit Multicast Good Bad Packet Counter Interrupt Status (TXMCGBPIS):** The bit is set when the txmulticastpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Multicast Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Multicast Good Bad Packet Counter Interrupt Status detected.
10	0h RO	**MMC Transmit Unicast Good Bad Packet Counter Interrupt Status (TXUCGBPIS):** This bit is set when the txunicastpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Unicast Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Unicast Good Bad Packet Counter Interrupt Status detected.
9	0h RO	**MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status (TX1024TMAXOCTGBPIS):** This bit is set when the tx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status detected.
8	0h RO	**MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Status (TX512T1023OCTGBPIS):** This bit is set when the tx512to1023octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Status (TX256T511OCTGBPIS):** This bit is set when the tx256to511octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Status detected.
6	0h RO	**MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Status (TX128T255OCTGBPIS):** This bit is set when the tx128to255octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Status detected.
5	0h RO	**MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Status (TX65T127OCTGBPIS):** This bit is set when the tx65to127octets_gb counter reaches half the maximum value, and also when it reaches the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Status detected.
4	0h RO	**MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Status (TX64OCTGBPIS):** This bit is set when the tx64octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Status detected.
3	0h RO	**MMC Transmit Multicast Good Packet Counter Interrupt Status (TXMCGPIS):** This bit is set when the txmulticastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Multicast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Multicast Good Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**MMC Transmit Broadcast Good Packet Counter Interrupt Status (TXBCGPIS):** This bit is set when the txbroadcastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Broadcast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Broadcast Good Packet Counter Interrupt Status detected.
1	0h RO	**MMC Transmit Good Bad Packet Counter Interrupt Status (TXGBPKTIS):** This bit is set when the txpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Good Bad Packet Counter Interrupt Status detected.
0	0h RO	**MMC Transmit Good Bad Octet Counter Interrupt Status (TXGBOCTIS):** This bit is set when the txoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Good Bad Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Good Bad Octet Counter Interrupt Status detected.

10.2.190 MMC_RX_INTERRUPT_MASK — Offset 70Ch

This register maintains the masks for interrupts generated from all Receive statistics counters.

The MMC Receive Interrupt Mask register maintains the masks for the interrupts generated when receive statistic counters reach half of their maximum value or the maximum values.

This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 70Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RW	**MMC Receive LPI transition counter interrupt Mask (RXLPITRCIM):** Setting this bit masks the interrupt when the Rx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive LPI transition counter interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive LPI transition counter interrupt Mask is enabled.
26	0h RW	**MMC Receive LPI microsecond counter interrupt Mask (RXLPIUSCIM):** Setting this bit masks the interrupt when the Rx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive LPI microsecond counter interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive LPI microsecond counter interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RW	**MMC Receive Control Packet Counter Interrupt Mask (RXCTRLPIM):** Setting this bit masks the interrupt when the rxctrlpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Control Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Control Packet Counter Interrupt Mask is enabled.
24	0h RW	**MMC Receive Error Packet Counter Interrupt Mask (RXRCVERRPIM):** Setting this bit masks the interrupt when the rxrcverror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Error Packet Counter Interrupt Mask is enabled.
23	0h RW	**MMC Receive Watchdog Error Packet Counter Interrupt Mask (RXWDOGPIM):** Setting this bit masks the interrupt when the rxwatchdog counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Watchdog Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Watchdog Error Packet Counter Interrupt Mask is enabled.
22	0h RW	**MMC Receive VLAN Good Bad Packet Counter Interrupt Mask (RXVLANGBPIM):** Setting this bit masks the interrupt when the rxvlanpackets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive VLAN Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive VLAN Good Bad Packet Counter Interrupt Mask is enabled.
21	0h RW	**MMC Receive FIFO Overflow Packet Counter Interrupt Mask (RXFOVPIM):** Setting this bit masks the interrupt when the rxfifooverflow counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive FIFO Overflow Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive FIFO Overflow Packet Counter Interrupt Mask is enabled.
20	0h RW	**MMC Receive Pause Packet Counter Interrupt Mask (RXPAUSPIM):** Setting this bit masks the interrupt when the rxpausepackets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Pause Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Pause Packet Counter Interrupt Mask is enabled.
19	0h RW	**MMC Receive Out Of Range Error Packet Counter Interrupt Mask (RXORANGEPIM):** Setting this bit masks the interrupt when the rxoutofrangetype counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Out Of Range Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Out Of Range Error Packet Counter Interrupt Mask is enabled.
18	0h RW	**MMC Receive Length Error Packet Counter Interrupt Mask (RXLENERPIM):** Setting this bit masks the interrupt when the rxlengtherror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Length Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Length Error Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**MMC Receive Unicast Good Packet Counter Interrupt Mask (RXUCGPIM):** Setting this bit masks the interrupt when the rxunicastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Unicast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Unicast Good Packet Counter Interrupt Mask is enabled.
16	0h RW	**MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask. (RX1024TMAXOCTGBPIM):** Setting this bit masks the interrupt when the rx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask is enabled.
15	0h RW	**MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask (RX512T1023OCTGBPIM):** Setting this bit masks the interrupt when the rx512to1023octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask is enabled.
14	0h RW	**MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Mask (RX256T511OCTGBPIM):** Setting this bit masks the interrupt when the rx256to511octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Mask is enabled.
13	0h RW	**MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Mask (RX128T255OCTGBPIM):** Setting this bit masks the interrupt when the rx128to255octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Mask is enabled.
12	0h RW	**MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Mask (RX65T127OCTGBPIM):** Setting this bit masks the interrupt when the rx65to127octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Mask is enabled.
11	0h RW	**MMC Receive 64 Octet Good Bad Packet Counter Interrupt Mask (RX64OCTGBPIM):** Setting this bit masks the interrupt when the rx64octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**MMC Receive Oversize Good Packet Counter Interrupt Mask (RXOSIZEGPIM):** Setting this bit masks the interrupt when the rxoversize_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Oversize Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Oversize Good Packet Counter Interrupt Mask is enabled.
9	0h RW	**MMC Receive Undersize Good Packet Counter Interrupt Mask (RXUSIZEGPIM):** Setting this bit masks the interrupt when the rxundersize_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Undersize Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Undersize Good Packet Counter Interrupt Mask is enabled.
8	0h RW	**MMC Receive Jabber Error Packet Counter Interrupt Mask (RXJABERPIM):** Setting this bit masks the interrupt when the rxjabbererror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Jabber Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Jabber Error Packet Counter Interrupt Mask is enabled.
7	0h RW	**MMC Receive Runt Packet Counter Interrupt Mask (RXRUNTPIM):** Setting this bit masks the interrupt when the rxrunterror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Runt Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Runt Packet Counter Interrupt Mask is enabled.
6	0h RW	**MMC Receive Alignment Error Packet Counter Interrupt Mask (RXALGNERPIM):** Setting this bit masks the interrupt when the rxalignmenterror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Alignment Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Alignment Error Packet Counter Interrupt Mask is enabled.
5	0h RW	**MMC Receive CRC Error Packet Counter Interrupt Mask (RXCRCERPIM):** Setting this bit masks the interrupt when the rxcrcerror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive CRC Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive CRC Error Packet Counter Interrupt Mask is enabled.
4	0h RW	**MMC Receive Multicast Good Packet Counter Interrupt Mask (RXMCGPIM):** Setting this bit masks the interrupt when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Multicast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Multicast Good Packet Counter Interrupt Mask is enabled.
3	0h RW	**MMC Receive Broadcast Good Packet Counter Interrupt Mask (RXBCGPIM):** Setting this bit masks the interrupt when the rxbroadcastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Broadcast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Broadcast Good Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**MMC Receive Good Octet Counter Interrupt Mask (RXGOCTIM):** Setting this bit masks the interrupt when the rxoctetcount_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Good Octet Counter Interrupt Mask is enabled.
1	0h RW	**MMC Receive Good Bad Octet Counter Interrupt Mask (RXGBOCTIM):** Setting this bit masks the interrupt when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Good Bad Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Good Bad Octet Counter Interrupt Mask is enabled.
0	0h RW	**MMC Receive Good Bad Packet Counter Interrupt Mask (RXGBPKTIM):** Setting this bit masks the interrupt when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Good Bad Packet Counter Interrupt Mask is enabled.

10.2.191 MMC_TX_INTERRUPT_MASK — Offset 710h

This register maintains the masks for interrupts generated from all Transmit statistics counters.

The MMC Transmit Interrupt Mask register maintains the masks for the interrupts generated when the transmit statistic counters reach half of their maximum value or the maximum values. This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 710h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RW	**MMC Transmit LPI transition counter interrupt Mask (TXLPITRCIM):** Setting this bit masks the interrupt when the Tx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit LPI transition counter interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit LPI transition counter interrupt Mask is enabled.
26	0h RW	**MMC Transmit LPI microsecond counter interrupt Mask (TXLPIUSCIM):** Setting this bit masks the interrupt when the Tx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit LPI microsecond counter interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit LPI microsecond counter interrupt Mask is enabled.
25	0h RW	**MMC Transmit Oversize Good Packet Counter Interrupt Mask (TXOSIZEGPIM):** Setting this bit masks the interrupt when the txoversize_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Oversize Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Oversize Good Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**MMC Transmit VLAN Good Packet Counter Interrupt Mask (TXVLANGPIM):** Setting this bit masks the interrupt when the txvlanpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit VLAN Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit VLAN Good Packet Counter Interrupt Mask is enabled.
23	0h RW	**MMC Transmit Pause Packet Counter Interrupt Mask (TXPAUSPIM):** Setting this bit masks the interrupt when the txpausepackets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Pause Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Pause Packet Counter Interrupt Mask is enabled.
22	0h RW	**MMC Transmit Excessive Deferral Packet Counter Interrupt Mask (TXEXDEFPIM):** Setting this bit masks the interrupt when the txexcessdef counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Excessive Deferral Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Excessive Deferral Packet Counter Interrupt Mask is enabled.
21	0h RW	**MMC Transmit Good Packet Counter Interrupt Mask (TXGPKTIM):** Setting this bit masks the interrupt when the txpacketcount_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Good Packet Counter Interrupt Mask is enabled.
20	0h RW	**MMC Transmit Good Octet Counter Interrupt Mask (TXGOCTIM):** Setting this bit masks the interrupt when the txoctetcount_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Good Octet Counter Interrupt Mask is enabled.
19	0h RW	**MMC Transmit Carrier Error Packet Counter Interrupt Mask (TXCARERPIM):** Setting this bit masks the interrupt when the txcarriererror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Carrier Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Carrier Error Packet Counter Interrupt Mask is enabled.
18	0h RW	**MMC Transmit Excessive Collision Packet Counter Interrupt Mask (TXEXCOLPIM):** Setting this bit masks the interrupt when the txexcesscol counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Excessive Collision Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Excessive Collision Packet Counter Interrupt Mask is enabled.
17	0h RW	**MMC Transmit Late Collision Packet Counter Interrupt Mask (TXLATCOLPIM):** Setting this bit masks the interrupt when the txlatecol counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Late Collision Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Late Collision Packet Counter Interrupt Mask is enabled.
16	0h RW	**MMC Transmit Deferred Packet Counter Interrupt Mask (TXDEFPIM):** Setting this bit masks the interrupt when the txdeferred counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Deferred Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Deferred Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**MMC Transmit Multiple Collision Good Packet Counter Interrupt Mask (TXMCOLGPIM):** Setting this bit masks the interrupt when the txmulticol_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Multiple Collision Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Multiple Collision Good Packet Counter Interrupt Mask is enabled.
14	0h RW	**MMC Transmit Single Collision Good Packet Counter Interrupt Mask (TXSCOLGPIM):** Setting this bit masks the interrupt when the txsinglecol_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Single Collision Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Single Collision Good Packet Counter Interrupt Mask is enabled.
13	0h RW	**MMC Transmit Underflow Error Packet Counter Interrupt Mask (TXUFLOWERPIM):** Setting this bit masks the interrupt when the txunderflowerror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Underflow Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Underflow Error Packet Counter Interrupt Mask is enabled.
12	0h RW	**MMC Transmit Broadcast Good Bad Packet Counter Interrupt Mask (TXBCGBPIM):** Setting this bit masks the interrupt when the txbroadcastpackets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Broadcast Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Broadcast Good Bad Packet Counter Interrupt Mask is enabled.
11	0h RW	**MMC Transmit Multicast Good Bad Packet Counter Interrupt Mask (TXMCGBPIM):** Setting this bit masks the interrupt when the txmulticastpackets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Multicast Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Multicast Good Bad Packet Counter Interrupt Mask is enabled.
10	0h RW	**MMC Transmit Unicast Good Bad Packet Counter Interrupt Mask (TXUCGBPIM):** Setting this bit masks the interrupt when the txunicastpackets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Unicast Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Unicast Good Bad Packet Counter Interrupt Mask is enabled.
9	0h RW	**MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask (TX1024TMAXOCTGBPIM):** Setting this bit masks the interrupt when the tx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask (TX512T1023OCTGBPIM):** Setting this bit masks the interrupt when the tx512to1023octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask is enabled.
7	0h RW	**MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Mask (TX256T511OCTGBPIM):** Setting this bit masks the interrupt when the tx256to511octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Mask is enabled.
6	0h RW	**MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Mask (TX128T255OCTGBPIM):** Setting this bit masks the interrupt when the tx128to255octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Mask is enabled.
5	0h RW	**MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Mask (TX65T127OCTGBPIM):** Setting this bit masks the interrupt when the tx65to127octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Mask is enabled.
4	0h RW	**MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Mask (TX64OCTGBPIM):** Setting this bit masks the interrupt when the tx64octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Mask is enabled.
3	0h RW	**MMC Transmit Multicast Good Packet Counter Interrupt Mask (TXMCGPIM):** Setting this bit masks the interrupt when the txmulticastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Multicast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Multicast Good Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**MMC Transmit Broadcast Good Packet Counter Interrupt Mask (TXBCGPIM):** Setting this bit masks the interrupt when the txbroadcastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Broadcast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Broadcast Good Packet Counter Interrupt Mask is enabled.
1	0h RW	**MMC Transmit Good Bad Packet Counter Interrupt Mask (TXGBPKTIM):** Setting this bit masks the interrupt when the txpacketcount_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Good Bad Packet Counter Interrupt Mask is enabled.
0	0h RW	**MMC Transmit Good Bad Octet Counter Interrupt Mask (TXGBOCTIM):** Setting this bit masks the interrupt when the txoctetcount_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Good Bad Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Good Bad Octet Counter Interrupt Mask is enabled.

10.2.192 TX_OCTET_COUNT_GOOD_BAD — Offset 714h

This register provides the number of bytes transmitted by the GbE Controller, exclusive of preamble and retried bytes, in good and bad packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 714h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Octet Count Good Bad (TXOCTGB):** This field indicates the number of bytes transmitted, exclusive of preamble and retried bytes, in good and bad packets.

10.2.193 TX_PACKET_COUNT_GOOD_BAD — Offset 718h

This register provides the number of good and bad packets transmitted by GbE Controller, exclusive of retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 718h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Packet Count Good Bad (TXPKTGB):** This field indicates the number of good and bad packets transmitted, exclusive of retried packets.

10.2.194 TX_BROADCAST_PACKETS_GOOD — Offset 71Ch

This register provides the number of good broadcast packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 71Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Broadcast Packets Good (TXBCASTG):** This field indicates the number of good broadcast packets transmitted.

10.2.195 TX_MULTICAST_PACKETS_GOOD — Offset 720h

This register provides the number of good multicast packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 720h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Multicast Packets Good (TXMCASTG):** This field indicates the number of good multicast packets transmitted.

10.2.196 TX_64OCTETS_PACKETS_GOOD_BAD — Offset 724h

This register provides the number of good and bad packets transmitted by GbE Controller with length 64 bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 724h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx 64Octets Packets Good_Bad (TX64OCTGB):** This field indicates the number of good and bad packets transmitted with length 64 bytes, exclusive of preamble and retried packets.

10.2.197 TX_65TO127OCTETS_PACKETS_GOOD_BAD — Offset 728h

This register provides the number of good and bad packets transmitted by GbE Controller with length between 65 and 127 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 728h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TX65_127OCTGB:** Tx 65To127Octets Packets Good Bad This field indicates the number of good and bad packets transmitted with length between 65 and 127 (inclusive) bytes, exclusive of preamble and retried packets.

10.2.198 TX_128TO255OCTETS_PACKETS_GOOD_BAD — Offset 72Ch

This register provides the number of good and bad packets transmitted by GbE Controller with length between 128 to 255 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 72Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx 128To255Octets Packets Good Bad (TX128_255OCTGB):** This field indicates the number of good and bad packets transmitted with length between 128 and 255 (inclusive) bytes, exclusive of preamble and retried packets.

10.2.199 TX_256TO511OCTETS_PACKETS_GOOD_BAD — Offset 730h

This register provides the number of good and bad packets transmitted by GbE Controller with length between 256 to 511 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 730h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx 256To511Octets Packets Good Bad (TX256_511OCTGB):** This field indicates the number of good and bad packets transmitted with length between 256 and 511 (inclusive) bytes, exclusive of preamble and retried packets.

10.2.200 TX_512TO1023OCTETS_PACKETS_GOOD_BAD — Offset 734h

This register provides the number of good and bad packets transmitted by GbE Controller with length 512 to 1023 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 734h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx 512To1023Octets Packets Good Bad (TX512_1023OCTGB):** This field indicates the number of good and bad packets transmitted with length between 512 and 1023 (inclusive) bytes, exclusive of preamble and retried packets.

10.2.201 TX_1024TOMAXOCTETS_PACKETS_GOOD_BAD — Offset 738h

This register provides the number of good and bad packets transmitted by GbE Controller with length 1024 to maxsize (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 738h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx 1024ToMaxOctets Packets Good Bad (TX1024_MAXOCTGB):** This field indicates the number of good and bad packets transmitted with length between 1024 and maxsize (inclusive) bytes, exclusive of preamble and retried packets.

10.2.202 TX_UNICAST_PACKETS_GOOD_BAD — Offset 73Ch

This register provides the number of good and bad unicast packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 73Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Unicast Packets Good Bad (TXUCASTGB):** This field indicates the number of good and bad unicast packets transmitted.

10.2.203 TX_MULTICAST_PACKETS_GOOD_BAD — Offset 740h

This register provides the number of good and bad multicast packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 740h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Multicast Packets Good Bad (TXMCASTGB):** This field indicates the number of good and bad multicast packets transmitted.

10.2.204 TX_BROADCAST_PACKETS_GOOD_BAD — Offset 744h

This register provides the number of good and bad broadcast packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 744h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Broadcast Packets Good Bad (TXBCASTGB):** This field indicates the number of good and bad broadcast packets transmitted.

10.2.205 TX_UNDERFLOW_ERROR_PACKETS — Offset 748h

This register provides the number of packets aborted by GbE Controller because of packets underflow error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 748h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Underflow Error Packets (TXUNDRFLW):** This field indicates the number of packets aborted because of packets underflow error.

10.2.206 TX_SINGLE_COLLISION_GOOD_PACKETS — Offset 74Ch

This register provides the number of successfully transmitted packets by GbE Controller after a single collision in the half-duplex mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 74Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Single Collision Good Packets (TXSNGLCOLG):** This field indicates the number of successfully transmitted packets after a single collision in the half-duplex mode.

10.2.207 TX_MULTIPLE_COLLISION_GOOD_PACKETS — Offset 750h

This register provides the number of successfully transmitted packets by GbE Controller after multiple collisions in the half-duplex mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 750h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Multiple Collision Good Packets (TXMULTCOLG):** This field indicates the number of successfully transmitted packets after multiple collisions in the half-duplex mode.

10.2.208 TX_DEFERRED_PACKETS — Offset 754h

This register provides the number of successfully transmitted by GbE Controller after a deferral in the half-duplex mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 754h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Deferred Packets (TXDEFRD):** This field indicates the number of successfully transmitted after a deferral in the half-duplex mode.

10.2.209 TX_LATE_COLLISION_PACKETS — Offset 758h

This register provides the number of packets aborted by GbE Controller because of late collision error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 758h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Late Collision Packets (TXLATECOL):** This field indicates the number of packets aborted because of late collision error.

10.2.210 TX_EXCESSIVE_COLLISION_PACKETS — Offset 75Ch

This register provides the number of packets aborted by GbE Controller because of excessive (16) collision errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 75Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Excessive Collision Packets (TXEXSCOL):** This field indicates the number of packets aborted because of excessive (16) collision errors.

10.2.211 TX_CARRIER_ERROR_PACKETS — Offset 760h

This register provides the number of packets aborted by GbE Controller because of carrier sense error (no carrier or loss of carrier).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 760h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Carrier Error Packets (TXCARR):** This field indicates the number of packets aborted because of carrier sense error (no carrier or loss of carrier).

10.2.212 TX_OCTET_COUNT_GOOD — Offset 764h

This register provides the number of bytes transmitted by GbE Controller, exclusive of preamble, only in good packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 764h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Octet Count Good (TXOCTG):** This field indicates the number of bytes transmitted, exclusive of preamble, only in good packets.

10.2.213 TX_PACKET_COUNT_GOOD — Offset 768h

This register provides the number of good packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 768h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Packet Count Good (TXPKTG):** This field indicates the number of good packets transmitted.

10.2.214 TX_EXCESSIVE_DEFERRAL_ERROR — Offset 76Ch

This register provides the number of packets aborted by GbE Controller because of excessive deferral error (deferred for more than two max-sized packet times).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 76Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Excessive Deferral Error (TXEXSDEF):** This field indicates the number of packets aborted because of excessive deferral error (deferred for more than two max-sized packet times).

10.2.215 TX_PAUSE_PACKETS — Offset 770h

This register provides the number of good Pause packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 770h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Pause Packets (TXPAUSE):** This field indicates the number of good Pause packets transmitted.

10.2.216 TX_VLAN_PACKETS_GOOD — Offset 774h

This register provides the number of good VLAN packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 774h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx VLAN Packets Good (TXVLANG):** This field provides the number of good VLAN packets transmitted.

10.2.217 TX_OSIZE_PACKETS_GOOD — Offset 778h

This register provides the number of packets transmitted by GbE Controller without errors and with length greater than the maxsize (1,518 or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in S2KP bit of the MAC_Configuration register).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 778h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx OSize Packets Good (TXOSIZG):** This field indicates the number of packets transmitted without errors and with length greater than the maxsize (1,518 or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in S2KP bit of the MAC_Configuration register).

10.2.218 RX_PACKETS_COUNT_GOOD_BAD — Offset 780h

This register provides the number of good and bad packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 780h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Packets Count Good Bad (RXPKTGB):** This field indicates the number of good and bad packets received.

10.2.219 RX_OCTET_COUNT_GOOD_BAD — Offset 784h

This register provides the number of bytes received, exclusive of preamble, in good and bad packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 784h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Octet Count Good Bad (RXOCTGB):** This field indicates the number of bytes received, exclusive of preamble, in good and bad packets.

10.2.220 RX_OCTET_COUNT_GOOD — Offset 788h

This register provides the number of bytes received by GbE Controller, exclusive of preamble, only in good packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 788h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Octet Count Good (RXOCTG):** This field indicates the number of bytes received, exclusive of preamble, only in good packets.

10.2.221 RX_BROADCAST_PACKETS_GOOD — Offset 78Ch

This register provides the number of good broadcast packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 78Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Broadcast Packets Good (RXBCASTG):** This field indicates the number of good broadcast packets received.

10.2.222 RX_MULTICAST_PACKETS_GOOD — Offset 790h

This register provides the number of good multicast packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 790h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Multicast Packets Good (RXMCASTG):** This field indicates the number of good multicast packets received.

10.2.223 RX_CRC_ERROR_PACKETS — Offset 794h

This register provides the number of packets received by GbE Controller with CRC error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 794h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx CRC Error Packets (RXCRCERR):** This field indicates the number of packets received with CRC error.

10.2.224 RX_ALIGNMENT_ERROR_PACKETS — Offset 798h

This register provides the number of packets received by GbE Controller with alignment (dribble) error. It is valid only in 10/100 mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 798h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Alignment Error Packets (RXALGNERR):** This field indicates the number of packets received with alignment (dribble) error. It is valid only in 10/100 mode.

10.2.225 RX_RUNT_ERROR_PACKETS — Offset 79Ch

This register provides the number of packets received by GbE Controller with runt (length less than 64 bytes and CRC error) error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 79Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Runt Error Packets (RXRUNTERR):** This field indicates the number of packets received with runt (length less than 64 bytes and CRC error) error.

10.2.226 RX_JABBER_ERROR_PACKETS — Offset 7A0h

This register provides the number of giant packets received by GbE Controller with length (including CRC) greater than 1,518 bytes (1,522 bytes for VLAN tagged) and with CRC error. If Jumbo Packet mode is enabled, packets of length greater than 9,018 bytes (9,022 bytes for VLAN tagged) are considered as giant packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Jabber Error Packets (RXJABERR):** This field indicates the number of giant packets received with length (including CRC) greater than 1,518 bytes (1,522 bytes for VLAN tagged) and with CRC error. If Jumbo Packet mode is enabled, packets of length greater than 9,018 bytes (9,022 bytes for VLAN tagged) are considered as giant packets.

10.2.227 RX_UNDERSIZE_PACKETS_GOOD — Offset 7A4h

This register provides the number of packets received by GbE Controller with length less than 64 bytes, without any errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Undersize Packets Good (RXUNDERSZG):** This field indicates the number of packets received with length less than 64 bytes, without any errors.

10.2.228 RX_OVERSIZE_PACKETS_GOOD — Offset 7A8h

This register provides the number of packets received by GbE Controller without errors, with length greater than the maxsize (1,518 bytes or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in the S2KP bit of the MAC_Configuration register).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Oversize Packets Good (RXOVERSZG):** This field indicates the number of packets received without errors, with length greater than the maxsize (1,518 bytes or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in the S2KP bit of the MAC_Configuration register).

10.2.229 RX_64OCTETS_PACKETS_GOOD_BAD — Offset 7ACh

This register provides the number of good and bad packets received by GbE Controller with length 64 bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx 64 Octets Packets Good Bad (RX64OCTGB):** This field indicates the number of good and bad packets received with length 64 bytes, exclusive of the preamble.

10.2.230 RX_65TO127OCTETS_PACKETS_GOOD_BAD — Offset 7B0h

This register provides the number of good and bad packets received by GbE Controller with length between 65 and 127 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RX65_127OCTGB:** Rx 65-127 Octets Packets Good Bad This field indicates the number of good and bad packets received with length between 65 and 127 (inclusive) bytes, exclusive of the preamble.

10.2.231 RX_128TO255OCTETS_PACKETS_GOOD_BAD — Offset 7B4h

This register provides the number of good and bad packets received by GbE Controller with length between 128 and 255 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RX128_255OCTGB:** Rx 128-255 Octets Packets Good Bad This field indicates the number of good and bad packets received with length between 128 and 255 (inclusive) bytes, exclusive of the preamble.

10.2.232 RX_256TO511OCTETS_PACKETS_GOOD_BAD — Offset 7B8h

This register provides the number of good and bad packets received by GbE ControllerGbE Controller with length between 256 and 511 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RX256_511OCTGB:** Rx 256-511 Octets Packets Good Bad This field indicates the number of good and bad packets received with length between 256 and 511 (inclusive) bytes, exclusive of the preamble.

10.2.233 RX_512TO1023OCTETS_PACKETS_GOOD_BAD — Offset 7BCh

This register provides the number of good and bad packets received by GbE Controller with length between 512 and 1023 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RX 512-1023 Octets Packets Good Bad (RX512_1023OCTGB):** This field indicates the number of good and bad packets received with length between 512 and 1023 (inclusive) bytes, exclusive of the preamble.

10.2.234 RX_1024TOMAXOCTETS_PACKETS_GOOD_BAD — Offset 7C0h

This register provides the number of good and bad packets received by GbE Controller with length between 1024 and maxsize (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx 1024-Max Octets Good Bad (RX1024_MAXOCTGB):** This field indicates the number of good and bad packets received with length between 1024 and maxsize (inclusive) bytes, exclusive of the preamble.

10.2.235 RX_UNICAST_PACKETS_GOOD — Offset 7C4h

This register provides the number of good unicast packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Unicast Packets Good (RXUCASTG):** This field indicates the number of good unicast packets received.

10.2.236 RX_LENGTH_ERROR_PACKETS — Offset 7C8h

This register provides the number of packets received by GbE Controller with length error (Length Type field not equal to packet size), for all packets with valid length field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Length Error Packets (RXLENERR):** This field indicates the number of packets received with length error (Length Type field not equal to packet size), for all packets with valid length field.

10.2.237 RX_OUT_OF_RANGE_TYPE_PACKETS — Offset 7CCh

This register provides the number of packets received by GbE Controller with length field not equal to the valid packet size (greater than 1,500 but less than 1,536).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Out of Range Type Packet (RXOUTOFRNG):** This field indicates the number of packets received with length field not equal to the valid packet size (greater than 1,500 but less than 1,536).

10.2.238 RX_PAUSE_PACKETS — Offset 7D0h

This register provides the number of good and valid Pause packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Pause Packets (RXPAUSEPKT):** This field indicates the number of good and valid Pause packets received.

10.2.239 RX_FIFO_OVERFLOW_PACKETS — Offset 7D4h

This register provides the number of missed received packets because of FIFO overflow in GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx FIFO Overflow Packets (RXFIFOOVFL):** This field indicates the number of missed received packets because of FIFO overflow.

10.2.240 RX_VLAN_PACKETS_GOOD_BAD — Offset 7D8h

This register provides the number of good and bad VLAN packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx VLAN Packets Good Bad (RXVLANPKTGB):** This field indicates the number of good and bad VLAN packets received.

10.2.241 RX_WATCHDOG_ERROR_PACKETS — Offset 7DCh

This register provides the number of packets received by GbE Controller with error because of watchdog timeout error (packets with a data load larger than 2,048 bytes (when JE and WD bits are reset in MAC_Configuration register), 10,240 bytes (when JE bit is set and WD bit is reset in MAC_Configuration register), 16,384 bytes (when WD bit is set in MAC_Configuration register) or the value programmed in the MAC_Watchdog_Timeout register).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Watchdog Error Packets (RXWDGERR):** This field indicates the number of packets received with error because of watchdog timeout error (packets with a data load larger than 2,048 bytes (when JE and WD bits are reset in MAC_Configuration register), 10,240 bytes (when JE bit is set and WD bit is reset in MAC_Configuration register), 16,384 bytes (when WD bit is set in MAC_Configuration register) or the value programmed in the MAC_Watchdog_Timeout register).

10.2.242 RX_RECEIVE_ERROR_PACKETS — Offset 7E0h

This register provides the number of packets received by GbE Controller with Receive error or Packet Extension error on the GMII or MII interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Receive Error Packets (RXRCVERR):** This field indicates the number of packets received with Receive error or Packet Extension error on the GMII or MII interface.

10.2.243 RX_CONTROL_PACKETS_GOOD — Offset 7E4h

This register provides the number of good control packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Control Packets Good (RXCTRLG):** This field indicates the number of good control packets received.

10.2.244 TX_LPI_USEC_CNTR — Offset 7ECh

This register provides the number of microseconds Tx LPI is asserted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx LPI Microseconds Counter (TXLPIUSC):** This field indicates the number of microseconds Tx LPI is asserted. For every Tx LPI Entry and Exit, the Timer value can have an error of +/- 1 microsecond.

10.2.245 TX_LPI_TRAN_CNTR — Offset 7F0h

This register provides the number of times GbE Controller has entered Tx LPI.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7F0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx LPI Transition counter (TXLPITRC):** This field indicates the number of times Tx LPI Entry has occurred. Even if Tx LPI Entry occurs in Automate Mode (because of LPITXA bit set in the LPI Control and Status register), the counter increments.

10.2.246 RX_LPI_USEC_CNTR — Offset 7F4h

This register provides the number of microseconds Rx LPI is sampled by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7F4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx LPI Microseconds Counter (RXLPIUSC):** This field indicates the number of microseconds Rx LPI is asserted. For every Rx LPI Entry and Exit, the Timer value can have an error of +/- 1 microsecond.

10.2.247 RX_LPI_TRAN_CNTR — Offset 7F8h

This register provides the number of times GbE Controller has entered Rx LPI.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx LPI Transition counter (RXLPITRC):** This field indicates the number of times Rx LPI Entry has occurred.

10.2.248 MMC_IPC_RX_INTERRUPT_MASK — Offset 800h

This register maintains the mask for the interrupt generated from the receive IPC statistic counters.

The MMC Receive Checksum Off load Interrupt Mask register maintains the masks for the interrupts generated when the receive IPC (Checksum Off load) statistic counters reach half their maximum value, and when they reach their maximum values. This register is 32 bits wide.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 800h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW	**MMC Receive ICMP Error Octet Counter Interrupt Mask (RXICMPEROIM):** Setting this bit masks the interrupt when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive ICMP Error Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive ICMP Error Octet Counter Interrupt Mask is enabled.
28	0h RW	**MMC Receive ICMP Good Octet Counter Interrupt Mask (RXICMPGOIM):** Setting this bit masks the interrupt when the rxicmp_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive ICMP Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive ICMP Good Octet Counter Interrupt Mask is enabled.
27	0h RW	**MMC Receive TCP Error Octet Counter Interrupt Mask (RXTCPEROIM):** Setting this bit masks the interrupt when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive TCP Error Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive TCP Error Octet Counter Interrupt Mask is enabled.
26	0h RW	**MMC Receive TCP Good Octet Counter Interrupt Mask (RXTCPGOIM):** Setting this bit masks the interrupt when the rxtcp_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive TCP Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive TCP Good Octet Counter Interrupt Mask is enabled.
25	0h RW	**MMC Receive UDP Good Octet Counter Interrupt Mask (RXUDPEROIM):** Setting this bit masks the interrupt when the rxudp_err_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive UDP Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive UDP Good Octet Counter Interrupt Mask is enabled.
24	0h RW	**MMC Receive IPV6 No Payload Octet Counter Interrupt Mask (RXUDPGOIM):** Setting this bit masks the interrupt when the rxudp_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 No Payload Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 No Payload Octet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**MMC Receive IPV6 Header Error Octet Counter Interrupt Mask (RXIPV6NOPAYOIM):** Setting this bit masks the interrupt when the rxipv6_nopay_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 Header Error Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Header Error Octet Counter Interrupt Mask is enabled.
22	0h RW	**MMC Receive IPV6 Good Octet Counter Interrupt Mask (RXIPV6HEROIM):** Setting this bit masks the interrupt when the rxipv6_hdrerr_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Good Octet Counter Interrupt Mask is enabled.
21	0h RW	**MMC Receive IPV6 Good Octet Counter Interrupt Mask (RXIPV6GOIM):** Setting this bit masks the interrupt when the rxipv6_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Good Octet Counter Interrupt Mask is enabled.
20	0h RW	**MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Mask (RXIPV4UDSBLOIM):** Setting this bit masks the interrupt when the rxipv4_udsbl_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Mask is enabled.
19	0h RW	**MMC Receive IPV4 Fragmented Octet Counter Interrupt Mask (RXIPV4FRAGOIM):** Setting this bit masks the interrupt when the rxipv4_frag_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Fragmented Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Fragmented Octet Counter Interrupt Mask is enabled.
18	0h RW	**MMC Receive IPV4 No Payload Octet Counter Interrupt Mask (RXIPV4NOPAYOIM):** Setting this bit masks the interrupt when the rxipv4_nopay_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 No Payload Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 No Payload Octet Counter Interrupt Mask is enabled.
17	0h RW	**MMC Receive IPV4 Header Error Octet Counter Interrupt Mask (RXIPV4HEROIM):** Setting this bit masks the interrupt when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Header Error Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Header Error Octet Counter Interrupt Mask is enabled.
16	0h RW	**MMC Receive IPV4 Good Octet Counter Interrupt Mask (RXIPV4GOIM):** Setting this bit masks the interrupt when the rxipv4_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Good Octet Counter Interrupt Mask is enabled.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**MMC Receive ICMP Error Packet Counter Interrupt Mask (RXICMPERPIM):** Setting this bit masks the interrupt when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive ICMP Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive ICMP Error Packet Counter Interrupt Mask is enabled.
12	0h RW	**MMC Receive ICMP Good Packet Counter Interrupt Mask (RXICMPGPIM):** Setting this bit masks the interrupt when the rxicmp_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive ICMP Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive ICMP Good Packet Counter Interrupt Mask is enabled.
11	0h RW	**MMC Receive TCP Error Packet Counter Interrupt Mask (RXTCPERPIM):** Setting this bit masks the interrupt when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive TCP Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive TCP Error Packet Counter Interrupt Mask is enabled.
10	0h RW	**MMC Receive TCP Good Packet Counter Interrupt Mask (RXTCPGPIM):** Setting this bit masks the interrupt when the rxtcp_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive TCP Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive TCP Good Packet Counter Interrupt Mask is enabled.
9	0h RW	**MMC Receive UDP Error Packet Counter Interrupt Mask (RXUDPERPIM):** Setting this bit masks the interrupt when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive UDP Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive UDP Error Packet Counter Interrupt Mask is enabled.
8	0h RW	**MMC Receive UDP Good Packet Counter Interrupt Mask (RXUDPGPIM):** Setting this bit masks the interrupt when the rxudp_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive UDP Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive UDP Good Packet Counter Interrupt Mask is enabled.
7	0h RW	**MMC Receive IPV6 No Payload Packet Counter Interrupt Mask (RXIPV6NOPAYPIM):** Setting this bit masks the interrupt when the rxipv6_nopay_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 No Payload Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 No Payload Packet Counter Interrupt Mask is enabled.
6	0h RW	**MMC Receive IPV6 Header Error Packet Counter Interrupt Mask (RXIPV6HERPIM):** Setting this bit masks the interrupt when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 Header Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Header Error Packet Counter Interrupt Mask is enabled.
5	0h RW	**MMC Receive IPV6 Good Packet Counter Interrupt Mask (RXIPV6GPIM):** Setting this bit masks the interrupt when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Good Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Mask (RXIPV4UDSBLPIM):** Setting this bit masks the interrupt when the rxipv4_udsbl_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Mask is enabled.
3	0h RW	**MMC Receive IPV4 Fragmented Packet Counter Interrupt Mask (RXIPV4FRAGPIM):** Setting this bit masks the interrupt when the rxipv4_frag_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Fragmented Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Fragmented Packet Counter Interrupt Mask is enabled.
2	0h RW	**MMC Receive IPV4 No Payload Packet Counter Interrupt Mask (RXIPV4NOPAYPIM):** Setting this bit masks the interrupt when the rxipv4_nopay_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 No Payload Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 No Payload Packet Counter Interrupt Mask is enabled.
1	0h RW	**MMC Receive IPV4 Header Error Packet Counter Interrupt Mask (RXIPV4HERPIM):** Setting this bit masks the interrupt when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Header Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Header Error Packet Counter Interrupt Mask is enabled.
0	0h RW	**MMC Receive IPV4 Good Packet Counter Interrupt Mask (RXIPV4GPIM):** Setting this bit masks the interrupt when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Good Packet Counter Interrupt Mask is enabled.

10.2.249 MMC_IPC_RX_INTERRUPT — Offset 808h

This register maintains the interrupt that the receive IPC statistic counters generate.

The MMC Receive Checksum Offload Interrupt register maintains the interrupts generated when receive IPC statistic counters reach half their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32 bit counter and 0xFFFF for 16 bit counter). When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones.

The MMC Receive Checksum Offload Interrupt register is 32 bit wide. When the MMC IPC counter that caused the interrupt is read, its corresponding interrupt bit is cleared. The counter's least-significant byte lane (Bits[7:0]) must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 808h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RO	**MMC Receive ICMP Error Octet Counter Interrupt Status (RXICMPEROIS):** This bit is set when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive ICMP Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive ICMP Error Octet Counter Interrupt Status detected.
28	0h RO	**MMC Receive ICMP Good Octet Counter Interrupt Status (RXICMPGOIS):** This bit is set when the rxicmp_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive ICMP Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive ICMP Good Octet Counter Interrupt Status detected.
27	0h RO	**MMC Receive TCP Error Octet Counter Interrupt Status (RXTCPEROIS):** This bit is set when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive TCP Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive TCP Error Octet Counter Interrupt Status detected.
26	0h RO	**MMC Receive TCP Good Octet Counter Interrupt Status (RXTCPGOIS):** This bit is set when the rxtcp_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive TCP Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive TCP Good Octet Counter Interrupt Status detected.
25	0h RO	**MMC Receive UDP Error Octet Counter Interrupt Status (RXUDPEROIS):** This bit is set when the rxudp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive UDP Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive UDP Error Octet Counter Interrupt Status detected.
24	0h RO	**MMC Receive UDP Good Octet Counter Interrupt Status (RXUDPGOIS):** This bit is set when the rxudp_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive UDP Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive UDP Good Octet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**MMC Receive IPV6 No Payload Octet Counter Interrupt Status (RXIPV6NOPAYOIS):** This bit is set when the rxipv6_nopay_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 No Payload Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 No Payload Octet Counter Interrupt Status detected.
22	0h RO	**MMC Receive IPV6 Header Error Octet Counter Interrupt Status (RXIPV6HEROIS):** This bit is set when the rxipv6_hdrerr_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 Header Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 Header Error Octet Counter Interrupt Status detected.
21	0h RO	**MMC Receive IPV6 Good Octet Counter Interrupt Status (RXIPV6GOIS):** This bit is set when the rxipv6_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 Good Octet Counter Interrupt Status detected.
20	0h RO	**RXIPV4UDSBLOIS:** MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Status This bit is set when the rxipv4_udsbl_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Status detected.
19	0h RO	**MMC Receive IPV4 Fragmented Octet Counter Interrupt Status (RXIPV4FRAGOIS):** This bit is set when the rxipv4_frag_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Fragmented Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Fragmented Octet Counter Interrupt Status detected.
18	0h RO	**MMC Receive IPV4 No Payload Octet Counter Interrupt Status (RXIPV4NOPAYOIS):** This bit is set when the rxipv4_nopay_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 No Payload Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 No Payload Octet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**MMC Receive IPV4 Header Error Octet Counter Interrupt Status (RXIPV4HEROIS):** This bit is set when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Header Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Header Error Octet Counter Interrupt Status detected.
16	0h RO	**MMC Receive IPV4 Good Octet Counter Interrupt Status (RXIPV4GOIS):** This bit is set when the rxipv4_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Good Octet Counter Interrupt Status detected.
15:14	0h RO	**Reserved**
13	0h RO	**MMC Receive ICMP Error Packet Counter Interrupt Status (RXICMPERPIS):** This bit is set when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive ICMP Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive ICMP Error Packet Counter Interrupt Status detected.
12	0h RO	**MMC Receive ICMP Good Packet Counter Interrupt Status (RXICMPGPIS):** This bit is set when the rxicmp_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive ICMP Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive ICMP Good Packet Counter Interrupt Status detected.
11	0h RO	**MMC Receive TCP Error Packet Counter Interrupt Status (RXTCPERPIS):** This bit is set when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive TCP Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive TCP Error Packet Counter Interrupt Status detected.
10	0h RO	**MMC Receive TCP Good Packet Counter Interrupt Status (RXTCPGPIS):** This bit is set when the rxtcp_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive TCP Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive TCP Good Packet Counter Interrupt Status detected.
9	0h RO	**MMC Receive UDP Error Packet Counter Interrupt Status (RXUDPERPIS):** This bit is set when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive UDP Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive UDP Error Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**MC Receive UDP Good Packet Counter Interrupt Status (RXUDPGPIS):** This bit is set when the rxudp_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive UDP Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive UDP Good Packet Counter Interrupt Status detected.
7	0h RO	**MMC Receive IPV6 No Payload Packet Counter Interrupt Status (RXIPV6NOPAYPIS):** This bit is set when the rxipv6_nopay_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 No Payload Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 No Payload Packet Counter Interrupt Status detected.
6	0h RO	**MMC Receive IPV6 Header Error Packet Counter Interrupt Status (RXIPV6HERPIS):** This bit is set when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 Header Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 Header Error Packet Counter Interrupt Status detected.
5	0h RO	**MMC Receive IPV6 Good Packet Counter Interrupt Status (RXIPV6GPIS):** This bit is set when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 Good Packet Counter Interrupt Status detected.
4	0h RO	**MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Status (RXIPV4UDSBLPIS):** This bit is set when the rxipv4_udsbl_pkts counter reaches half of the maximum value or the maximum value. 0x0 (INACTIVE): MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Status detected.
3	0h RO	**MMC Receive IPV4 Fragmented Packet Counter Interrupt Status (RXIPV4FRAGPIS):** This bit is set when the rxipv4_frag_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Fragmented Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Fragmented Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**MMC Receive IPV4 No Payload Packet Counter Interrupt Status (RXIPV4NOPAYPIS):** This bit is set when the rxipv4_nopay_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 No Payload Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 No Payload Packet Counter Interrupt Status detected.
1	0h RO	**MMC Receive IPV4 Header Error Packet Counter Interrupt Status (RXIPV4HERPIS):** This bit is set when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Header Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Header Error Packet Counter Interrupt Status detected.
0	0h RO	**MMC Receive IPV4 Good Packet Counter Interrupt Status (RXIPV4GPIS):** This bit is set when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Good Packet Counter Interrupt Status detected.

10.2.250 RXIPV4_GOOD_PACKETS — Offset 810h

This register provides the number of good IPv4 datagrams received by GbE Controller with the TCP, UDP, or ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 810h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Good Packets (RXIPV4GDPKT):** This field indicates the number of good IPv4 datagrams received with the TCP, UDP, or ICMP payload.

10.2.251 RXIPV4_HEADER_ERROR_PACKETS — Offset 814h

RxIPv4 Header Error Packets

This register provides the number of IPv4 datagrams received by GbE Controller with header (checksum, length, or version mismatch) errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 814h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Header Error Packets (RXIPV4HDRERRPKT):** This field indicates the number of IPv4 datagrams received with header (checksum, length, or version mismatch) errors.

10.2.252 RXIPV4_NO_PAYLOAD_PACKETS — Offset 818h

This register provides the number of IPv4 datagram packets received by GbE Controller that did not have a TCP, UDP, or ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 818h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Payload Packets (RXIPV4NOPAYPKT):** This field indicates the number of IPv4 datagram packets received that did not have a TCP, UDP, or ICMP payload.

10.2.253 RXIPV4_FRAGMENTED_PACKETS — Offset 81Ch

This register provides the number of good IPv4 datagrams received by GbE Controller with fragmentation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 81Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Fragmented Packets (RXIPV4FRAGPKT):** This field indicates the number of good IPv4 datagrams received with fragmentation.

10.2.254 RXIPV4_UDP_CHECKSUM_DISABLED_PACKETS — Offset 820h

This register provides the number of good IPv4 datagrams received by GbE Controller that had a UDP payload with checksum disabled.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 820h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 UDP Checksum Disabled Packets (RXIPV4UDSBLPKT):** This field indicates the number of good IPv4 datagrams received that had a UDP payload with checksum disabled.

10.2.255 RXIPV6_GOOD_PACKETS — Offset 824h

This register provides the number of good IPv6 datagrams received by GbE Controller with the TCP, UDP, or ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 824h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Good Packets (RXIPV6GDPKT):** This field indicates the number of good IPv6 datagrams received with the TCP, UDP, or ICMP payload.

10.2.256 RXIPV6_HEADER_ERROR_PACKETS — Offset 828h

This register provides the number of IPv6 datagrams received by GbE Controller with header (length or version mismatch) errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 828h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Header Error Packets (RXIPV6HDRERRPKT):** This field indicates the number of IPv6 datagrams received with header (length or version mismatch) errors.

10.2.257 RXIPV6_NO_PAYLOAD_PACKETS — Offset 82Ch

This register provides the number of IPv6 datagram packets received by GbE Controller that did not have a TCP, UDP, or ICMP payload. This includes all IPv6 datagrams with fragmentation or security extension headers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 82Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Payload Packets (RXIPV6NOPAYPKT):** This field indicates the number of IPv6 datagram packets received that did not have a TCP, UDP, or ICMP payload. This includes all IPv6 datagrams with fragmentation or security extension headers.

10.2.258 RXUDP_GOOD_PACKETS — Offset 830h

This register provides the number of good IP datagrams received by GbE Controller with a good UDP payload. This counter is not updated when the RxIPv4_UDP_Checksum_Disabled_Packets counter is incremented.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 830h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxUDP Good Packets (RXUDPGDPKT):** This field indicates the number of good IP datagrams received with a good UDP payload. This counter is not updated when the RxIPv4_UDP_Checksum_Disabled_Packets counter is incremented.

10.2.259 RXUDP_ERROR_PACKETS — Offset 834h

This register provides the number of good IP datagrams received by GbE Controller whose UDP payload has a checksum error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 834h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxUDP Error Packets (RXUDPERRPKT):** This field indicates the number of good IP datagrams received whose UDP payload has a checksum error.

10.2.260 RXTCP_GOOD_PACKETS — Offset 838h

This register provides the number of good IP datagrams received by GbE Controller with a good TCP payload.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 838h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxTCP Good Packets (RXTCPGDPKT):** This field indicates the number of good IP datagrams received with a good TCP payload.

10.2.261 RXTCP_ERROR_PACKETS — Offset 83Ch

This register provides the number of good IP datagrams received by GbE Controller whose TCP payload has a checksum error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 83Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxTCP Error Packets (RXTCPERRPKT):** This field indicates the number of good IP datagrams received whose TCP payload has a checksum error.

10.2.262 RXICMP_GOOD_PACKETS — Offset 840h

This register provides the number of good IP datagrams received by GbE Controller with a good ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 840h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxICMP Good Packets (RXICMPGDPKT):** This field indicates the number of good IP datagrams received with a good ICMP payload.

10.2.263 RXICMP_ERROR_PACKETS — Offset 844h

This register provides the number of good IP datagrams received by GbE Controller whose ICMP payload has a checksum error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 844h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxICMP Error Packets (RXICMPERRPKT):** This field indicates the number of good IP datagrams received whose ICMP payload has a checksum error.

10.2.264 RXIPV4_GOOD_OCTETS — Offset 850h

This register provides the number of bytes received by GbE Controller in good IPv4 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 850h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Good Octets (RXIPV4GDOCT):** This field indicates the number of bytes received in good IPv4 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

10.2.265 RXIPV4_HEADER_ERROR_OCTETS — Offset 854h

This register provides the number of bytes received by GbE Controller in IPv4 datagrams with header errors (checksum, length, version mismatch). The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 854h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Header Error Octets (RXIPV4HDRERROCT):** This field indicates the number of bytes received in IPv4 datagrams with header errors (checksum, length, version mismatch). The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

10.2.266 RXIPV4_NO_PAYLOAD_OCTETS — Offset 858h

This register provides the number of bytes received by GbE Controller in IPv4 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 858h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Payload Octets (RXIPV4NOPAYOCT):** This field indicates the number of bytes received in IPv4 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

10.2.267 RXIPV4_FRAGMENTED_OCTETS — Offset 85Ch

This register provides the number of bytes received by GbE Controller in fragmented IPv4 datagrams. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 85Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Fragmented Octets (RXIPV4FRAGOCT):** This field indicates the number of bytes received in fragmented IPv4 datagrams. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

10.2.268 RXIPV4_UDP_CHECKSUM_DISABLE_OCTETS — Offset 860h

This register provides the number of bytes received by GbE Controller in a UDP segment that had the UDP checksum disabled. This counter does not count IP Header bytes. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 860h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 UDP Checksum Disable Octets (RXIPV4UDSBLOCT):** This field indicates the number of bytes received in a UDP segment that had the UDP checksum disabled. This counter does not count IP Header bytes. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

10.2.269 RXIPV6_GOOD_OCTETS — Offset 864h

This register provides the number of bytes received by GbE Controller in good IPv6 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 864h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Good Octets (RXIPV6GDOCT):** This field indicates the number of bytes received in good IPv6 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

10.2.270 RXIPV6_HEADER_ERROR_OCTETS — Offset 868h

This register provides the number of bytes received by GbE Controller in IPv6 datagrams with header errors (length, version mismatch). The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 868h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Header Error Octets (RXIPV6HDRERROCT):** This field indicates the number of bytes received in IPv6 datagrams with header errors (length, version mismatch). The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

10.2.271 RXIPV6_NO_PAYLOAD_OCTETS — Offset 86Ch

This register provides the number of bytes received by GbE Controller in IPv6 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 86Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Payload Octets (RXIPV6NOPAYOCT):** This field indicates the number of bytes received in IPv6 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

10.2.272 RXUDP_GOOD_OCTETS — Offset 870h

This register provides the number of bytes received by GbE Controller in a good UDP segment. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 870h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxUDP Good Octets (RXUDPGDOCT):** This field indicates the number of bytes received in a good UDP segment. This counter does not count IP header bytes.

10.2.273 RXUDP_ERROR_OCTETS — Offset 874h

This register provides the number of bytes received by GbE Controller in a UDP segment that had checksum errors. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 874h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxUDP Error Octets (RXUDPERROCT):** This field indicates the number of bytes received in a UDP segment that had checksum errors. This counter does not count IP header bytes.

10.2.274 RXTCP_GOOD_OCTETS — Offset 878h

This register provides the number of bytes received by GbE Controller in a good TCP segment. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 878h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxTCP Good Octets (RXTCPGDOCT):** This field indicates the number of bytes received in a good TCP segment. This counter does not count IP header bytes.

10.2.275 RXTCP_ERROR_OCTETS — Offset 87Ch

This register provides the number of bytes received by GbE Controller in a TCP segment that had checksum errors. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 87Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxTCP Error Octets (RXTCPERROCT):** This field indicates the number of bytes received in a TCP segment that had checksum errors. This counter does not count IP header bytes.

10.2.276 RXICMP_GOOD_OCTETS — Offset 880h

This register provides the number of bytes received by GbE Controller in a good ICMP segment. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 880h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxICMP Good Octets (RXICMPGDOCT):** This field indicates the number of bytes received in a good ICMP segment. This counter does not count IP header bytes.

10.2.277 RXICMP_ERROR_OCTETS — Offset 884h

This register provides the number of bytes received by GbE Controller in a ICMP segment that had checksum errors. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 884h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxICMP Error Octets (RXICMPERROCT):** This field indicates the number of bytes received in a ICMP segment that had checksum errors. This counter does not count IP header bytes.

10.2.278 MMC_FPE_TX_INTERRUPT — Offset 8A0h

This register maintains the interrupts generated from all FPE related Transmit statistics counters. The MMC FPE Transmit Interrupt register maintains the interrupts generated when transmit statistic counters reach half their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32-bit counter and 0xFFFF for 16-bit counter). When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones. The MMC FPE Transmit Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RO	**MMC Tx Hold Request Counter Interrupt Status (HRCIS):** This bit is set when the Tx_Hold_Req_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration. 0x0 (INACTIVE): MMC Tx Hold Request Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Tx Hold Request Counter Interrupt Status detected.
0	0h RO	**MMC Tx FPE Fragment Counter Interrupt status (FCIS):** This bit is set when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Tx FPE Fragment Counter Interrupt status not detected. 0x1 (ACTIVE): MMC Tx FPE Fragment Counter Interrupt status detected.

10.2.279 MMC_FPE_TX_INTERRUPT_MASK — Offset 8A4h

This register maintains the masks for interrupts generated from all FPE related Transmit statistics counters. The MMC Receive Interrupt Mask register maintains the masks for the interrupts generated when FPE related receive statistic counters reach half of their maximum value or the maximum values. This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**MMC Transmit Hold Request Counter Interrupt Mask (HRCIM):** Setting this bit masks the interrupt when the Tx_Hold_Req_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration. 0x0 (DISABLE): MMC Transmit Hold Request Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Hold Request Counter Interrupt Mask is enabled.
0	0h RW	**MMC Transmit Fragment Counter Interrupt Mask (FCIM):** Setting this bit masks the interrupt when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (DISABLE): MMC Transmit Fragment Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Fragment Counter Interrupt Mask is enabled.

10.2.280 MMC_TX_FPE_FRAGMENT_CNTR — Offset 8A8h

This register provides the number of additional mPackets transmitted due to preemption.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx FPE Fragment counter (TXFFC):** This field indicates the number of additional mPackets that has been transmitted due to preemption Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

10.2.281 MMC_TX_HOLD_REQ_CNTR — Offset 8ACh

This register provides the count of number of times a hold request is given to MAC

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Hold Request Counter (TXHRC):** This field indicates count of number of a hold request is given to MAC. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration.

10.2.282 MMC_FPE_RX_INTERRUPT — Offset 8C0h

This register maintains the interrupts generated from all FPE related Receive statistics counters. The MMC FPE Receive Interrupt register maintains the interrupts generated when transmit statistic counters reach half their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32-bit counter and 0xFFFF for 16-bit counter). When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones. The MMC FPE Receive Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RO	**MMC Rx FPE Fragment Counter Interrupt Status (FCIS):** This bit is set when the Rx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Rx FPE Fragment Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Rx FPE Fragment Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**MMC Rx Packet Assembly OK Counter Interrupt Status (PAOCIS):** This bit is set when the Rx_Packet_Assemble_Ok_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Rx Packet Assembly OK Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Rx Packet Assembly OK Counter Interrupt Status detected.
1	0h RO	**MMC Rx Packet SMD Error Counter Interrupt Status (PSECIS):** This bit is set when the Rx_Packet_SMD_Err_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Rx Packet SMD Error Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Rx Packet SMD Error Counter Interrupt Status detected.
0	0h RO	**MMC Rx Packet Assembly Error Counter Interrupt Status (PAECIS):** This bit is set when the Rx_Packet_Assemble_Err_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Rx Packet Assembly Error Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Rx Packet Assembly Error Counter Interrupt Status detected.

10.2.283 MMC_FPE_RX_INTERRUPT_MASK — Offset 8C4h

This register maintains the masks for interrupts generated from all FPE related Receive statistics counters. The MMC Receive Interrupt Mask register maintains the masks for the interrupts generated when FPE related receive statistic counters reach half of their maximum value or the maximum values. This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**MMC Rx FPE Fragment Counter Interrupt Mask (FCIM):** Setting this bit masks the interrupt when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (DISABLE): MMC Rx FPE Fragment Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Rx FPE Fragment Counter Interrupt Mask is enabled.
2	0h RW	**MMC Rx Packet Assembly OK Counter Interrupt Mask (PAOCIM):** Setting this bit masks the interrupt when the Rx_Packet_Assemble_Ok_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (DISABLE): MMC Rx Packet Assembly OK Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Rx Packet Assembly OK Counter Interrupt Mask is enabled.
1	0h RW	**MMC Rx Packet SMD Error Counter Interrupt Mask (PSECIM):** Setting this bit masks the interrupt when the R Rx_Packet_SMD_Err_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (DISABLE): MMC Rx Packet SMD Error Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Rx Packet SMD Error Counter Interrupt Mask is enabled.
0	0h RW	**MMC Rx Packet Assembly Error Counter Interrupt Mask (PAECIM):** Setting this bit masks the interrupt when the R Rx_Packet_Assemble_Err_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (DISABLE): MMC Rx Packet Assembly Error Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Rx Packet Assembly Error Counter Interrupt Mask is enabled.

10.2.284 MMC_RX_PACKET_ASSEMBLY_ERR_CNTR — Offset 8C8h

This register provides the number of MAC frames with reassembly errors on the Receiver, due to mismatch in the Fragment Count value.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Packet Assembly Error Counter (PAEC):** This field indicates the number of MAC frames with reassembly errors on the Receiver, due to mismatch in the Fragment Count value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

10.2.285 MMC_RX_PACKET_SMD_ERR_CNTR — Offset 8CCh

This register provides the number of received MAC frames rejected due to unknown SMD value and MAC frame fragments rejected due to arriving with an SMD-C when there was no preceding preempted frame.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Packet SMD Error Counter (PSEC):** This field indicates the number of MAC frames rejected due to unknown SMD value and MAC frame fragments rejected due to arriving with an SMD-C when there was no preceding preempted frame. Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

10.2.286 MMC_RX_PACKET_ASSEMBLY_OK_CNTR — Offset 8D0h

This register provides the number of MAC frames that were successfully reassembled and delivered to MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Packet Assembly OK Counter (PAOC):** This field indicates the number of MAC frames that were successfully reassembled and delivered to MAC. Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

10.2.287 MMC_RX_FPE_FRAGMENT_CNTR — Offset 8D4h

This register provides the number of additional mPackets received due to preemption.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx FPE Fragment Counter (FFC):** This field indicates the number of additional mPackets received due to preemption Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

10.2.288 MAC_L3_L4_CONTROL0 — Offset 900h

The Layer 3 and Layer 4 Control register controls the operations of filter 0 of Layer 3 and Layer 4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 900h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**DMA Channel Select Enable (DMCHEN0):** When set, this bit enables the selection of the DMA channel number for the packet that is passed by this L3_L4 filter. The DMA channel is indicated by the DMCHN bits. When this bit is reset, the DMA channel is not decided by this filter. 0x0 (DISABLE): DMA Channel Select is disabled. 0x1 (ENABLE): DMA Channel Select is enabled.
27	0h RO	**Reserved**
26:24	0h RW	**DMA Channel Number (DMCHN0):** When DMCHEN is set high, this field selects the DMA Channel number to which the packet passed by this filter is routed. The width of this field depends on the number of the DMA channels present in your configuration.
23:22	0h RO	**Reserved**
21	0h RW	**Layer 4 Destination Port Inverse Match Enable (L4DPIM0):** When this bit is set, the Layer 4 Destination Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Destination Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4DPM0 bit is set high. 0x0 (DISABLE): Layer 4 Destination Port Inverse Match is disabled. 0x1 (ENABLE): Layer 4 Destination Port Inverse Match is enabled.
20	0h RW	**Layer 4 Destination Port Match Enable (L4DPM0):** When this bit is set, the Layer 4 Destination Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Destination Port number field for matching. 0x0 (DISABLE): Layer 4 Destination Port Match is disabled. 0x1 (ENABLE): Layer 4 Destination Port Match is enabled.
19	0h RW	**Layer 4 Source Port Inverse Match Enable (L4SPIM0):** When this bit is set, the Layer 4 Source Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Source Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4SPM0 bit is set high. 0x0 (DISABLE): Layer 4 Source Port Inverse Match is disabled. 0x1 (ENABLE): Layer 4 Source Port Inverse Match is enabled.
18	0h RW	**Layer 4 Source Port Match Enable (L4SPM0):** When this bit is set, the Layer 4 Source Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Source Port number field for matching. 0x0 (DISABLE): Layer 4 Source Port Match is disabled. 0x1 (ENABLE): Layer 4 Source Port Match is enabled.
17	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Layer 4 Protocol Enable (L4PEN0):** When this bit is set, the Source and Destination Port number fields of UDP packets are used for matching. When this bit is reset, the Source and Destination Port number fields of TCP packets are used for matching. The Layer 4 matching is done only when the L4SPM0 or L4DPM0 bit is set. 0x0 (DISABLE): Layer 4 Protocol is disabled. 0x1 (ENABLE): Layer 4 Protocol is enabled.
15:11	00h RW	**L3HDBM0:** Layer 3 IP DA Higher Bits Match IPv4 Packets: This field contains the number of higher bits of IP Destination Address that are matched in the IPv4 packets. The following list describes the values of this field: - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. IPv6 Packets: Bits[12:11] of this field correspond to Bits[6:5] of L3HSBM0 which indicate the number of lower bits of IP Source or Destination Address that are masked in the IPv6 packets. The following list describes the concatenated values of the L3HDBM0[1:0] and L3HSBM0 bits: - 0: No bits are masked. - 1: LSb[0] is masked. - 2: Two LSbs [1:0] are masked - .. - 127: All bits except MSb are masked. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set.
10:6	00h RW	**L3HSBM0:** Layer 3 IP SA Higher Bits Match IPv4 Packets: This field contains the number of lower bits of IP Source Address that are masked for matching in the IPv4 packets. The following list describes the values of this field: - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. IPv6 Packets: This field contains Bits[4:0] of L3HSBM0. These bits indicate the number of higher bits of IP Source or Destination Address matched in the IPv6 packets. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set high.
5	0h RW	**Layer 3 IP DA Inverse Match Enable (L3DAIM0):** When this bit is set, the Layer 3 IP Destination Address field is enabled for inverse matching. When this bit is reset, the Layer 3 IP Destination Address field is enabled for perfect matching. This bit is valid and applicable only when the L3DAM0 bit is set high. 0x0 (DISABLE): Layer 3 IP DA Inverse Match is disabled. 0x1 (ENABLE): Layer 3 IP DA Inverse Match is enabled.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Layer 3 IP DA Match Enable (L3DAM0):** When this bit is set, the Layer 3 IP Destination Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Destination Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3SAM0 bit because either IPv6 DA or SA can be checked for filtering. 0x0 (DISABLE): Layer 3 IP DA Match is disabled. 0x1 (ENABLE): Layer 3 IP DA Match is enabled.
3	0h RW	**Layer 3 IP SA Inverse Match Enable (L3SAIM0):** When this bit is set, the Layer 3 IP Source Address field is enabled for inverse matching. When this bit reset, the Layer 3 IP Source Address field is enabled for perfect matching. This bit is valid and applicable only when the L3SAM0 bit is set. 0x0 (DISABLE): Layer 3 IP SA Inverse Match is disabled. 0x1 (ENABLE): Layer 3 IP SA Inverse Match is enabled.
2	0h RW	**Layer 3 IP SA Match Enable (L3SAM0):** When this bit is set, the Layer 3 IP Source Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Source Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3DAM0 bit because either IPv6 SA or DA can be checked for filtering. 0x0 (DISABLE): Layer 3 IP SA Match is disabled. 0x1 (ENABLE): Layer 3 IP SA Match is enabled.
1	0h RO	**Reserved**
0	0h RW	**Layer 3 Protocol Enable (L3PEN0):** When this bit is set, the Layer 3 IP Source or Destination Address matching is enabled for IPv6 packets. When this bit is reset, the Layer 3 IP Source or Destination Address matching is enabled for IPv4 packets. The Layer 3 matching is done only when the L3SAM0 or L3DAM0 bit is set. 0x0 (DISABLE): Layer 3 Protocol is disabled. 0x1 (ENABLE): Layer 3 Protocol is enabled.

10.2.289 MAC_LAYER4_ADDRESS0 — Offset 904h

The MAC_Layer4_Address(#i), MAC_L3_L4_Control(#i), MAC_Layer3_Addr0_Reg(#i), MAC_Layer3_Addr1_Reg(#i), MAC_Layer3_Addr2_Reg(#i) and MAC_Layer3_Addr3_Reg(#i) registers are reserved (RO with default value) if Enable Layer 3 and Layer 4 Packet Filter option is not selected while configuring the core.

You can configure the Layer 3 and Layer 4 Address Registers to be double-synchronized by selecting the Synchronize Layer 3 and Layer 4 Address Registers to Rx Clock Domain option while configuring the core. When you select this option, the synchronization is triggered only when Bits[31:24] of the Layer 3 and Layer 4 Address Registers are written. For proper synchronization updates, you should perform consecutive writes to same Layer 3 and Layer 4 Address Registers after at least four clock cycles delay of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 904h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Layer 4 Destination Port Number Field (L4DP0):** When the L4PEN0 bit is reset and the L4DPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Destination Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4DPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Destination Port Number field in the IPv4 or IPv6 packets.
15:0	0000h RW	**Layer 4 Source Port Number Field (L4SP0):** When the L4PEN0 bit is reset and the L4SPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Source Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4SPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Source Port Number field in the IPv4 or IPv6 packets.

10.2.290 MAC_LAYER3_ADDR0_REG0 — Offset 910h

For IPv4 packets, the Layer 3 Address 0 Register 0 register contains the 32-bit IP Source Address field. For IPv6 packets, it contains Bits[31:0] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 910h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 0 Field (L3A00):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Source Address field in the IPv4 packets.

10.2.291 MAC_LAYER3_ADDR1_REG0 — Offset 914h

For IPv4 packets, the Layer 3 Address 1 Register 0 register contains the 32-bit IP Destination Address field. For IPv6 packets, it contains Bits[63:32] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 914h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 1 Field (L3A10):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Destination Address field in the IPv4 packets.

10.2.292 MAC_LAYER3_ADDR2_REG0 — Offset 918h

The Layer 3 Address 2 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[95:64] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 918h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 2 Field (L3A20):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

10.2.293 MAC_LAYER3_ADDR3_REG0 — Offset 91Ch

The Layer 3 Address 3 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[127:96] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 91Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 3 Field (L3A30):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

10.2.294 MAC_L3_L4_CONTROL1 — Offset 930h

The Layer 3 and Layer 4 Control register controls the operations of filter 0 of Layer 3 and Layer 4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 930h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**DMA Channel Select Enable (DMCHEN1):** When set, this bit enables the selection of the DMA channel number for the packet that is passed by this L3_L4 filter. The DMA channel is indicated by the DMCHN bits. When this bit is reset, the DMA channel is not decided by this filter. 0x0 (DISABLE): DMA Channel Select is disabled. 0x1 (ENABLE): DMA Channel Select is enabled.
27	0h RO	**Reserved**
26:24	0h RW	**DMA Channel Number (DMCHN1):** When DMCHEN is set high, this field selects the DMA Channel number to which the packet passed by this filter is routed. The width of this field depends on the number of the DMA channels present in your configuration.
23:22	0h RO	**Reserved**
21	0h RW	**Layer 4 Destination Port Inverse Match Enable (L4DPIM1):** When this bit is set, the Layer 4 Destination Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Destination Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4DPM0 bit is set high. 0x0 (DISABLE): Layer 4 Destination Port Inverse Match is disabled. 0x1 (ENABLE): Layer 4 Destination Port Inverse Match is enabled.
20	0h RW	**Layer 4 Destination Port Match Enable (L4DPM1):** When this bit is set, the Layer 4 Destination Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Destination Port number field for matching. 0x0 (DISABLE): Layer 4 Destination Port Match is disabled. 0x1 (ENABLE): Layer 4 Destination Port Match is enabled.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Layer 4 Source Port Inverse Match Enable (L4SPIM1):** When this bit is set, the Layer 4 Source Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Source Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4SPM0 bit is set high. 0x0 (DISABLE): Layer 4 Source Port Inverse Match is disabled. 0x1 (ENABLE): Layer 4 Source Port Inverse Match is enabled.
18	0h RW	**Layer 4 Source Port Match Enable (L4SPM1):** When this bit is set, the Layer 4 Source Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Source Port number field for matching. 0x0 (DISABLE): Layer 4 Source Port Match is disabled. 0x1 (ENABLE): Layer 4 Source Port Match is enabled.
17	0h RO	**Reserved**
16	0h RW	**Layer 4 Protocol Enable (L4PEN1):** When this bit is set, the Source and Destination Port number fields of UDP packets are used for matching. When this bit is reset, the Source and Destination Port number fields of TCP packets are used for matching. The Layer 4 matching is done only when the L4SPM0 or L4DPM0 bit is set. 0x0 (DISABLE): Layer 4 Protocol is disabled. 0x1 (ENABLE): Layer 4 Protocol is enabled.
15:11	00h RW	**L3HDBM1:** Layer 3 IP DA Higher Bits Match IPv4 Packets: This field contains the number of higher bits of IP Destination Address that are matched in the IPv4 packets. The following list describes the values of this field: - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. IPv6 Packets: Bits[12:11] of this field correspond to Bits[6:5] of L3HSBM0 which indicate the number of lower bits of IP Source or Destination Address that are masked in the IPv6 packets. The following list describes the concatenated values of the L3HDBM0[1:0] and L3HSBM0 bits: - 0: No bits are masked. - 1: LSb[0] is masked. - 2: Two LSbs [1:0] are masked - .. - 127: All bits except MSb are masked. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set.

Bit Range	Default & Access	Field Name (ID): Description
10:6	00h RW	**L3HSBM1:** Layer 3 IP SA Higher Bits Match IPv4 Packets: This field contains the number of lower bits of IP Source Address that are masked for matching in the IPv4 packets. The following list describes the values of this field: - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. IPv6 Packets: This field contains Bits[4:0] of L3HSBM0. These bits indicate the number of higher bits of IP Source or Destination Address matched in the IPv6 packets. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set high.
5	0h RW	**Layer 3 IP DA Inverse Match Enable (L3DAIM1):** When this bit is set, the Layer 3 IP Destination Address field is enabled for inverse matching. When this bit is reset, the Layer 3 IP Destination Address field is enabled for perfect matching. This bit is valid and applicable only when the L3DAM0 bit is set high. 0x0 (DISABLE): Layer 3 IP DA Inverse Match is disabled. 0x1 (ENABLE): Layer 3 IP DA Inverse Match is enabled.
4	0h RW	**Layer 3 IP DA Match Enable (L3DAM1):** When this bit is set, the Layer 3 IP Destination Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Destination Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3SAM0 bit because either IPv6 DA or SA can be checked for filtering. 0x0 (DISABLE): Layer 3 IP DA Match is disabled. 0x1 (ENABLE): Layer 3 IP DA Match is enabled.
3	0h RW	**Layer 3 IP SA Inverse Match Enable (L3SAIM1):** When this bit is set, the Layer 3 IP Source Address field is enabled for inverse matching. When this bit reset, the Layer 3 IP Source Address field is enabled for perfect matching. This bit is valid and applicable only when the L3SAM0 bit is set. 0x0 (DISABLE): Layer 3 IP SA Inverse Match is disabled. 0x1 (ENABLE): Layer 3 IP SA Inverse Match is enabled.
2	0h RW	**Layer 3 IP SA Match Enable (L3SAM1):** When this bit is set, the Layer 3 IP Source Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Source Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3DAM0 bit because either IPv6 SA or DA can be checked for filtering. 0x0 (DISABLE): Layer 3 IP SA Match is disabled. 0x1 (ENABLE): Layer 3 IP SA Match is enabled.
1	0h RO	**Reserved**
0	0h RW	**Layer 3 Protocol Enable (L3PEN1):** When this bit is set, the Layer 3 IP Source or Destination Address matching is enabled for IPv6 packets. When this bit is reset, the Layer 3 IP Source or Destination Address matching is enabled for IPv4 packets. The Layer 3 matching is done only when the L3SAM0 or L3DAM0 bit is set. 0x0 (DISABLE): Layer 3 Protocol is disabled. 0x1 (ENABLE): Layer 3 Protocol is enabled.

10.2.295 MAC_LAYER4_ADDRESS1 — Offset 934h

The MAC_Layer4_Address(#i), MAC_L3_L4_Control(#i), MAC_Layer3_Addr0_Reg(#i), MAC_Layer3_Addr1_Reg(#i), MAC_Layer3_Addr2_Reg(#i) and MAC_Layer3_Addr3_Reg(#i) registers are reserved (RO with default value) if Enable Layer 3 and Layer 4 Packet Filter option is not selected while configuring the core.

You can configure the Layer 3 and Layer 4 Address Registers to be double-synchronized by selecting the Synchronize Layer 3 and Layer 4 Address Registers to Rx Clock Domain option while configuring the core. When you select this option, the synchronization is triggered only when Bits[31:24] of the Layer 3 and Layer 4 Address Registers are written. For proper synchronization updates, you should perform consecutive writes to same Layer 3 and Layer 4 Address Registers after at least four clock cycles delay of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 934h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Layer 4 Destination Port Number Field (L4DP1):** When the L4PEN0 bit is reset and the L4DPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Destination Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4DPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Destination Port Number field in the IPv4 or IPv6 packets.
15:0	0000h RW	**Layer 4 Source Port Number Field (L4SP1):** When the L4PEN0 bit is reset and the L4SPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Source Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4SPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Source Port Number field in the IPv4 or IPv6 packets.

10.2.296 MAC_LAYER3_ADDR0_REG1 — Offset 940h

For IPv4 packets, the Layer 3 Address 0 Register 0 register contains the 32-bit IP Source Address field. For IPv6 packets, it contains Bits[31:0] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 940h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 0 Field (L3A01):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Source Address field in the IPv4 packets.

10.2.297 MAC_LAYER3_ADDR1_REG1 — Offset 944h

For IPv4 packets, the Layer 3 Address 1 Register 0 register contains the 32-bit IP Destination Address field. For IPv6 packets, it contains Bits[63:32] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 944h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 1 Field (L3A11):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Destination Address field in the IPv4 packets.

10.2.298 MAC_LAYER3_ADDR2_REG1 — Offset 948h

The Layer 3 Address 2 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[95:64] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 948h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 2 Field (L3A21):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

10.2.299 MAC_LAYER3_ADDR3_REG1 — Offset 94Ch

The Layer 3 Address 3 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[127:96] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 94Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 3 Field (L3A31):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

10.2.300 MAC_TIMESTAMP_CONTROL — Offset B00h

This register controls the operation of the System Time generator and processing of PTP packets for timestamping in the Receiver.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B00h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**AV 802.1AS Mode Enable (AV8021ASMEN):** When this bit is set, the MAC processes only untagged PTP over Ethernet packets for providing PTP status and capturing timestamp snapshots, that is, IEEE 802.1AS mode of operation. When PTP offload feature is enabled, for the purpose of PTP offload, the transport specific field in the PTP header is generated and checked based on the value of this bit. 0x0 (DISABLE): AV 802.1AS Mode is disabled. 0x1 (ENABLE): AV 802.1AS Mode is enabled.
27:25	0h RO	**Reserved**
24	0h RW	**Transmit Timestamp Status Mode (TXTSSTSM):** When this bit is set, the MAC overwrites the earlier transmit timestamp status even if it is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register. When this bit is reset, the MAC ignores the timestamp status of current packet if the timestamp status of previous packet is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register. 0x0 (DISABLE): Transmit Timestamp Status Mode is disabled. 0x1 (ENABLE): Transmit Timestamp Status Mode is enabled.
23:21	0h RO	**Reserved**
20	0h RW	**External System Time Input (ESTI):** When this bit is set, the MAC uses the external 64-bit reference System Time input for the following: - To take the timestamp provided as status - To insert the timestamp in transmit PTP packets when One-step Timestamp or Timestamp Offload feature is enabled. When this bit is reset, the MAC uses the internal reference System Time. 0x0 (DISABLE): External System Time Input is disabled. 0x1 (ENABLE): External System Time Input is enabled.
19	0h RW	**Enable checksum correction during OST for PTP over UDP/IPv4 packets (CSC):** When this bit is set, the last two bytes of PTP message sent over UDP/IPv4 is updated to keep the UDP checksum correct, for changes made to origin timestamp and/or correction field as part of one step timestamp operation. The application shall form the packet with these two dummy bytes. When reset, no updates are done to keep the UDP checksum correct. The application shall form the packet with UDP checksum set to 0. 0x0 (DISABLE): checksum correction during OST for PTP over UDP/IPv4 packets is disabled. 0x1 (ENABLE): checksum correction during OST for PTP over UDP/IPv4 packets is enabled.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**Enable MAC Address for PTP Packet Filtering (TSENMACADDR):** When this bit is set, the DA MAC address (that matches any MAC Address register) is used to filter the PTP packets when PTP is directly sent over Ethernet. When this bit is set, received PTP packets with DA containing a special multicast or unicast address that matches the one programmed in MAC address registers are considered for processing as indicated below, when PTP is directly sent over Ethernet. For normal time stamping operation, MAC address registers 0 to 31 is considered for unicast destination address matching. For PTP offload, only MAC address register 0 is considered for unicast destination address matching. 0x0 (DISABLE): MAC Address for PTP Packet Filtering is disabled. 0x1 (ENABLE): MAC Address for PTP Packet Filtering is enabled.
17:16	0h RW	**Select PTP packets for Taking Snapshots (SNAPTYPSEL):** These bits, along with Bits 15 and 14, decide the set of PTP packet types for which snapshot needs to be taken. The encoding is given in Timestamp Snapshot Dependency on Register Bits Table.
15	0h RW	**Enable Snapshot for Messages Relevant to Master (TSMSTRENA):** When this bit is set, the snapshot is taken only for the messages that are relevant to the master node. Otherwise, the snapshot is taken for the messages relevant to the slave node. 0x0 (DISABLE): Snapshot for Messages Relevant to Master is disabled. 0x1 (ENABLE): Snapshot for Messages Relevant to Master is enabled.
14	0h RW	**Enable Timestamp Snapshot for Event Messages (TSEVNTENA):** When this bit is set, the timestamp snapshot is taken only for event messages (SYNC, Delay_Req, Pdelay_Req, or Pdelay_Resp). When this bit is reset, the snapshot is taken for all messages except Announce, Management, and Signaling. For more information about the timestamp snapshots, see Timestamp Snapshot Dependency on Register Bits Table. 0x0 (DISABLE): Timestamp Snapshot for Event Messages is disabled. 0x1 (ENABLE): Timestamp Snapshot for Event Messages is enabled.
13	1h RW	**Enable Processing of PTP Packets Sent over IPv4-UDP (TSIPV4ENA):** When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv4-UDP packets. When this bit is reset, the MAC ignores the PTP transported over IPv4-UDP packets. This bit is set by default. 0x0 (DISABLE): Processing of PTP Packets Sent over IPv4-UDP is disabled. 0x1 (ENABLE): Processing of PTP Packets Sent over IPv4-UDP is enabled.
12	0h RW	**Enable Processing of PTP Packets Sent over IPv6-UDP (TSIPV6ENA):** When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv6-UDP packets. When this bit is clear, the MAC ignores the PTP transported over IPv6-UDP packets. 0x0 (DISABLE): Processing of PTP Packets Sent over IPv6-UDP is disabled. 0x1 (ENABLE): Processing of PTP Packets Sent over IPv6-UDP is enabled.
11	0h RW	**Enable Processing of PTP over Ethernet Packets (TSIPENA):** When this bit is set, the MAC receiver processes the PTP packets encapsulated directly in the Ethernet packets. When this bit is reset, the MAC ignores the PTP over Ethernet packets. 0x0 (DISABLE): Processing of PTP over Ethernet Packets is disabled. 0x1 (ENABLE): Processing of PTP over Ethernet Packets is enabled.
10	0h RW	**Enable PTP Packet Processing for Version 2 Format (TSVER2ENA):** When this bit is set, the IEEE 1588 version 2 format is used to process the PTP packets. When this bit is reset, the IEEE 1588 version 1 format is used to process the PTP packets. The IEEE 1588 formats are described in 'PTP Processing and Control'. 0x0 (DISABLE): PTP Packet Processing for Version 2 Format is disabled. 0x1 (ENABLE): PTP Packet Processing for Version 2 Format is enabled.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Timestamp Digital or Binary Rollover Control (TSCTRLSSR):** When this bit is set, the Timestamp Low register rolls over after 0x3B9A_C9FF value (that is, 1 nanosecond accuracy) and increments the timestamp (High) seconds. When this bit is reset, the rollover value of sub-second register is 0x7FFF_FFFF. The sub-second increment must be programmed correctly depending on the PTP reference clock frequency and the value of this bit. 0x0 (DISABLE): Timestamp Digital or Binary Rollover Control is disabled. 0x1 (ENABLE): Timestamp Digital or Binary Rollover Control is enabled.
8	0h RW	**Enable Timestamp for All Packets (TSENALL):** When this bit is set, the timestamp snapshot is enabled for all packets received by the MAC. 0x0 (DISABLE): Timestamp for All Packets disabled. 0x1 (ENABLE): Timestamp for All Packets enabled.
7	0h RO	**Reserved**
6	0h RW	**Presentation Time Generation Enable (PTGE):** When this bit is set the Presentation Time generation is enabled. 0x0 (DISABLE): Presentation Time Generation is disabled. 0x1 (ENABLE): Presentation Time Generation is enabled.
5	0h RW	**Update Addend Register (TSADDREG):** When this bit is set, the content of the Timestamp Addend register is updated in the PTP block for fine correction. This bit is cleared when the update is complete. This bit should be zero before it is set. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Addend Register is not updated. 0x1 (ENABLE): Addend Register is updated.
4	0h RO	**Reserved**
3	0h RW	**Update Timestamp (TSUPDT):** When this bit is set, the system time is updated (added or subtracted) with the value specified in MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before updating it. This bit is reset when the update is complete in hardware. The Timestamp Higher Word register (if enabled during core configuration) is not updated. When Media Clock Generation and Recovery is DWC_EQOS_FLEXI_PPS_OUT_EN=1 enabled MAC_Presn_Time_Updt should also be updated before setting this field. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Timestamp is not updated. 0x1 (ENABLE): Timestamp is updated.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Initialize Timestamp (TSINIT):** When this bit is set, the system time is initialized (overwritten) with the value specified in the MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before it is updated. This bit is reset when the initialization is complete. The Timestamp Higher Word register (if enabled during core configuration) can only be initialized. When Media Clock Generation and Recovery is DWC_EQOS_FLEXI_PPS_OUT_EN=1 enabled MAC_Presn_Time_Updt should also be updated before setting this field. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Timestamp is not initialized. 0x1 (ENABLE): Timestamp is initialized.
1	0h RW	**Fine or Coarse Timestamp Update (TSCFUPDT):** When this bit is set, the Fine method is used to update system timestamp. When this bit is reset, Coarse method is used to update the system timestamp. 0x0 (COARSE): Coarse method is used to update system timestamp. 0x1 (FINE): Fine method is used to update system timestamp.
0	0h RW	**Enable Timestamp (TSENA):** When this bit is set, the timestamp is added for Transmit and Receive packets. When disabled, timestamp is not added for transmit and receive packets and the Timestamp Generator is also suspended. You need to initialize the Timestamp (system time) after enabling this mode. On the Receive side, the MAC processes the 1588 packets only if this bit is set. 0x0 (DISABLE): Timestamp is disabled. 0x1 (ENABLE): Timestamp is enabled.

10.2.301 MAC_SUB_SECOND_INCREMENT — Offset B04h

This register specifies the value to be added to the internal system time register every cycle of clk_ptp_ref_i clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B04h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW	**Sub-second Increment Value (SSINC):** The value programmed in this field is accumulated every clock cycle (of clk_ptp_i) with the contents of the sub-second register. For example, when the PTP clock is 50 MHz (period is 20 ns), you should program 20 (0x14) when the System Time Nanoseconds register has an accuracy of 1 ns [Bit 9 (TSCTRLSSR) is set in MAC_Timestamp_Control]. When TSCTRLSSR is clear, the Nanoseconds register has a resolution of ~0.465 ns. In this case, you should program a value of 43 (0x2B) which is derived by 20 ns/0.465.
15:8	00h RW	**Sub-nanosecond Increment Value (SNSINC):** This field contains the sub-nanosecond increment value, represented in nanoseconds multiplied by 2^8. This value is accumulated with the sub-nanoseconds field of the subsecond register. For example, when TSCTRLSSR field in the MAC_Timestamp_Control register is set. and if the required increment is 5.3ns, then SSINC should be 0x05 and SNSINC should be 0x4C.
7:0	0h RO	**Reserved**

10.2.302 MAC_SYSTEM_TIME_SECONDS — Offset B08h

The System Time Seconds register, along with System Time Nanoseconds register, indicates the current value of the system time maintained by the MAC. Though it is updated on a continuous basis, there is some delay from the actual time because of clock domain transfer latencies (from clk_ptp_ref_i to CSR clock).

Type	Size	Offset	Default
MMIO	32 bit	BAR + B08h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Timestamp Second (TSS):** The value in this field indicates the current value in seconds of the System Time maintained by the MAC.

10.2.303 MAC_SYSTEM_TIME_NANOSECONDS — Offset B0Ch

The System Time Nanoseconds register, along with System Time Seconds register, indicates the current value of the system time maintained by the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B0Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:0	00000000h RO	**Timestamp Sub Seconds (TSSS):** The value in this field has the sub-second representation of time, with an accuracy of 0.46 ns. When Bit 9 is set in MAC_Timestamp_Control, each bit represents 1 ns. The maximum value is 0x3B9A_C9FF after which it rolls-over to zero.

10.2.304 MAC_SYSTEM_TIME_SECONDS_UPDATE — Offset B10h

The System Time Seconds Update register, along with the System Time Nanoseconds Update register, initializes or updates the system time maintained by the MAC. You must write both registers before setting the TSINIT or TSUPDT bits in MAC_Timestamp_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Timestamp Seconds (TSS):** The value in this field is the seconds part of the update. When ADDSUB is reset, this field must be programmed with the seconds part of the update value. When ADDSUB is set, this field must be programmed with the complement of the seconds part of the update value. For example, if 2.000000001 seconds need to be subtracted from the system time, the TSS field in the MAC_Timestamp_Seconds_Update register must be 0xFFFF_FFFE (that is, 2^32 - 2).

10.2.305 MAC_SYSTEM_TIME_NANOSECONDS_UPDATE — Offset B14h

MAC System Time Nanoseconds Update register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Add or Subtract Time (ADDSUB):** When this bit is set, the time value is subtracted with the contents of the update register. When this bit is reset, the time value is added with the contents of the update register. 0x0 (ADD): Add time. 0x1 (SUB): Subtract time.
30:0	00000000h RW	**Timestamp Sub Seconds (TSSS):** The value in this field is the sub-seconds part of the update. When ADDSUB is reset, this field must be programmed with the sub-seconds part of the update value, with an accuracy based on the TSCTRLSSR bit of the MAC_Timestamp_Control register. When ADDSUB is set, this field must be programmed with the complement of the sub-seconds part of the update value as described below. When TSCTRLSSR bit in MAC_Timestamp_Control is set, the programmed value must be 10^9 - <sub-second value>. When TSCTRLSSR bit in MAC_Timestamp_Control is reset, the programmed value must be 2^31 - <sub-second_value>. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, each bit represents an accuracy of 0.46 ns. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, each bit represents 1 ns and the programmed value should not exceed 0x3B9A_C9FF. For example, if 2.000000001 seconds need to be subtracted from the system time, then the TSSS field in the MAC_Timestamp_Nanoseconds_Update register must be 0x7FFF_FFFF (that is, 2^31 - 1), when TSCTRLSSR bit in MAC_Timestamp_Control is reset and 0x3B9A_C9FF (that is, 10^9 - 1), when TSCTRLSSR bit in MAC_Timestamp_Control is set.

10.2.306 MAC_TIMESTAMP_ADDEND — Offset B18h

Timestamp Addend register. This register value is used only when the system time is configured for Fine Update mode (TSCFUPDT bit in the MAC_Timestamp_Control register). The content of this register is added to a 32-bit accumulator in every clock cycle (of clk_ptp_ref_i) and the system time is updated whenever the accumulator overflows.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Timestamp Addend Register (TSAR):** This field indicates the 32-bit time value to be added to the Accumulator register to achieve time synchronization.

10.2.307 MAC_SYSTEM_TIME_HIGHER_WORD_SECONDS — Offset B1Ch

System Time - Higher Word Seconds register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Timestamp Higher Word Register (TSHWR):** This field contains the most-significant 16-bits of timestamp seconds value. This register is optional. You can add this register by selecting the Add IEEE 1588 Higher Word Register option. This register is directly written to initialize the value and it is incremented when there is an overflow from 32-bits of the System Time Seconds register. Access restriction applies. Updated based on the event. Setting 1 sets. Setting 0 clears.

10.2.308 MAC_TIMESTAMP_STATUS — Offset B20h

Timestamp Status register. All bits except Bits[27:25] gets cleared when the application reads this register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:25	00h RO	**Number of Auxiliary Timestamp Snapshots (ATSNS):** This field indicates the number of Snapshots available in the FIFO. A value equal to the selected depth of FIFO (4, 8, or 16) indicates that the Auxiliary Snapshot FIFO is full. These bits are cleared (to 00000) when the Auxiliary snapshot FIFO clear bit is set. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected.
24	0h RO	**Auxiliary Timestamp Snapshot Trigger Missed (ATSSTM):** This bit is set when the Auxiliary timestamp snapshot FIFO is full and external trigger was set. This indicates that the latest snapshot is not stored in the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected. 0x0 (INACTIVE): Auxiliary Timestamp Snapshot Trigger Missed status not detected. 0x1 (ACTIVE): Auxiliary Timestamp Snapshot Trigger Missed status detected.
23:20	0h RO	**Reserved**
19:16	0h RO	**Auxiliary Timestamp Snapshot Trigger Identifier (ATSSTN):** These bits identify the Auxiliary trigger inputs for which the timestamp available in the Auxiliary Snapshot Register is applicable. When more than one bit is set at the same time, it means that corresponding auxiliary triggers were sampled at the same clock. These bits are applicable only if the number of Auxiliary snapshots is more than one. One bit is assigned for each trigger as shown in the following list: - Bit 16: Auxiliary trigger 0 - Bit 17: Auxiliary trigger 1 - Bit 18: Auxiliary trigger 2 - Bit 19: Auxiliary trigger 3 The software can read this register to find the triggers that are set when the timestamp is taken. Access restriction applies. Clears on read. Self-set to 1 on internal event.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Tx Timestamp Status Interrupt Status (TXTSSIS):** In non-EQOS_CORE configurations when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers. When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers, for PTO generated Delay Request and Pdelay request packets. This bit is cleared when the MAC_Tx_Timestamp_Status_Seconds register is read (or write to MAC_Tx_Timestamp_Status_Seconds register when RCWE bit of MAC_CSR_SW_Ctrl register is set). 0x0 (INACTIVE): Tx Timestamp Status Interrupt status not detected. 0x1 (ACTIVE): Tx Timestamp Status Interrupt status detected.
14:6	0h RO	**Reserved**
5	0h RO	**Timestamp Target Time Error (TSTRGTERR1):** This bit is set when the latest target time programmed in the MAC_PPS1_Target_Time_Seconds and MAC_PPS1_Target_Time_Nanoseconds registers elapses. This bit is cleared when the application reads this bit. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Timestamp Target Time Error status not detected. 0x1 (ACTIVE): Timestamp Target Time Error status detected.
4	0h RO	**Timestamp Target Time Reached for Target Time PPS1 (TSTARGT1):** When this bit is set and MCGREN1 of MAC_PPS_Control register is reset, it indicates that the value of system time is greater than or equal to the value specified in the MAC_PPS1_Target_Time_Seconds and MAC_PPS1_Target_Time_Nanoseconds registers. Access restriction applies. When this bit is set and MCGREN1 of MAC_PPS_Control register is set, it indicates that mcgr_dma_req_o[1] is asserted. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
3	0h RO	**Timestamp Target Time Error (TSTRGTERR0):** This bit is set when the latest target time programmed in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers elapses. This bit is cleared when the application reads this bit. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Timestamp Target Time Error status not detected. 0x1 (ACTIVE): Timestamp Target Time Error status detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Auxiliary Timestamp Trigger Snapshot (AUXTSTRIG):** This bit is set high when the auxiliary snapshot is written to the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Auxiliary Timestamp Trigger Snapshot status not detected. 0x1 (ACTIVE): Auxiliary Timestamp Trigger Snapshot status detected.
1	0h RO	**Timestamp Target Time Reached (TSTARGT0):** When this bit is set and MCGREN0 of MAC_PPS_Control register is reset, it indicates that the value of system time is greater than or equal to the value specified in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers. Access restriction applies. When this bit is set and MCGREN0 of MAC_PPS_Control register is set, it indicates that mcgr_dma_req_o[0] is asserted. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
0	0h RO	**Timestamp Seconds Overflow (TSSOVF):** When this bit is set, it indicates that the seconds value of the timestamp (when supporting version 2 format) has overflowed beyond 32'hFFFF_FFFF. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Timestamp Seconds Overflow status not detected. 0x1 (ACTIVE): Timestamp Seconds Overflow status detected.

10.2.309 MAC_TX_TIMESTAMP_STATUS_NANOSECONDS — Offset B30h

This register contains the nanosecond part of timestamp captured for Transmit packets when Tx status is disabled.

The MAC_Tx_Timestamp_Status_Nanoseconds register, along with MAC_Tx_Timestamp_Status_Seconds, gives the 64-bit timestamp captured for the PTP packet successfully transmitted by the MAC. This value is considered to be read by the application when the last byte (bits [31:24]) of MAC_Tx_Timestamp_Status_Nanoseconds is read.

If the application does not read these registers and timestamp of another packet is captured, then either the current timestamp is lost (overwritten) or the new timestamp is lost (dropped), depending on the setting of the TXTSSTSM bit of the MAC_Timestamp_Control register. The status bit TXTSC bit [15] in MAC_Timestamp_Status register is set whenever the MAC transmitter captures the timestamp.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Transmit Timestamp Status Missed (TXTSSMIS):** When this bit is set, it indicates one of the following: - The timestamp of the current packet is ignored if TXTSSTSM bit of the MAC_Timestamp_Control register is reset - The timestamp of the previous packet is overwritten with timestamp of the current packet if TXTSSTSM bit of the MAC_Timestamp_Control register is set. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Transmit Timestamp Status Missed status not detected. 0x1 (ACTIVE): Transmit Timestamp Status Missed status detected.
30:0	00000000h RO	**Transmit Timestamp Status Low (TXTSSLO):** This field contains the 31 bits of the Nanoseconds field of the Transmit packet's captured timestamp.

10.2.310 MAC_TX_TIMESTAMP_STATUS_SECONDS — Offset B34h

The register contains the higher 32 bits of the timestamp (in seconds) captured when a PTP packet is transmitted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Transmit Timestamp Status High (TXTSSHI):** This field contains the lower 32 bits of the Seconds field of Transmit packet's captured timestamp.

10.2.311 MAC_AUXILIARY_CONTROL — Offset B40h

The Auxiliary Timestamp Control register controls the Auxiliary Timestamp snapshot.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW	**Auxiliary Snapshot 1 Enable (ATSEN1):** This bit controls the capturing of Auxiliary Snapshot Trigger 1. When this bit is set, the auxiliary snapshot of the event on ptp_aux_trig_i[1] input is enabled. When this bit is reset, the events on this input are ignored. 0x0 (DISABLE): Auxiliary Snapshot $i is disabled. 0x1 (ENABLE): Auxiliary Snapshot $i is enabled.
4	0h RW	**Auxiliary Snapshot 0 Enable (ATSEN0):** This bit controls the capturing of Auxiliary Snapshot Trigger 0. When this bit is set, the auxiliary snapshot of the event on ptp_aux_trig_i[0] input is enabled. When this bit is reset, the events on this input are ignored. 0x0 (DISABLE): Auxiliary Snapshot $i is disabled. 0x1 (ENABLE): Auxiliary Snapshot $i is enabled.
3:1	0h RO	**Reserved**
0	0h RW	**Auxiliary Snapshot FIFO Clear (ATSFC):** When set, this bit resets the pointers of the Auxiliary Snapshot FIFO. This bit is cleared when the pointers are reset and the FIFO is empty. When this bit is high, the auxiliary snapshots are stored in the FIFO. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Auxiliary Snapshot FIFO Clear is disabled. 0x1 (ENABLE): Auxiliary Snapshot FIFO Clear is enabled.

10.2.312 MAC_AUXILIARY_TIMESTAMP_NANOSECONDS — Offset B48h

The Auxiliary Timestamp Nanoseconds register, along with MAC_Auxiliary_Timestamp_Seconds, gives the 64-bit timestamp stored as auxiliary snapshot. These two registers form the read port of a 64-bit wide FIFO with a depth of 4, 8, or 16 as selected while configuring the core.

You can store multiple snapshots in this FIFO. Bits[29:25] in MAC_Timestamp_Status indicate the fill-level of the FIFO. The top of the FIFO is removed only when the last byte (bits [31:24]) of MAC_Auxiliary_Timestamp_Seconds register is read.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:0	00000000h RO	**Auxiliary Timestamp (AUXTSLO):** Contains the lower 31 bits (nanoseconds field) of the auxiliary timestamp.

10.2.313 MAC_AUXILIARY_TIMESTAMP_SECONDS — Offset B4Ch

The Auxiliary Timestamp - Seconds register contains the lower 32 bits of the Seconds field of the auxiliary timestamp register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B4Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Auxiliary Timestamp (AUXTSHI):** Contains the lower 32 bits of the Seconds field of the auxiliary timestamp.

10.2.314 MAC_TIMESTAMP_INGRESS_ASYM_CORR — Offset B50h

The MAC Timestamp Ingress Asymmetry Correction register contains the Ingress Asymmetry Correction value to be used while updating correction field in PDelay_Resp PTP messages.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**One-Step Timestamp Ingress Asymmetry Correction (OSTIAC):** This field contains the ingress path asymmetry value to be added to correctionField of Pdelay_Resp PTP packet. The programmed value should be in units of nanoseconds and multiplied by 2^16. For example, 2.5 ns is represented as 0x00028000. The value can also be negative, which is represented in 2's complement form with bit 31 representing the sign bit.

10.2.315 MAC_TIMESTAMP_EGRESS_ASYM_CORR — Offset B54h

The MAC Timestamp Egress Asymmetry Correction register contains the Egress Asymmetry Correction value to be used while updating the correction field in PDelay_Req PTP messages.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B54h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**One-Step Timestamp Egress Asymmetry Correction (OSTEAC):** This field contains the egress path asymmetry value to be subtracted from correctionField of Pdelay_Resp PTP packet. The programmed value must be the negated value in units of nanoseconds multiplied by 2^16. For example, if the required correction is +2.5 ns, the programmed value must be 0xFFFD_8000, which is the 2's complement of 0x0002_8000(2.5 * 216). Similarly, if the required correction is -3.3 ns, the programmed value is 0x0003_4CCC (3.3 * 216).

10.2.316 MAC_TIMESTAMP_INGRESS_CORR_NANOSECOND — Offset B58h

This register contains the correction value in nanoseconds to be used with the captured timestamp value in the ingress path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Timestamp Ingress Correction (TSIC):** This field contains the ingress path correction value as defined by the Ingress Correction expression.

10.2.317 MAC_TIMESTAMP_EGRESS_CORR_NANOSECOND — Offset B5Ch

This register contains the correction value in nanoseconds to be used with the captured timestamp value in the egress path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B5Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Timestamp Egress Correction (TSEC):** This field contains the nanoseconds part of the egress path correction value as defined by the Egress Correction expression.

10.2.318 MAC_TIMESTAMP_INGRESS_CORR_SUBNANOSEC — Offset B60h

This register contains the sub-nanosecond part of the correction value to be used with the captured timestamp value, for ingress direction.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**Timestamp Ingress Correction, sub-nanoseconds (TSICSNS):** This field contains the sub-nanoseconds part of the ingress path correction value as defined by the "Ingress Correction" expression.
7:0	0h RO	**Reserved**

10.2.319 MAC_TIMESTAMP_EGRESS_CORR_SUBNANOSEC — Offset B64h

This register contains the sub-nanosecond part of the correction value to be used with the captured timestamp value, for egress direction.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**Timestamp Egress Correction, sub-nanoseconds (TSECSNS):** This field contains the sub-nanoseconds part of the egress path correction value as defined by the "Egress Correction" expression.
7:0	0h RO	**Reserved**

10.2.320 MAC_TIMESTAMP_INGRESS_LATENCY — Offset B68h

This register holds the Ingress MAC latency.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:16	000h RO	**Ingress Timestamp Latency, in sub-nanoseconds (ITLNS):** This register holds the average latency in sub-nanoseconds between the input ports (phy_rxd_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken.
15:8	00h RO	**Ingress Timestamp Latency, in nanoseconds (ITLSNS):** This register holds the average latency in nanoseconds between the input ports (phy_rxd_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken.
7:0	0h RO	**Reserved**

10.2.321 MAC_TIMESTAMP_EGRESS_LATENCY — Offset B6Ch

This register holds the Egress MAC latency.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B6Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:16	000h RO	**Egress Timestamp Latency, in nanoseconds (ETLNS):** This register holds the average latency in nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_txd_o) of the MAC.
15:8	00h RO	**Egress Timestamp Latency, in sub-nanoseconds (ETLSNS):** This register holds the average latency in sub-nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_txd_o) of the MAC.
7:0	0h RO	**Reserved**

10.2.322 MAC_PPS_CONTROL — Offset B70h

PPS Control register.

Bits[30:24] of this register are valid only when four Flexible PPS outputs are selected.
Bits[22:16] are valid only when three or more Flexible PPS outputs are selected.
Bits[14:8] are valid only when two or more Flexible PPS outputs are selected.
Bits[6:4] are valid only when Flexible PPS feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Time Select (TRGTMODSEL1):** When set, 64-bit PTP time is used to capture time at MCGR trigger[0] input. When reset, presentation time is used to capture time at trigger input, maintaining backward compatibility.
27:16	0h RO	**Reserved**
15	0h RW	**MCGR Mode Enable for PPS1 Output (MCGREN1):** This field enables the 1st PPS instance to operate in PPS or MCGR mode. When set it operates in MCGR mode and on reset it operates in PPS mode. 0x0 (DISABLE): 1st PPS instance is disabled to operate in PPS or MCGR mode. 0x1 (ENABLE): 1st PPS instance is enabled to operate in PPS or MCGR mode.
14:13	0h RW	**Target Time Register Mode for PPS1 Output (TIMESEL):** This field indicates the Target Time registers (MAC_PPS1_Target_Time_Seconds and MAC_PPS1_Target_Time_Nanoseconds) mode for PPS1 output signal. 0x0 (ONLY_INT): Target Time registers are programmed only for generating the interrupt event. The Flexible PPS function must not be enabled in this mode, otherwise spurious transitions may be observed on the corresponding Pulse Per Second (PPS) output signal. 0x1 (MCGR): Enables MCGR Interrupt whose status bit is indicated by TSTARGT1 (MAC_Timestamp_Status[4]). 0x2 (INT_ST): Target Time registers are programmed for generating the interrupt event and starting or stopping the PPS0 output signal generation. 0x3 (ONLY_ST): Target Time registers are programmed only for starting or stopping the PPS0 output signal generation. No interrupt is asserted.
12	0h RO	**Reserved**
11:8	0h RW	**Flexible PPS1 Output Control (PPSCMD1):** This field controls the flexible PPS1 output signal. This field is similar to the PPSCMD0 field. If MCGREN1 is set, then PPSCMD1 indicated by these 4 bits [11:8] are taken as Presentation Time Control bits for media clock generation and recovery for comparator instance 1. This field is similar to the PPSCMD0 Presentation Time Control bits. If MCGREN1 is not set then only 3 bits from [10:8] is used as PPSCMD1 and the 4th bit is to be set as 0. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.
7	0h RW	**MCGR Mode Enable for PPS0 Output (MCGREN0):** This field enables the 0th PPS instance to operate in PPS or MCGR mode. When set it operates in MCGR mode and on reset it operates in PPS mode. 0x0 (PPS): 0th PPS instance is enabled to operate in PPS mode. 0x1 (MCGR): 0th PPS instance is enabled to operate in MCGR mode.

Bit Range	Default & Access	Field Name (ID): Description
6:5	0h RW	**Target Time Register Mode for PPS0 Output (TRGTMODSEL0):** Target Time Register Mode for PPS0 Output This field indicates the Target Time registers (MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds) mode for PPS0 output signal. 0x0 (ONLY_INT): Target Time registers are programmed only for generating the interrupt event. The Flexible PPS function must not be enabled in this mode, otherwise spurious transitions may be observed on the corresponding Pulse Per Second (PPS) output signal. 0x1 (MCGR): Enables MCGR Interrupt whose status bit is indicated by TSTARGT0 (MAC_Timestamp_Status[1]) 0x2 (INT_ST): Target Time registers are programmed for generating the interrupt event and starting or stopping the PPS0 output signal generation 0x3 (ONLY_ST): Target Time registers are programmed only for starting or stopping the PPS0 output signal generation. No interrupt is asserted.
4	0h RW	**Flexible PPS Output Mode Enable (PPSEN0):** When this bit is set, Bits[3:0] function as PPSCMD. When this bit is reset, Bits[3:0] function as PPSCTRL (Fixed PPS mode). 0x0 (DISABLE): Flexible PPS Output Mode is disabled. 0x1 (ENABLE): Flexible PPS Output Mode is enabled.

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RW	**PPS Output Frequency Control (PPSCTRL_PPSCMD):** This field controls the frequency of the PPS0 output signal. The default value of PPSCTRL is 0000, and the PPS output is 1 pulse (of width clk_ptp_i) every second. For other values of PPSCTRL, the PPS output becomes a generated clock of following frequencies: - 0001: The binary rollover is 2 Hz, and the digital rollover is 1 Hz. - 0010: The binary rollover is 4 Hz, and the digital rollover is 2 Hz. - 0011: The binary rollover is 8 Hz, and the digital rollover is 4 Hz. - 0100: The binary rollover is 16 Hz, and the digital rollover is 8 Hz. - .. - 1111: The binary rollover is 32.768 KHz and the digital rollover is 16.384 KHz. Note: In the binary rollover mode, the PPS output signal has a duty cycle of 50 percent with these frequencies. In the digital rollover mode, the PPS output frequency is an average number. The actual clock is of different frequency that gets synchronized every second. For example: - When PPSCTRL = 0001, the PPS (1 Hz) has a low period of 537 ms and a high period of 463 ms - When PPSCTRL = 0010, the PPS (2 Hz) is a sequence of One clock of 50 percent duty cycle and 537 ms period Second clock of 463 ms period (268 ms low and 195 ms high) - When PPSCTRL = 0011, the PPS (4 Hz) is a sequence of Three clocks of 50 percent duty cycle and 268 ms period Fourth clock of 195 ms period (134 ms low and 61 ms high) This behavior is because of the non-linear toggling of bits in the digital rollover mode in the MAC_System_Time_Nanoseconds register. or Flexible PPS Output Control Programming these bits with a non-zero value instructs the MAC to initiate an event. When the command is transferred or synchronized to the PTP clock domain, these bits get cleared automatically. The software should ensure that these bits are programmed only when they are 'all-zero'. The following list describes the values of PPSCMD0: - 0000: No Command - 0001: START Single Pulse This command generates single pulse rising at the start point defined in MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds register and of a duration defined in the PPS0 Width Register. - 0010: START Pulse Train This command generates the train of pulses rising at the start point defined in the Target Time Registers and of a duration defined in the PPS0 Width Register and repeated at interval defined in the PPS Interval Register. By default, the PPS pulse train is free-running unless stopped by the 'Stop Pulse train at time' or 'Stop Pulse Train immediately' commands. - 0011: Cancel START This command cancels the START Single Pulse and START Pulse Train commands if the system time has not crossed the programmed start time. - 0100: STOP Pulse train at time This command stops the train of pulses initiated by the START Pulse Train command (PPSCMD = 0010) after the time programmed in the Target Time registers elapses. - 0101: STOP Pulse Train immediately This command immediately stops the train of pulses initiated by the START Pulse Train command (PPSCMD = 0010). - 110: Cancel STOP Pulse train This command cancels the STOP pulse train at time command if the programmed stop time has not elapsed. The PPS pulse train becomes free-running on the successful execution of this command. - 0111-1111: Reserved or Presentation Time Control If MCGREN0 is set then these bits are treated as Presentation time control bits. The following list describes the values of PPSCMD0: - 0000: MCGR operation is not carried out. If set to this value in the mid of clock recovery or generation, all the processing inputs are flushed - 0001: Capture the Presentation time at the rising edge of mcg_pst_trig_i[0] into the MAC_PPS0_Target_Time_Seconds register - 0010: Capture the Presentation time at the falling edge of mcg_pst_trig_i[0] into the MAC_PPS0_Target_Time_Seconds register - 0011: Capture the Presentation time at both edges of mcg_pst_trig_i[0] into the MAC_PPS0_Target_Time_Seconds register - 0100-1000: Reserved - 1001: Toggle output on compare - 1010: Pulse output low on compare for one PTP-clock cycle - 1011: Pulse output high on compare for one PTP-clock cycle - 1100-1111: Reserved

10.2.323 MAC_PPS0_TARGET_TIME_SECONDS — Offset B80h

The PPS Target Time Seconds register, along with PPS Target Time Nanoseconds register, is used to schedule an interrupt event [Bit 1 of MAC_Timestamp_Status] when the system time exceeds the value programmed in these registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Target Time Seconds Register (TSTRH0):** This field stores the time in seconds. When the timestamp value matches or exceeds both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on Target Time mode selected for the corresponding PPS output in the MAC_PPS_Control register. If DWC_EQOS_FLEXI_PPS_OUT_EN is enabled in the configuration and PTGE field of MAC_Timestamp_Control Register is set with Presentation time control set in recovery mode, then these bits indicate the TPT being programmed by the application and in generation mode it indicates the CPT generated at the sampled trigger.

10.2.324 MAC_PPS0_TARGET_TIME_NANOSECONDS — Offset B84h

PPS0 Target Time Nanoseconds register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**PPS Target Time Register Busy (TRGTBUSY0):** The MAC sets this bit when the PPSCMD0 field in the MAC_PPS_Control register is programmed to 010 or 011. Programming the PPSCMD0 field to 010 or 011 instructs the MAC to synchronize the Target Time Registers to the PTP clock domain. The MAC clears this bit after synchronizing the Target Time Registers to the PTP clock domain The application must not update the Target Time Registers when this bit is read as 1. Otherwise, the synchronization of the previous programmed time gets corrupted. 0x0 (INACTIVE): PPS Target Time Register Busy status is not detected. 0x1 (ACTIVE): PPS Target Time Register Busy is detected.
30:0	00000000h RW	**Target Time Low for PPS Register (TTSL0):** This register stores the time in (signed) nanoseconds. When the value of the timestamp matches the value in both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on the TRGTMODSEL0 field (Bits [6:5]) in MAC_PPS_Control. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, this value should be (time in ns / 0.465). The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, this value should not exceed 0x3B9A_C9FF. The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

10.2.325 MAC_PPS0_INTERVAL — Offset B88h

The PPS0 Interval register contains the number of units of sub-second increment value between the rising edges of PPS0 signal output.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Output Signal Interval (PPSINT0):** These bits store the interval between the rising edges of PPS0 signal output. The interval is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if the PTP reference clock is 50 MHz (period of 20 ns), and desired interval between the rising edges of PPS0 signal output is 100 ns (that is, 5 units of sub-second increment value), you should program value 4 (5-1) in this register.

10.2.326 MAC_PPS0_WIDTH — Offset B8Ch

The PPS0 Width register contains the number of units of sub-second increment value between the rising and corresponding falling edges of PPS0 signal output.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B8Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Output Signal Width (PPSWIDTH0):** These bits store the width between the rising edge and corresponding falling edge of PPS0 signal output. The width is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if PTP reference clock is 50 MHz (period of 20 ns), and width between the rising and corresponding falling edges of PPS0 signal output is 80 ns (that is, four units of sub-second increment value), you should program value 3 (4-1) in this register. Note: The value programmed in this register must be lesser than the value programmed in MAC_PPS0_Interval.

10.2.327 MAC_PPS1_TARGET_TIME_SECONDS — Offset B90h

The PPS Target Time Seconds register, along with PPS Target Time Nanoseconds register, is used to schedule an interrupt event [Bit 1 of MAC_Timestamp_Status] when the system time exceeds the value programmed in these registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Target Time Seconds Register (TSTRH1):** This field stores the time in seconds. When the timestamp value matches or exceeds both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on Target Time mode selected for the corresponding PPS output in the MAC_PPS_Control register. If DWC_EQOS_FLEXI_PPS_OUT_EN is enabled in the configuration and PTGE field of MAC_Timestamp_Control Register is set with Presentation time control set in recovery mode, then these bits indicate the TPT being programmed by the application and in generation mode it indicates the CPT generated at the sampled trigger.

10.2.328 MAC_PPS1_TARGET_TIME_NANOSECONDS — Offset B94h

PPS0 Target Time Nanoseconds register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**PPS Target Time Register Busy (TRGTBUSY1):** The MAC sets this bit when the PPSCMD0 field in the MAC_PPS_Control register is programmed to 010 or 011. Programming the PPSCMD0 field to 010 or 011 instructs the MAC to synchronize the Target Time Registers to the PTP clock domain. The MAC clears this bit after synchronizing the Target Time Registers to the PTP clock domain The application must not update the Target Time Registers when this bit is read as 1. Otherwise, the synchronization of the previous programmed time gets corrupted. 0x0 (INACTIVE): PPS Target Time Register Busy status is not detected. 0x1 (ACTIVE): PPS Target Time Register Busy is detected.
30:0	00000000h RW	**Target Time Low for PPS Register (TTSL1):** This register stores the time in (signed) nanoseconds. When the value of the timestamp matches the value in both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on the TRGTMODSEL0 field (Bits [6:5]) in MAC_PPS_Control. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, this value should be (time in ns / 0.465). The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, this value should not exceed 0x3B9A_C9FF. The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

10.2.329 MAC_PPS1_INTERVAL — Offset B98h

The PPS0 Interval register contains the number of units of sub-second increment value between the rising edges of PPS0 signal output.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Output Signal Interval (PPSINT1):** These bits store the interval between the rising edges of PPS0 signal output. The interval is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if the PTP reference clock is 50 MHz (period of 20 ns), and desired interval between the rising edges of PPS0 signal output is 100 ns (that is, 5 units of sub-second increment value), you should program value 4 (5-1) in this register.

10.2.330 MAC_PPS1_WIDTH — Offset B9Ch

The PPS0 Width register contains the number of units of sub-second increment value between the rising and corresponding falling edges of PPS0 signal output.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Output Signal Width (PPSWIDTH1):** These bits store the width between the rising edge and corresponding falling edge of PPS0 signal output. The width is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if PTP reference clock is 50 MHz (period of 20 ns), and width between the rising and corresponding falling edges of PPS0 signal output is 80 ns (that is, four units of sub-second increment value), you should program value 3 (4-1) in this register. Note: The value programmed in this register must be lesser than the value programmed in MAC_PPS0_Interval.

10.2.331 MAC_PTO_CONTROL — Offset BC0h

This register controls the PTP Offload Engine operation. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BC0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**Domain Number (DN):** This field indicates the domain Number in which the PTP node is operating.
7	0h RW	**Disable Peer Delay Response response generation (PDRDIS):** When this bit is set, the Peer Delay Response (Pdelay_Resp) response is not be generated for received Peer Delay Request (Pdelay_Req) request packet, as required by the programmed mode. Note: Setting this bit to 1 affects the normal PTP Offload operation and the time synchronization. So, this bit must be set only if there is problem with Pdelay_Resp generation in Hardware and/or Pdelay_Resp generation is handled by Software. 0x0 (ENABLE): Peer Delay Response response generation is enabled. 0x1 (DISABLE): Peer Delay Response response generation is disabled.
6	0h RW	**Disable PTO Delay Request/Response response generation (DRRDIS):** When this bit is set, the Delay Request and Delay response is not generated for received SYNC and Delay request packet respectively, as required by the programmed mode. 0x0 (ENABLE): PTO Delay Request/Response response generation is enabled. 0x1 (DISABLE): PTO Delay Request/Response response generation is disabled.
5	0h RW	**Automatic PTP Pdelay_Req message Trigger (APDREQTRIG):** When this bit is set, one PTP Pdelay_Req message is transmitted. This bit is automatically cleared after the PTP Pdelay_Req message is transmitted. The application should set the APDREQEN bit for this operation. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Automatic PTP Pdelay_Req message Trigger is disabled. 0x1 (ENABLE): Automatic PTP Pdelay_Req message Trigger is enabled.
4	0h RW	**Automatic PTP SYNC message Trigger (ASYNCTRIG):** When this bit is set, one PTP SYNC message is transmitted. This bit is automatically cleared after the PTP SYNC message is transmitted. The application should set the ASYNCEN bit for this operation. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Automatic PTP SYNC message Trigger is disabled. 0x1 (ENABLE): Automatic PTP SYNC message Trigger is enabled.
3	0h RO	**Reserved**
2	0h RW	**Automatic PTP Pdelay_Req message Enable (APDREQEN):** When this bit is set, PTP Pdelay_Req message is generated periodically based on interval programmed or trigger from application, when the MAC is programmed to be in Peer-to-Peer Transparent mode. 0x0 (DISABLE): Automatic PTP Pdelay_Req message is disabled. 0x1 (ENABLE): Automatic PTP Pdelay_Req message is enabled.
1	0h RW	**Automatic PTP SYNC message Enable (ASYNCEN):** When this bit is set, PTP SYNC message is generated periodically based on interval programmed or trigger from application, when the MAC is programmed to be in Clock Master mode. 0x0 (DISABLE): Automatic PTP SYNC message is disabled. 0x1 (ENABLE): Automatic PTP SYNC message is enabled.
0	0h RW	**PTP Offload Enable (PTOEN):** When this bit is set, the PTP Offload feature is enabled. 0x0 (DISABLE): PTP Offload feature is disabled. 0x1 (ENABLE): PTP Offload feature is enabled.

10.2.332 MAC_SOURCE_PORT_IDENTITY0 — Offset BC4h

This register contains Bits[31:0] of the 80-bit Source Port Identity of the PTP node. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BC4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Source Port Identity 0 (SPI0):** This field indicates bits [31:0] of sourcePortIdentity of PTP node.

10.2.333 MAC_SOURCE_PORT_IDENTITY1 — Offset BC8h

This register contains Bits[63:32] of the 80-bit Source Port Identity of the PTP node. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BC8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Source Port Identity 1 (SPI1):** This field indicates bits [63:32] of sourcePortIdentity of PTP node.

10.2.334 MAC_SOURCE_PORT_IDENTITY2 — Offset BCCh

This register contains Bits[79:64] of the 80-bit Source Port Identity of the PTP node. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BCCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Source Port Identity 2 (SPI2):** This field indicates bits [79:64] of sourcePortIdentity of PTP node.

10.2.335 MAC_LOG_MESSAGE_INTERVAL — Offset BD0h

This register contains the periodic intervals for automatic PTP packet generation. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BD0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**Log Min Pdelay_Req Interval (LMPDRI):** This field indicates logMinPdelayReqInterval of PTP node. This is used to schedule the periodic Pdelay request packet transmission. Allowed values are -15 to 15.Negative value must be represented in 2's-complement form. For example, if the required value is -1, the value programmed must be 0xFF.
23:11	0h RO	**Reserved**
10:8	0h RW	**DRSYNCR:** Delay_Req to SYNC Ratio In Slave mode, it is used for controlling frequency of Delay_Req messages transmitted. - 0: DelayReq generated for every received SYNC - 1: DelayReq generated every alternate reception of SYNC - 2: for every 4 SYNC messages - 3: for every 8 SYNC messages - 4: for every 16 SYNC messages - 5: for every 32 SYNC messages - 6-7: Reserved The master sends this information (logMinDelayReqInterval) in the DelayResp PTP messages to the slave. The GbE Controller Receiver processes this value from the received DelayResp messages and updates this field accordingly. In the Slave mode, the host must not write/update this register unless it has to override the received value. In Master mode, the sum of this field and logSyncInterval (LSI) field is provided in the logMinDelayReqInterval field of the generated multicast Delay_Resp PTP message. Access restriction applies. Updated based on the event. Setting 1 sets. Setting 0 clears. 0x0 (SYNC1): DelayReq generated for every received SYNC. 0x1 (SYNC2): DelayReq generated every alternate reception of SYNC. 0x2 (SYNC4): for every 4 SYNC messages. 0x3 (SYNC8): for every 8 SYNC messages. 0x4 (SYNC16): for every 16 SYNC messages. 0x5 (SYNC32): for every 32 SYNC messages. 0x6 (RSVD): Reserved.
7:0	00h RW	**LSI:** Log Sync Interval This field indicates the periodicity of the automatically generated SYNC message when the PTP node is Master. Allowed values are -15 to 15. Negative value must be represented in 2's-complement form. For example, if the required value is -1, the value programmed must be 0xFF.

10.2.336 MTL_OPERATION_MODE — Offset C00h

The Operation Mode register establishes the Transmit and Receive operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C00h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Flexible Rx parser Enable (FRPE):** When this bit is set to 1, the Programmable Rx Parser functionality is enabled. When the Rx parser is disabled and if the Rx parser is in the middle of the parsing then it gets disabled only after completing the current packet parsing. When the Rx parser is enabled from disabled state then the Rx parser gets activated for the next immediate packet. 0x0 (DISABLE): Flexible Rx parser is disabled. 0x1 (ENABLE): Flexible Rx parser is enabled.
14	0h RW	**RxParser Software Error/Incomplete Parsing Packet Drop Enable (RXPED):** When set to 0, packets encountering software programming errors (NPE/NVE/frame offset overflow errors) or incomplete parsing are forwarded to application with the corresponding RxParser status. When set to 1, backward compatibility is maintained where all above mentioned packets are dropped (when RA is not set). 0x0 (DISABLE): Flexible Rx parser, packet drop in case software error is disabled. 0x1 (ENABLE): Flexible Rx parser, packet drop in case software error is enabled.
13:10	0h RO	**Reserved**
9	0h RW	**Counters Reset (CNTCLR):** When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. If this bit is set along with CNT_PRESET bit, CNT_PRESET has precedence. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Counters are not reset. 0x1 (ENABLE): All counters are reset.
8	0h RW	**Counters Preset (CNTPRST):** When this bit is set, - MTL_TxQ[0-7]_Underflow register is initialized/preset to 12'h7F0. - Missed Packet and Overflow Packet counters in MTL_RxQ[0-7]_Missed_Packet_Overflow_Cnt register is initialized/preset to 12'h7F0. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Counters Preset is disabled. 0x1 (ENABLE): Counters Preset is enabled.
7	0h RO	**Reserved**
6:5	0h RW	**Tx Scheduling Algorithm (SCHALG):** This field indicates the algorithm for Tx scheduling: 0x0 (WRR): WRR algorithm. 0x1 (WFQ): WFQ algorithm when DCB feature is selected.Otherwise, Reserved. 0x2 (DWRR): DWRR algorithm when DCB feature is selected.Otherwise, Reserved. 0x3 (SP): Strict priority algorithm.
4:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Receive Arbitration Algorithm (RAA):** This field is used to select the arbitration algorithm for the Rx side. - 0: Strict priority (SP) Queue 0 has the lowest priority and the last queue has the highest priority. - 1: Weighted Strict Priority (WSP) 0x0 (SP): Strict priority (SP). 0x1 (WSP): Weighted Strict Priority (WSP).
1	0h RW	**Drop Transmit Status (DTXSTS):** When this bit is set, the Tx packet status received from the MAC is dropped in the MTL. When this bit is reset, the Tx packet status received from the MAC is forwarded to the application. 0x0 (DISABLE): Drop Transmit Status is disabled. 0x1 (ENABLE): Drop Transmit Status is enabled.
0	0h RO	**Reserved**

10.2.337 MTL_DBG_CTL — Offset C08h

The FIFO Debug Access Control and Status register controls the operation mode of FIFO debug access.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C08h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18:17	0h RW	**ECC Inject Error Control for Tx, Rx and TSO memories (EIEC):** When EIEE bit of this register is set, following are the errors inserted based on the value encoded in this field. 0x0 (M_1BIT): Insert 1 bit error. 0x1 (M_2BIT): Insert 2 bit errors. 0x2 (M_3BIT): Insert 3 bit errors. 0x3 (M_1BIT_ADDR): Insert 1 bit error in address field.
16	0h RW	**ECC Inject Error Enable for Tx, Rx and TSO memories (EIEE):** When set, enables the ECC error injection feature. When reset, disables the ECC error injection feature. 0x0 (DISABLE): ECC Inject Error for Tx, Rx and TSO memories is disabled. 0x1 (ENABLE): ECC Inject Error for Tx, Rx and TSO memories is enabled.
15	0h RW	**Transmit Status Available Interrupt Status Enable (STSIE):** When this bit is set, an interrupt is generated when Transmit status is available in slave mode. 0x0 (DISABLE): Transmit Packet Available Interrupt Status is disabled. 0x1 (ENABLE): Transmit Packet Available Interrupt Status is enabled.
14	0h RW	**Receive Packet Available Interrupt Status Enable (PKTIE):** When this bit is set, an interrupt is generated when EOP of received packet is written to the Rx FIFO. 0x0 (DISABLE): Receive Packet Available Interrupt Status is disabled. 0x1 (ENABLE): Receive Packet Available Interrupt Status is enabled.

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**FIFO Selected for Access (FIFOSEL):** This field indicates the FIFO selected for debug access: 0x0 (TXFIFO): Tx FIFO. 0x1 (TXSTSFIFO): Tx Status FIFO (only read access when SLVMOD is set). 0x2 (TSOFIFO): TSO FIFO (cannot be accessed when SLVMOD is set). 0x3 (RXFIFO): Rx FIFO.
11	0h RW	**FIFO Write Enable (FIFOWREN):** When this bit is set, it enables the Write operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): FIFO Write is disabled. 0x1 (ENABLE): FIFO Write is enabled.
10	0h RW	**FIFO Read Enable (FIFORDEN):** When this bit is set, it enables the Read operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): FIFO Read is disabled. 0x1 (ENABLE): FIFO Read is enabled.
9	0h RW	**Reset Pointers of Selected FIFO (RSTSEL):** When this bit is set, the pointers of the currently-selected FIFO are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): Reset Pointers of Selected FIFO is disabled. 0x1 (ENABLE): Reset Pointers of Selected FIFO is enabled.
8	0h RW	**Reset All Pointers (RSTALL):** When this bit is set, the pointers of all FIFOs are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): Reset All Pointers is disabled. 0x1 (ENABLE): Reset All Pointers is enabled.
7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6:5	0h RW	**Encoded Packet State (PKTSTATE):** This field is used to write the control information to the Tx FIFO or Rx FIFO. Tx FIFO: - 00: Packet Data - 01: Control Word - 10: SOP Data - 11: EOP Data Rx FIFO: - 00: Packet Data - 01: Normal Status - 10: Last Status - 11: EOP 0x0 (PKT_DATA): Packet Data. 0x1 (CW_NS): Control Word/Normal Status. 0x2 (SOP_LS): SOP Data/Last Status. 0x3 (EOP): EOP Data/EOP.
4	0h RO	**Reserved**
3:2	0h RW	**Byte Enables (BYTEEN):** This field indicates the number of data bytes valid in the data register during Write operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected. 0x0 (B0_VAL): Byte 0 valid. 0x1 (B01_VAL): Byte 0 and Byte 1 are valid. 0x2 (B012_VAL): Byte 0, Byte 1, and Byte 2 are valid. 0x3 (B0123_VAL): All four bytes are valid.
1	0h RW	**Debug Mode Access to FIFO (DBGMOD):** When this bit is set, it indicates that the current access to the FIFO is read, write, and debug access. In this mode, the following access types are allowed: - Read and Write access to Tx FIFO, TSO FIFO, and Rx FIFO - Read access is allowed to Tx Status FIFO. When this bit is reset, it indicates that the current access to the FIFO is slave access bypassing the DMA. In this mode, the following access are allowed: - Write access to the Tx FIFO - Read access to the Rx FIFO and Tx Status FIFO 0x0 (DISABLE): Debug Mode Access to FIFO is disabled. 0x1 (ENABLE): Debug Mode Access to FIFO is enabled.
0	0h RW	**FIFO Debug Access Enable (FDBGEN):** When this bit is set, it indicates that the debug mode access to the FIFO is enabled. When this bit is reset, it indicates that the FIFO can be accessed only through a master interface. 0x0 (DISABLE): FIFO Debug Access is disabled. 0x1 (ENABLE): FIFO Debug Access is enabled.

10.2.338 MTL_DBG_STS — Offset C0Ch

The FIFO Debug Status register contains the status of FIFO debug access.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C0Ch	00000018h

Bit Range	Default & Access	Field Name (ID): Description
31:15	00000h RO	**Remaining Locations in the FIFO (LOCR):** Slave Access Mode: This field indicates the space available in selected FIFO. Debug Access Mode: This field contains the Write or Read pointer value of the selected FIFO during Write or Read operation, respectively.
14:10	0h RO	**Reserved**
9	0h RW	**Transmit Status Available Interrupt Status (STSI):** When set, this bit indicates that the Slave mode Tx packet is transmitted, and the status is available in Tx Status FIFO. This bit is reset when 1 is written to this bit. 0x0 (INACTIVE): Transmit Status Available Interrupt Status not detected. 0x1 (ACTIVE): Transmit Status Available Interrupt Status detected.
8	0h RW	**Receive Packet Available Interrupt Status (PKTI):** When set, this bit indicates that MAC layer has written the EOP of received packet to the Rx FIFO. This bit is reset when 1 is written to this bit. 0x0 (INACTIVE): Receive Packet Available Interrupt Status not detected. 0x1 (ACTIVE): Receive Packet Available Interrupt Status detected.
7:5	0h RO	**Reserved**
4:3	3h RO	**Byte Enables (BYTEEN):** This field indicates the number of data bytes valid in the data register during Read operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected. 0x0 (B0_VAL): Byte 0 valid. 0x1 (B01_VAL): Byte 0 and Byte 1 are valid. 0x2 (B012_VAL): Byte 0, Byte 1, and Byte 2 are valid. 0x3 (B0123_VAL): All four bytes are valid.
2:1	0h RO	**Encoded Packet State (PKTSTATE):** This field is used to get the control or status information of the selected FIFO. Tx FIFO: - 00: Packet Data - 01: Control Word - 10: SOP Data - 11: EOP Data Rx FIFO: - 00: Packet Data - 01: Normal Status - 10: Last Status - 11: EOP This field is applicable only for Tx FIFO and Rx FIFO during Read operation. 0x0 (PKT_DATA): Packet Data. 0x1 (CW_NS): Control Word/Normal Status. 0x2 (SOP_LS): SOP Data/Last Status. 0x3 (EOP): EOP Data/EOP.
0	0h RO	**FIFO Busy (FIFOBUSY):** When set, this bit indicates that a FIFO operation is in progress in the MAC and content of the following fields is not valid: - All other fields of this register - All fields of the MTL_FIFO_Debug_Data register 0x0 (INACTIVE): FIFO Busy not detected. 0x1 (ACTIVE): FIFO Busy detected.

10.2.339 MTL_FIFO_DEBUG_DATA — Offset C10h

The FIFO Debug Data register contains the data to be written to or read from the FIFOs.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**FIFO Debug Data (FDBGDATA):** During debug or slave access write operation, this field contains the data to be written to the Tx FIFO, Rx FIFO, or TSO FIFO. During debug or slave access read operation, this field contains the data read from the Tx FIFO, Rx FIFO, TSO FIFO, or Tx Status FIFO.

10.2.340 MTL_INTERRUPT_STATUS — Offset C20h

The software driver (application) reads this register during interrupt service routine or polling to determine the interrupt status of MTL queues and the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**MTL Rx Parser Interrupt Status (MTLPIS):** This bit indicates that there is an interrupt from Rx Parser Block. To reset this bit, the application must read the MTL_ Rxp_Interrupt_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): MTL Rx Parser Interrupt status not detected. 0x1 (ACTIVE): MTL Rx Parser Interrupt status detected.
22:19	0h RO	**Reserved**
18	0h RO	**EST (TAS- 802.1Qbv) Interrupt Status (ESTIS):** This bit indicates an interrupt event during the operation of 802.1Qbv. To reset this bit, the application must clear the error/event that has caused the Interrupt. 0x0 (INACTIVE): EST (TAS- 802.1Qbv) Interrupt status not detected. 0x1 (ACTIVE): EST (TAS- 802.1Qbv) Interrupt status detected.
17	0h RO	**Debug Interrupt status (DBGIS):** This bit indicates an interrupt event during the slave access. To reset this bit, the application must read the FIFO Debug Access Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Debug Interrupt status not detected. 0x1 (ACTIVE): Debug Interrupt status detected.
16:8	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Queue 7 Interrupt status (Q7IS):** This bit indicates that there is an interrupt from Queue 7. To reset this bit, the application must read the MTL_Q7_Interrupt_Control_Status Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 7 Interrupt status not detected. 0x1 (ACTIVE): Queue 7 Interrupt status detected.
6	0h RO	**Queue 6 Interrupt status (Q6IS):** This bit indicates that there is an interrupt from Queue 6. To reset this bit, the application must read the MTL_Q6_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 6 Interrupt status not detected. 0x1 (ACTIVE): Queue 6 Interrupt status detected.
5	0h RO	**Queue 5 Interrupt status (Q5IS):** This bit indicates that there is an interrupt from Queue 5. To reset this bit, the application must read the MTL_Q5_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 5 Interrupt status not detected. 0x1 (ACTIVE): Queue 5 Interrupt status detected.
4	0h RO	**Queue 4 Interrupt status (Q4IS):** This bit indicates that there is an interrupt from Queue 4. To reset this bit, the application must read the MTL_Q4_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 4 Interrupt status not detected. 0x1 (ACTIVE): Queue 4 Interrupt status detected.
3	0h RO	**Queue 3 Interrupt status (Q3IS):** This bit indicates that there is an interrupt from Queue 3. To reset this bit, the application must read the MTL_Q3_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 3 Interrupt status not detected. 0x1 (ACTIVE): Queue 3 Interrupt status detected.
2	0h RO	**Queue 2 Interrupt status (Q2IS):** This bit indicates that there is an interrupt from Queue 2. To reset this bit, the application must read the MTL_Q2_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 2 Interrupt status not detected. 0x1 (ACTIVE): Queue 2 Interrupt status detected.
1	0h RO	**Queue 1 Interrupt status (Q1IS):** This bit indicates that there is an interrupt from Queue 1. To reset this bit, the application must read the MTL_Q1_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 1 Interrupt status not detected. 0x1 (ACTIVE): Queue 1 Interrupt status detected.
0	0h RO	**Queue 0 Interrupt status (Q0IS):** This bit indicates that there is an interrupt from Queue 0. To reset this bit, the application must read Queue 0 Interrupt Control and Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 0 Interrupt status not detected. 0x1 (ACTIVE): Queue 0 Interrupt status detected.

10.2.341 MTL_RXQ_DMA_MAP0 — Offset C30h

The Receive Queue and DMA Channel Mapping 0 register is reserved in EQOS-CORE and EQOS-MTL configurations.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Queue 3 Enabled for Dynamic (per packet) DMA Channel Selection (Q3DDMACH):** When set, this bit indicates that the packets received in Queue 3 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 3 are routed to the DMA Channel programmed in the Q3MDMACH field (Bits[26:24]). 0x0 (DISABLE): Queue 3 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 3 enabled for DA-based DMA Channel Selection.
27	0h RO	**Reserved**
26:24	0h RW	**Queue 3 Mapped to DMA Channel (Q3MDMACH):** This field controls the routing of the received packet in Queue 3 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q3DDMACH field is reset. Note: The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the others are reserved
23:21	0h RO	**Reserved**
20	0h RW	**Queue 2 Enabled for DA-based DMA Channel Selection (Q2DDMACH):** When set, this bit indicates that the packets received in Queue 2 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 2 are routed to the DMA Channel programmed in the Q2MDMACH field (Bits[18:16]). 0x0 (DISABLE): Queue 2 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 2 enabled for DA-based DMA Channel Selection.
19	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18:16	0h RW	**Queue 2 Mapped to DMA Channel (Q2MDMACH):** This field controls the routing of the received packet in Queue 2 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q2DDMACH field is reset.
15:13	0h RO	**Reserved**
12	0h RW	**Queue 1 Enabled for DA-based DMA Channel Selection (Q1DDMACH):** When set, this bit indicates that the packets received in Queue 1 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 1 are routed to the DMA Channel programmed in the Q1MDMACH field (Bits[10:8]). 0x0 (DISABLE): Queue 1 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 1 enabled for DA-based DMA Channel Selection.
11	0h RO	**Reserved**
10:8	0h RW	**Queue 1 Mapped to DMA Channel (Q1MDMACH):** This field controls the routing of the received packet in Queue 1 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q1DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.
7:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Queue 0 Enabled for DA-based DMA Channel Selection (Q0DDMACH):** When set, this bit indicates that the packets received in Queue 0 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 0 are routed to the DMA Channel programmed in the Q0MDMACH field. 0x0 (DISABLE): Queue 0 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 0 enabled for DA-based DMA Channel Selection.
3	0h RO	**Reserved**
2:0	0h RW	**Queue 0 Mapped to DMA Channel (Q0MDMACH):** This field controls the routing of the packet received in Queue 0 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q0DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.

10.2.342 MTL_RXQ_DMA_MAP1 — Offset C34h

The Receive Queue and DMA Channel Mapping 1 register is reserved in EQOS-CORE and EQOS-MTL configurations.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Queue 7 Enabled for DA-based DMA Channel Selection (Q7DDMACH):** When set, this bit indicates that the packets received in Queue 7 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 7 are routed to the DMA Channel programmed in the Q7MDMACH field. 0x0 (DISABLE): Queue 5 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 5 enabled for DA-based DMA Channel Selection.
27	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
26:24	0h RW	**Queue 7 Mapped to DMA Channel (Q7MDMACH):** This field controls the routing of the packet received in Queue 7 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q7DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.
23:21	0h RO	**Reserved**
20	0h RW	**Queue 6 Enabled for DA-based DMA Channel Selection (Q6DDMACH):** When set, this bit indicates that the packets received in Queue 6 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 6 are routed to the DMA Channel programmed in the Q6MDMACH field. 0x0 (DISABLE): Queue 6 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 6 enabled for DA-based DMA Channel Selection.
19	0h RO	**Reserved**
18:16	0h RW	**Queue 6 Mapped to DMA Channel (Q6MDMACH):** This field controls the routing of the packet received in Queue 6 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q6DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.
15:13	0h RO	**Reserved**
12	0h RW	**Queue 5 Enabled for DA-based DMA Channel Selection (Q5DDMACH):** When set, this bit indicates that the packets received in Queue 5 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 5 are routed to the DMA Channel programmed in the Q5MDMACH field. 0x0 (DISABLE): Queue 5 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 5 enabled for DA-based DMA Channel Selection.
11	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**Queue 5 Mapped to DMA Channel (Q5MDMACH):** This field controls the routing of the packets received in Queue 5 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q5DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.
7:5	0h RO	**Reserved**
4	0h RW	**Queue 4 Enabled for DA-based DMA Channel Selection (Q4DDMACH):** When set, this bit indicates that the packets received in Queue 4 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 4 are routed to the DMA Channel programmed in the Q4MDMACH field. 0x0 (DISABLE): Queue 4 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 4 enabled for DA-based DMA Channel Selection.
3	0h RO	**Reserved**
2:0	0h RW	**Queue 4 Mapped to DMA Channel (Q4MDMACH):** This field controls the routing of the packet received in Queue 4 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q4DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.

10.2.343 MTL_TBS_CTRL — Offset C40h

This register controls the operation of Time Based Scheduling.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RW	**Launch Expiry Offset (LEOS):** The value in units of 256 nanoseconds that has to be added to the Launch time to compute the Launch Expiry time. Value valid only when LEOV is set. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value.
7	0h RO	**Reserved**
6:4	0h RW	**Launch Expiry GSN Offset (LEGOS):** The number GSN slots that has to be added to the Launch GSN to compute the Launch Expiry time. Value valid only when LEOV is set.
3:2	0h RO	**Reserved**
1	0h RW	**Launch Expiry Offset Valid (LEOV):** When set indicates the LEOS field is valid. When not set, indicates the Launch Expiry Offset is not valid and the MTL must not check for Launch expiry time. 0x0 (INVALID): LEOS field is invalid. 0x1 (VALID): LEOS field is valid.
0	0h RW	**EST offset Mode (ESTM):** When this bit is set, the Launch Time value used in Time Based Scheduling is interpreted as an EST offset value and is added to the Base Time Register (BTR) of the current list. When reset, the Launch Time value is used as an absolute value that should be compared with the System time [39:8]. 0x0 (DISABLE): EST offset Mode is disabled. 0x1 (ENABLE): EST offset Mode is enabled.

10.2.344 MTL_EST_CONTROL — Offset C50h

This register controls the operation of Enhancements to Scheduled Transmission (IEEE802.1Qbv).

Type	Size	Offset	Default
MMIO	32 bit	BAR + C50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**PTP Time Offset Value (PTOV):** The value of PTP Clock period multiplied by 6 in nanoseconds. This value is needed to avoid transmission overruns at the beginning of the installation of a new GCL.
23:12	000h RW	**Current Time Offset Value (CTOV):** Provides a 12 bit time offset value in nano second that is added to the current time to compensate for all the implementation pipeline delays such as the CDC sync delay, buffering delays, data path delays etc. This offset helps to ensure that the impact of gate controls is visible on the line exactly at the pre-determined schedule (or as close to the schedule as possible).
11	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**Time Interval Left Shift Amount (TILS):** This field provides the left shift amount for the programmed Time Interval values used in the Gate Control Lists. - 000: No left shift needed (equal to x1ns) - 001: Left shift TI by 1 bit (equal to x2ns) - 010: Left shift TI by 2 bits (equal to x4ns) - . - . - 100: Left shift TI by 7 bits (equal to x128ns) Based on the configuration one or more bits of this field should be treated as Reserved/Read-Only.
7:6	0h RW	**Loop Count to report Scheduling Error (LCSE):** Programmable number of GCL list iterations before reporting an HLBS error defined in EST_Status register. 0x0 (M_4_ITERNS): 4 iterations. 0x1 (M_8_ITERNS): 8 iterations. 0x2 (M_16_ITERNS): 16 iterations. 0x3 (M_32_ITERNS): 32 iterations.
5	0h RW	**Drop Frames causing Scheduling Error (DFBS):** When set frames reported to cause HOL Blocking due to not getting scheduled (HLBS field of EST_Status register) after 4,8,16,32 (based on LCSE field of this register) GCL iterations are dropped. 0x0 (DONT_DROP): Do not Drop Frames causing Scheduling Error. 0x1 (DROP): Drop Frames causing Scheduling Error.
4	0h RW	**Do not Drop frames during Frame Size Error (DDBF):** When set, frames are not be dropped during Head-of-Line blocking due to Frame Size Error (HLBF field of EST_Status register). 0x0 (DROP): Drop frames during Frame Size Error. 0x1 (DONT_DROP): Do not Drop frames during Frame Size Error.
3:2	0h RO	**Reserved**
1	0h RW	**Switch to S/W owned list (SSWL):** When set indicates that the software has programmed that list that it currently owns (SWOL) and the hardware should switch to the new list based on the new BTR. Hardware clears this bit when the switch to the SWOL happens to indicate the completion of the switch or when an BTR error (BTRE in Status register) is set. When BTRE is set this bit is cleared but SWOL is not updated as the switch was not successful. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Switch to S/W owned list is disabled. 0x1 (ENABLE): Switch to S/W owned list is enabled.
0	0h RW	**Enable EST (EEST):** When reset, the gate control list processing is halted and all gates are assumed to be in Open state. Should be set for the hardware to start processing the gate control lists. During the toggle from 0 to 1, the gate control list processing starts only after the SSWL bit it set. If any uncorrectable error is detected in the EST memory the hardware resets this bit and disables the EST function. 0x0 (DISABLE): EST is disabled. 0x1 (ENABLE): EST is enabled.

10.2.345 MTL_EST_STATUS — Offset C58h

This register provides Status related to Enhancements to Scheduled Transmission (IEEE802.1Qbv).

Type	Size	Offset	Default
MMIO	32 bit	BAR + C58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**Current GCL Slot Number (CGSN):** Indicates the slot number of the GCL list. Slot number is a modulo 16 count of the GCL List loops executed so far. Even if a new GCL list is installed, the count is incremental.
15:8	00h RO	**BTR Error Loop Count (BTRL):** Provides the minimum count (N) for which the equation Current Time =< New BTR + (N * New Cycle Time) becomes true. N = "11111111" indicates the iterations exceeded the value of 128 and the hardware was not able to update New BTR to be equal to or greater than Current Time. Software intervention is needed to update the New BTR. Value cleared when BTRE field of this register is cleared.
7	0h RO	**S/W owned list (SWOL):** When '0' indicates Gate control list number "0" is owned by software and when "1" indicates the Gate Control list "1" is owned by the software. Any reads/writes by the software (using indirect access via GCL_Control) is directed to the list indicated by this value by default. The inverse of this value is treated as HWOL. R/W operations performed by hardware are directed to the list pointed by HWOL by default. 0x0 (INACTIVE): Gate control list number "0" is owned by software. 0x1 (ACTIVE): Gate control list number "1" is owned by software.
6:5	0h RO	**Reserved**
4	0h RW	**Constant Gate Control Error (CGCE):** This error occurs when the list length (LLR) is 1 and the Cycle Time (CTR) is less than or equal to the programmed Time Interval (TI) value after the optional Left Shifting. The above programming implies Gates are either always Closed or always Open based on the Gate Control values; the same effect can be achieved by other simpler (non TSN) programming mechanisms. Since the implementation does not support such a programming an error is reported. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Constant Gate Control Error not detected. 0x1 (ACTIVE): Constant Gate Control Error detected.
3	0h RO	**Head-Of-Line Blocking due to Scheduling (HLBS):** Set when the frame is not able to win arbitration and get scheduled even after 4 iterations of the GCL. Indicates to software a potential programming error. The one hot encoded values of the Queue Numbers that are not able to make progress are indicated in the MTL_EST_Sch_Error register. Bit cleared when MTL_EST_Sch_Error register is all zeros. 0x0 (INACTIVE): Head-Of-Line Blocking due to Scheduling not detected. 0x1 (ACTIVE): Head-Of-Line Blocking due to Scheduling detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Head-Of-Line Blocking due to Frame Size (HLBF):** Set when HOL Blocking is noticed on one or more Queues as a result of none of the Time Intervals of gate open in the GCL being greater than or equal to the duration needed for frame size (or frame fragment size when preemption is enabled) transmission. The one hot encoded Queue numbers that are experiencing HLBF are indicated in the MTL_EST_Frm_Size_Error register. Additionally, the first Queue number that experienced HLBF along with the frame size is captured in MTL_EST_Frm_Size_Capture register. Bit cleared when MTL_EST_Frame_Size_ Error register is all zeros. 0x0 (INACTIVE): Head-Of-Line Blocking due to Frame Size not detected. 0x1 (ACTIVE): Head-Of-Line Blocking due to Frame Size detected.
1	0h RW	**BTR Error (BTRE):** When "1" indicates a programming error in the BTR of SWOL where the programmed value is less than current time. If the BTRL = "11111111", SWOL is not updated and Software should reprogram the BTR to a value greater than current time and then set SSWL to reinitiate the switch to SWOL. Else if the value of BTRL < "11111111", SWOL is updated and this field indicates the number of iterations (of + CycleTime) taken by hardware to update the BTR to a value greater than Current Time. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): BTR Error not detected. 0x1 (ACTIVE): BTR Error detected.
0	0h RW	**Switch to S/W owned list Complete (SWLC):** When "1" indicates the hardware has successfully switched to the SWOL, and the SWOL bit has been updated to that effect. Cleared when the SSWL of EST_Control register transitions from 0 to 1, or on a software write. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Switch to S/W owned list Complete not detected. 0x1 (ACTIVE): Switch to S/W owned list Complete detected.

10.2.346 MTL_EST_SCH_ERROR — Offset C60h

This register provides the One Hot encoded Queue Numbers that are having the Scheduling related error (timeout).

Type	Size	Offset	Default
MMIO	32 bit	BAR + C60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Schedule Error Queue Number (SEQN):** The One Hot Encoded Queue Numbers that have experienced error/timeout described in HLBS field of status register. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.

10.2.347 MTL_EST_FRM_SIZE_ERROR — Offset C64h

This register provides the One Hot encoded Queue Numbers that are having the Frame Size related error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Frame Size Error Queue Number (FEQN):** The One Hot Encoded Queue Numbers that have experienced error described in HLBF field of status register. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.

10.2.348 MTL_EST_FRM_SIZE_CAPTURE — Offset C68h

This register captures the Frame Size and Queue Number of the first occurrence of the Frame Size related error. Up on clearing it captures the data of immediate next occurrence of a similar error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18:16	0h RO	**Queue Number of HLBF (HBFQ):** Captures the binary value of the of the first Queue (number) experiencing HLBF error (see HLBF field of status register). Value once written is not altered by any subsequent queue errors of similar nature. Once cleared the queue number of the next occurring HLBF error is captured. Width is based on the number of Tx Queues configured; remaining bits are Read-Only. Cleared when MTL_EST_Frm_Size_Error register is all zeros.
15	0h RO	**Reserved**
14:0	0000h RO	**Frame Size of HLBF (HBFS):** Captures the Frame Size of the dropped frame related to queue number indicated in HBFQ field of this register. Contents of this register should be considered invalid, if this field is zero. Cleared when MTL_EST_Frm_Size_Error register is all zeros.

10.2.349 MTL_EST_INTR_ENABLE — Offset C70h

This register implements the Interrupt Enable bits for the various events that generate an interrupt. Bit positions have a 1 to 1 correlation with the status bit positions in MTL_ETS_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RW	**Interrupt Enable for CGCE (CGCE):** When set, generates interrupt when the Constant Gate Control Error occurs and is indicated in the status. When reset this event does not generate an interrupt 0x0 (DISABLE): Interrupt for CGCE is disabled. 0x1 (ENABLE): Interrupt for CGCE is enabled.
3	0h RW	**Interrupt Enable for HLBS (IEHS):** When set, generates interrupt when the Head-of-Line Blocking due to Scheduling issue and is indicated in the status. When reset this event does not generate an interrupt. 0x0 (DISABLE): Interrupt for HLBS is disabled. 0x1 (ENABLE): Interrupt for HLBS is enabled.
2	0h RW	**Interrupt Enable for HLBF (IEHF):** When set, generates interrupt when the Head-of-Line Blocking due to Frame Size error occurs and is indicated in the status. When reset this event does not generate an interrupt. 0x0 (DISABLE): Interrupt for HLBF is disabled. 0x1 (ENABLE): Interrupt for HLBF is enabled.
1	0h RW	**Interrupt Enable for BTR Error (IEBE):** When set, generates interrupt when the BTR Error occurs and is indicated in the status. When reset this event does not generate an interrupt. 0x0 (DISABLE): Interrupt for BTR Error is disabled. 0x1 (ENABLE): Interrupt for BTR Error is enabled.
0	0h RW	**Interrupt Enable for Switch List (IECC):** When set, generates interrupt when the configuration change is successful and the hardware has switched to the new list. When reset this event does not generate an interrupt. 0x0 (DISABLE): Interrupt for Switch List is disabled. 0x1 (ENABLE): Interrupt for Switch List is enabled.

10.2.350 MTL_EST_GCL_CONTROL — Offset C80h

This register provides the control information for reading/writing to the Gate Control lists.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:22	0h RW	**ECC Inject Error Control for EST Memory (ESTEIEC):** When EIEE bit of this register is set, following are the errors inserted based on the value encoded in this field. 0x0 (M_1BIT): Insert 1 bit error. 0x1 (M_2BIT): Insert 2 bit errors. 0x2 (M_3BIT): Insert 3 bit errors. 0x3 (M_1BIT_ADDR): Insert 1 bit error in address field.
21	0h RW	**EST ECC Inject Error Enable (ESTEIEE):** When set along with EEST bit of MTL_EST_Control register, enables the ECC error injection feature. When reset, disables the ECC error injection feature. 0x0 (DISABLE): EST ECC Inject Error is disabled. 0x1 (ENABLE): EST ECC Inject Error is enabled.
20:17	0h RO	**Reserved**
16:8	000h RW	**Gate Control List Address: (GCLA when GCRR is "0"). (ADDR):** Provides the address (row number) of the Gate Control List at which the R/W operation has to be performed. By default the Gate Control List pointed by SWOL of MTL_EST_Status is selected for R/W, however if the DBGM bit of this register is set, a debug mode access is given to R/W from DBGB. Gate Control list Related Registers Address: (GCRA when GCRR is "1"). By default the GCL related register set pointed by SWOL of MTL_EST_Status is selected for R/W, however if the DBGM bit of this register is set, a debug mode access is given to R/W from DBGB. Lower 3 bits are only used in this mode, higher order bits are treated as dont cares. - 000: BTR Low (31:0) - 001: BTR High (63:31) - 010: CTR Low (31:0) - 011: CTR High (39:32) - 100: TER (31:0) - 101: LLR (n:0) (where n is (log{512} / log2)) - Others: Reserved
7:6	0h RO	**Reserved**
5	0h RW	**Debug Mode Bank Select (DBGB):** When set to "0" indicates R/W in debug mode should be directed to Bank 0 (GCL0 and corresponding Time related registers). When set to "1" indicates R/W in debug mode should be directed to Bank 1 (GCL1 and corresponding Time related registers). This value is used when DBGM is set and overrides by value of SWOL which is normally used. 0x0 (BANK0): R/W in debug mode should be directed to Bank 0. 0x1 (BANK1): R/W in debug mode should be directed to Bank 1.
4	0h RW	**Debug Mode (DBGM):** When set to "1" indicates R/W in debug mode where the memory bank (for GCL and Time related registers) is explicitly provided by DBGB value, when set to "0" SWOL bit is used to determine which bank to use. 0x0 (DISABLE): Debug Mode is disabled. 0x1 (ENABLE): Debug Mode is enabled.
3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Gate Control Related Registers (GCRR):** When set to "1" indicates the R/W access is for the GCL related registers (BTR, CTR, TER, LLR) whose address is provided by GCRA. When "0" indicates R/W should be directed to GCL from the address provided by GCLA. 0x0 (DISABLE): Gate Control Related Registers are disabled. 0x1 (ENABLE): Gate Control Related Registers are enabled.
1	0h RW	**Read '1', Write '0': (R1W0):** When set to '1': Read Operation When set to '0': Write Operation. 0x0 (WRITE): Write Operation. 0x1 (READ): Read Operation.
0	0h RW	**Start Read/Write Op (SRWO):** When set indicates a Read/Write Op has started and is in progress. When reset by hardware indicates the R/W Op has completed or an error has occurred (when bit 20 is set) Reads: Data can be read from MTL_EST_GCL_Data register after this bit is reset Writes: MTL_EST_GCL_Data should be programmed with write data before setting SRWO. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Start Read/Write Op disabled. 0x1 (ENABLE): Start Read/Write Op enabled.

10.2.351 MTL_EST_GCL_DATA — Offset C84h

This register holds the read data or write data in case of reads and writes respectively.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Gate Control Data (GCD):** The data corresponding to the address selected in the GCL_Control register. Used for both Read and Write operations.

10.2.352 MTL_FPE_CTRL_STS — Offset C90h

This register controls the operation of, and provides status for Frame Preemption (IEEE802.1Qbu/802.3br).

Type	Size	Offset	Default
MMIO	32 bit	BAR + C90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RO	**HRS:** Hold/Release Status - 1: Indicates a Set-and-Hold-MAC operation was last executed and the pMAC is in Hold State. - 0: Indicates a Set-and-Release-MAC operation was last executed and the pMAC is in Release State. 0x0 (SET_REL): Indicates a Set-and-Release-MAC operation was last executed and the pMAC is in Release State. 0x1 (SET_HOLD): Indicates a Set-and-Hold-MAC operation was last executed and the pMAC is in Hold State.
27:16	0h RO	**Reserved**
15:8	00h RW	**Preemption Classification (PEC):** When set indicates the corresponding Queue must be classified as preemptable, when '0' Queue is classified as express. When both EST (Qbv) and Preemption are enabled, Queue-0 is always assumed to be preemptable. When EST (Qbv) is enabled Queues categorized as preemptable here are always assumed to be in "Open" state in the Gate Control List.
7:2	0h RO	**Reserved**
1:0	0h RW	**Additional Fragment Size (AFSZ):** used to indicate, in units of 64 bytes, the minimum number of bytes over 64 bytes required in non-final fragments of preempted frames. The minimum non-final fragment size is (AFSZ +1) * 64 bytes

10.2.353 MTL_FPE_ADVANCE — Offset C94h

This register holds the Hold and Release Advance time.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Release Advance (RADV):** The maximum time in nanoseconds that can elapse between issuing a RELEASE to the MAC and the MAC being ready to resume transmission of preemptable frames, in the absence of there being any express frames available for transmission.
15:0	0000h RW	**Hold Advance (HADV):** The maximum time in nanoseconds that can elapse between issuing a HOLD to the MAC and the MAC ceasing to transmit any preemptable frame that is in the process of transmission or any preemptable frames that are queued for transmission.

10.2.354 MTL_RXP_CONTROL_STATUS — Offset CA0h

The MTL_RXP_Control_Status register establishes the operating mode of Rx Parser and provides some status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CA0h	80FF00FFh

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**RX Parser in Idle state (RXPI):** This status bit is set to 1 when the Rx parser is in Idle State and waiting for a new packet for processing. This bit is used as a handshake with software when parser gets disables. After disabling, when bit is set then software can update the Rx parser instruction table. 0x0 (INACTIVE): RX Parser not in Idle state. 0x1 (ACTIVE): RX Parser in Idle state.
30:24	0h RO	**Reserved**
23:16	FFh RW	**Number of parsable entries in the Instruction table (NPE):** This control indicates the number of parsable entries in the Instruction Memory. This is used in Rx parser logic to detect programming Error. In case number of parsed entries for a packet is more than this entry then NPEOVIS bit in the MTL_RXP_Interrupt_Control_Status register is set.
15:8	0h RO	**Reserved**
7:0	FFh RW	**Number of valid entry address/index in the Instruction table (NVE):** This control indicates the number of valid entries address/index in the Instruction Memory (i.e. when NVE field in register=31, the maximum valid entry address is NVE+1 i.e. addresses/indices=0 to 32, or 33 entries). This is used in Rx parser logic to detect any programming Error. In case while parsing Table address (memory address) found to be more than this maximum valid entry address then NVEOVIS bit in the MTL_RXP_Interrupt_Control_Status register is set. Note: The minimum value of this should be 2.

10.2.355 MTL_RXP_INTERRUPT_CONTROL_STATUS — Offset CA4h

The MTL_RXP_Interrupt_Control_Status registers provides enable control for the interrupts and provides interrupt status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CA4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RW	**Packet Drop due to RF Interrupt Enable (PDRFIE):** When this bit is set, the PDRFIS interrupt is enabled. When this bit is reset, the PDRFIS interrupt is disabled. 0x0 (DISABLE): Packet Drop due to RF Interrupt is disabled. 0x1 (ENABLE): Packet Drop due to RF Interrupt is enabled.
18	0h RW	**Frame Offset Overflow Interrupt Enable (FOOVIE):** When this bit is set, the FOOVIS interrupt is enabled. When this bit is reset, the FOOVIS interrupt is disabled. 0x0 (DISABLE): Frame Offset Overflow Interrupt is disabled. 0x1 (ENABLE): Frame Offset Overflow Interrupt is enabled.
17	0h RW	**Number of Parsable Entries Overflow Interrupt Enable (NPEOVIE):** When this bit is set, the NPEOVIS interrupt is enabled. When this bit is reset, the NPEOVIS interrupt is disabled. 0x0 (DISABLE): Number of Parsable Entries Overflow Interrupt is disabled. 0x1 (ENABLE): Number of Parsable Entries Overflow Interrupt is enabled.
16	0h RW	**Number of Valid Entries Overflow Interrupt Enable (NVEOVIE):** When this bit is set, the NVEOVIS interrupt is enabled. When this bit is reset, the NVEOVIS interrupt is disabled. 0x0 (DISABLE): Number of Valid Entries Overflow Interrupt is disabled. 0x1 (ENABLE): Number of Valid Entries Overflow Interrupt is enabled.
15:4	0h RO	**Reserved**
3	0h RW	**Packet Dropped due to RF Interrupt Status (PDRFIS):** If the Rx Parser result says to drop the packet by setting RF=1 in the instruction memory, then this bit is set to 1. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Packet Dropped due to RF Interrupt Status not detected. 0x1 (ACTIVE): Packet Dropped due to RF Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Frame Offset Overflow Interrupt Status (FOOVIS):** While parsing if the Instruction table entry's 'Frame Offset' found to be more than EOF offset, then then this bit is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Frame Offset Overflow Interrupt Status not detected. 0x1 (ACTIVE): Frame Offset Overflow Interrupt Status detected.
1	0h RW	**Number of Parsable Entries Overflow Interrupt Status (NPEOVIS):** While parsing a packet if the number of parsed entries found to be more than NPE[] (Number of Parseable Entries in MTL_RXP_Control register),then this bit is set to 1. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Number of Parsable Entries Overflow Interrupt Status not detected. 0x1 (ACTIVE): Number of Parsable Entries Overflow Interrupt Status detected.
0	0h RW	**Number of Valid Entry Address/Index Overflow Interrupt Status (NVEOVIS):** While parsing if the Instruction address found to be more than NVE (Number of Valid Entry Address/index in MTL_RXP_Control register), then this bit is set to 1. For example, when NVE field in register=31, the maximum valid entry address/index is NVE+1 i.e. 32 (addresses/indices=0 to 32, or 33 entries), so NVEOVIS is set when currently processed entry indicates next address is 33 or more i.e. 34th or later entries. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Number of Valid Entries Overflow Interrupt Status not detected. 0x1 (ACTIVE): Number of Valid Entries Overflow Interrupt Status detected.

10.2.356 MTL_RXP_DROP_CNT — Offset CA8h

The MTL_RXP_Drop_Cnt register provides the drop count of Rx Parser initiated drops.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CA8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Drop Counter Overflow Bit (RXPDCOVF):** When set, this bit indicates that the MTL_RXP_Drop_cnt (RXPDC) Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Drop count overflow not occurred. 0x1 (ACTIVE): Rx Parser Drop count overflow occurred.
30:0	00000000h RO	**Rx Parser Drop count (RXPDC):** This 31-bit counter is implemented whenever a Rx Parser Drops a packet due to RF =1. The counter is cleared when the register is read.

10.2.357 MTL_RXP_ERROR_CNT — Offset CAChh

The MTL_RXP_Error_Cnt register provides the Rx Parser related error occurrence count.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Error Counter Overflow Bit (RXPECOVF):** When set, this bit indicates that the MTL_RXP_Error_cnt (RXPEC) Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Error count overflow not occurred. 0x1 (ACTIVE): Rx Parser Error count overflow occurred.
30:0	00000000h RO	**Rx Parser Error count (RXPEC):** This 31-bit counter is implemented whenever a Rx Parser encounters following Error scenarios - Entry address >= NVE[] - Number Parsed Entries >= NPE[] - Entry address > EOF data entry address The counter is cleared when the register is read.

10.2.358 MTL_RXP_INDIRECT_ACC_CONTROL_STATUS — Offset CB0h

The MTL_RXP_Indirect_Acc_Control_Status register provides the Indirect Access control and status for Rx Parser memory.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CB0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**FRP Instruction Table Access Busy (STARTBUSY):** When this bit is set to 1 by the software then it indicates to start the Read/Write operation from/to the Rx Parser Memory. Software should read this bit as 0 before issuing read or write request to access the Parser Memory Instructions. This bit when set to 1 indicates that hardware is busy until its gets cleared by hardware and software should not issue any read or write operation. 0x0 (INACTIVE): hardware not busy. 0x1 (ACTIVE): hardware is busy (Read/Write operation from/to the Rx Parser Memory).
30:23	0h RO	**Reserved**
22:21	0h RW	**ECC Inject Error Control for Rx Parser Memory (RXPEIEC):** When EIEE bit of this register is set, following are the errors inserted based on the value encoded in this field. 0x0 (M_1BIT): Insert 1 bit error. 0x1 (M_2BIT): Insert 2 bit errors. 0x2 (M_3BIT): Insert 3 bit errors. 0x3 (M_1BIT_ADDR): Insert 1 bit error in address field.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**ECC Inject Error Enable for Rx Parser Memory (RXPEIEE):** When set, enables the ECC error injection feature. When reset, disables the ECC error injection feature. 0x0 (DISABLE): ECC Inject Error for Rx Parser Memory is disabled. 0x1 (ENABLE): ECC Inject Error for Rx Parser Memory is enabled.
19:17	0h RO	**Reserved**
16	0h RW	**Read Write Control (WRRDN):** When this bit is set to 1 indicates the write operation to the Rx Parser Memory. When this bit is set to 0 indicates the read operation to the Rx Parser Memory. 0x0 (READ): Read operation to the Rx Parser Memory. 0x1 (WRITE): Write operation to the Rx Parser Memory.
15:10	0h RO	**Reserved**
9:0	000h RW	**FRP Instruction Table Offset Address (ADDR):** This field indicates the ADDR of the 32-bit entry in Rx parser instruction table. Each entry has 128-bit (4x32-bit words). There are 256 FRP entries. This must be written by the software before issuing any Read/Write command. The hardware does not support auto-increment of ADDR.

10.2.359 MTL_RXP_INDIRECT_ACC_DATA — Offset CB4h

The MTL_RXP_Indirect_Acc_Data registers holds the data associated to Indirect Access to Rx Parser memory.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CB4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**FRP Instruction Table Write/Read Data (DATA):** Software should write this register before issuing any write command. The hardware provides the read data from the Rx Parser Memory for read operation when STARTBUSY =0 after read command.

10.2.360 MTL_ECC_CONTROL — Offset CC0h

The MTL_ECC_Control register establishes the operating mode of ECC related to MTL memories.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CC0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**MTL ECC Error Address Status Over-ride (MEEAO):** When set, the following error address fields hold the last valid address where the error is detected. When reset, the following error address fields hold the first address where the error is detected. EUEAS/ECEAS of MTL_ECC_Err_Addr_Status register. 0x0 (DISABLE): MTL ECC Error Address Status Over-ride is disabled. 0x1 (ENABLE): MTL ECC Error Address Status Over-ride is enabled.
7:5	0h RO	**Reserved**
4	0h RW	**TSO memory ECC Enable (TSOEE):** When set to 1, enables the ECC feature for TSO memory in DMA. When set to zero, disables the ECC feature for TSO memory in DMA. 0x0 (DISABLE): TSO memory ECC is disabled. 0x1 (ENABLE): TSO memory ECC is enabled.
3	0h RW	**MTL Rx Parser ECC Enable (MRXPEE):** When set to 1, enables the ECC feature for Rx Parser memory. When set to zero, disables the ECC feature for Rx Parser memory. 0x0 (DISABLE): MTL Rx Parser ECC is disabled. 0x1 (ENABLE): MTL Rx Parser ECC is enabled.
2	0h RW	**MTL EST ECC Enable (MESTEE):** When set to 1, enables the ECC feature for EST memory. When set to zero, disables the ECC feature for EST memory. 0x0 (DISABLE): MTL EST ECC is disabled. 0x1 (ENABLE): MTL EST ECC is enabled.
1	0h RW	**MTL Rx FIFO ECC Enable (MRXEE):** When set to 1, enables the ECC feature for MTL Rx FIFO memory. When set to zero, disables the ECC feature for MTL Rx FIFO memory. 0x0 (DISABLE): MTL Rx FIFO ECC is disabled. 0x1 (ENABLE): MTL Rx FIFO ECC is enabled.
0	0h RW	**MTL Tx FIFO ECC Enable (MTXEE):** When set to 1, enables the ECC feature for MTL Tx FIFO memory. When set to zero, disables the ECC feature for MTL Tx FIFO memory. 0x0 (DISABLE): MTL Tx FIFO ECC is disabled. 0x1 (ENABLE): MTL Tx FIFO ECC is enabled.

10.2.361 MTL_SAFETY_INTERRUPT_STATUS — Offset CC4h

The MTL_Safety_Interrupt_Status registers provides Safety interrupt status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CC4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RO	**MTL ECC Uncorrectable error Interrupt Status (MEUIS):** This bit indicates that an uncorrectable error interrupt event in the MTL ECC safety feature. To get the exact cause of the interrupt the application should read the MTL_ECC_Interrupt_Status register. 0x0 (INACTIVE): MTL ECC Uncorrectable error Interrupt Status not detected. 0x1 (ACTIVE): MTL ECC Uncorrectable error Interrupt Status detected.
0	0h RO	**MTL ECC Correctable error Interrupt Status (MECIS):** This bit indicates that a correctable error interrupt event in the MTL ECC safety feature. To get the exact cause of the interrupt the application should read the MTL_ECC_Interrupt_Status register. 0x0 (INACTIVE): MTL ECC Correctable error Interrupt Status not detected. 0x1 (ACTIVE): MTL ECC Correctable error Interrupt Status detected.

10.2.362 MTL_ECC_INTERRUPT_ENABLE — Offset CC8h

The MTL_ECC_Interrupt_Enable register provides enable bits for the ECC interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CC8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RW	**Rx Parser memory Correctable Error Interrupt Enable (RPCEIE):** When set, generates an interrupt when an uncorrectable error is detected at the Rx Parser memory interface. It is indicated in RPCES status bit of MTL_ECC_Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): Rx Parser memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): Rx Parser memory Correctable Error Interrupt is enabled.
11:9	0h RO	**Reserved**
8	0h RW	**EST memory Correctable Error Interrupt Enable (ECEIE):** When set, generates an interrupt when a correctable error is detected at the MTL EST memory interface. It is indicated in the ECES bit of MTL_ECC_Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): EST memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): EST memory Correctable Error Interrupt is enabled.
7:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Rx memory Correctable Error Interrupt Enable (RXCEIE):** When set, generates an interrupt when a correctable error is detected at the MTL Rx memory interface. It is indicated in the RXCES bit of MTL_ECC_Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): Rx memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): Rx memory Correctable Error Interrupt is enabled.
3:1	0h RO	**Reserved**
0	0h RW	**Tx memory Correctable Error Interrupt Enable (TXCEIE):** When set, generates an interrupt when a correctable error is detected at the MTL Tx memory interface. It is indicated in the TXCES bit of MTL_ECC_Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): Tx memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): Tx memory Correctable Error Interrupt is enabled.

10.2.363 MTL_ECC_INTERRUPT_STATUS — Offset CCCh

The MTL_ECC_Interrupt_Status register provides MTL ECC Interrupt Status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CCCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14	0h RW	**Rx Parser memory Uncorrectable Error Status (RPUES):** When set, indicates that an uncorrectable error is detected at Rx Parser memory interface. 0x0 (INACTIVE): Rx Parser memory Uncorrectable Error Status not detected. 0x1 (ACTIVE): Rx Parser memory Uncorrectable Error Status detected.
13	0h RW	**MTL Rx Parser memory Address Mismatch Status (RPAMS):** This bit when set indicates that address mismatch is found for address bus of Rx Parser memory. 0x0 (INACTIVE): MTL Rx Parser memory Address Mismatch Status not detected. 0x1 (ACTIVE): MTL Rx Parser memory Address Mismatch Status detected.
12	0h RW	**MTL Rx Parser memory Correctable Error Status (RPCES):** This bit when set indicates that correctable error is detected at RX Parser memory interface. 0x0 (INACTIVE): MTL Rx Parser memory Correctable Error Status not detected. 0x1 (ACTIVE): MTL Rx Parser memory Correctable Error Status detected.
11	0h RO	**Reserved**
10	0h RW	**MTL EST memory Uncorrectable Error Status (EUES):** When set, indicates that an uncorrectable error is detected at MTL EST memory interface. 0x0 (INACTIVE): MTL EST memory Uncorrectable Error Status not detected. 0x1 (ACTIVE): MTL EST memory Uncorrectable Error Status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**MTL EST memory Address Mismatch Status (EAMS):** This bit when set indicates that address mismatch is found for address bus of MTL EST memory. 0x0 (INACTIVE): MTL EST memory Address Mismatch Status not detected. 0x1 (ACTIVE): MTL EST memory Address Mismatch Status detected.
8	0h RW	**MTL EST memory Correctable Error Status (ECES):** This bit when set indicates that correctable error is detected at the MTL EST memory. 0x0 (INACTIVE): MTL EST memory Correctable Error Status not detected. 0x1 (ACTIVE): MTL EST memory Correctable Error Status detected.
7	0h RO	**Reserved**
6	0h RW	**MTL Rx memory Uncorrectable Error Status (RXUES):** When set, indicates that an uncorrectable error is detected at the MTL Rx memory interface. 0x0 (INACTIVE): MTL Rx memory Uncorrectable Error Status not detected. 0x1 (ACTIVE): MTL Rx memory Uncorrectable Error Status detected.
5	0h RW	**MTL Rx memory Address Mismatch Status (RXAMS):** This bit when set indicates that address mismatch is found for address bus of the MTL Rx memory. 0x0 (INACTIVE): MTL Rx memory Address Mismatch Status not detected. 0x1 (ACTIVE): MTL Rx memory Address Mismatch Status detected.
4	0h RW	**MTL Rx memory Correctable Error Status (RXCES):** This bit when set indicates that correctable error is detected at the MTL Rx memory. 0x0 (INACTIVE): MTL Rx memory correctable Error Status not detected. 0x1 (ACTIVE): MTL Rx memory correctable Error Status detected.
3	0h RO	**Reserved**
2	0h RW	**MTL Tx memory Uncorrectable Error Status (TXUES):** When set, indicates that an uncorrectable error is detected at the MTL TX memory interface. 0x0 (INACTIVE): MTL Tx memory Uncorrectable Error Status not detected. 0x1 (ACTIVE): MTL Tx memory Uncorrectable Error Status detected.
1	0h RW	**MTL Tx memory Address Mismatch Status (TXAMS):** This bit when set indicates that address mismatch is found for address bus of the MTL Tx memory. 0x0 (INACTIVE): MTL Tx memory Address Mismatch Status not detected. 0x1 (ACTIVE): MTL Tx memory Address Mismatch Status detected.
0	0h RW	**MTL Tx memory Correctable Error Status (TXCES):** This bit when set indicates that a correctable error is detected at the MTL Tx memory. 0x0 (INACTIVE): MTL Tx memory Correctable Error Status not detected. 0x1 (ACTIVE): MTL Tx memory Correctable Error Status detected.

10.2.364 MTL_ECC_ERR_STS_RCTL — Offset CD0h

The MTL_ECC_Err_Sts_Rctl register establishes the control for ECC Error status capture.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CD0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW	**Clear Uncorrectable Error Status (CUES):** When this bit is set along with EESRE bit of this register, based on the EMS field of this register, the respective memory's uncorrectable error address and uncorrectable error count values are cleared upon reading. Hardware resets this bit when all the error status values are cleared. 0x0 (INACTIVE): Clear Uncorrectable Error Status not detected. 0x1 (ACTIVE): Clear Uncorrectable Error Status detected.
4	0h RW	**Clear Correctable Error Status (CCES):** When this bit is set along with EESRE bit of this register, based on the EMS field of this register, the respective memory's correctable error address and correctable error count values are cleared upon reading. Hardware resets this bit when all the error status values are cleared. 0x0 (INACTIVE): Clear Correctable Error Status not detected. 0x1 (ACTIVE): Clear Correctable Error Status detected.
3:1	0h RW	**MTL ECC Memory Selection (EMS):** When EESRE bit of this register is set, this field indicates which memory's error status value to be read. The memory selection encoding is as described below. 0x0 (TX_MEM): MTL Tx memory. 0x1 (RX_MEM): MTL Rx memory. 0x2 (EST_MEM): MTL EST memory. 0x3 (RXP_MEM): MTL Rx Parser memory. 0x4 (TSO_MEM): DMA TSO memory.
0	0h RW	**MTL ECC Error Status Read Enable (EESRE):** When this bit is set, based on the EMS field of this register, the respective memory's error status values are captured as described: - The correctable and uncorrectable error count values are captured into MTL_ECC_Err_Cnt_Status register - The address location's of correctable and uncorrectable errors are captured into MTL_ECC_Err_Addr_Status register. Hardware resets this bit when all the status values are captured into the MTL_ECC_Err_Cnt_Status and MTL_ECC_Err_Addr_Status registers. 0x0 (DISABLE): MTL ECC Error Status Read is disabled. 0x1 (ENABLE): MTL ECC Error Status Read is enabled.

10.2.365 MTL_ECC_ERR_ADDR_STATUS — Offset CD4h

The MTL_ECC_Err_Addr_Status register provides the memory addresses for the correctable and uncorrectable errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CD4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**MTL ECC Uncorrectable Error Address Status (EUEAS):** Based on the EMS field of MTL_ECC_Err_Sts_Rctl register, this field holds the respective memory's address locations for which an uncorrectable error or address mismatch is detected. When MEEAO bit of MTL_ECC_Control register is set, this field holds the last valid address of memory for which either an uncorrectable error or an address mismatch is detected. When MEEAO bit of MTL_ECC_Control register is reset, this field holds the first address of the memory for which either an uncorrectable error or address mismatch is detected.
15:0	0000h RO	**MTL ECC Correctable Error Address Status (ECEAS):** Based on the EMS field of MTL_ECC_Err_Sts_Rctl register, this field holds the respective memory's address locations for which a correctable error is detected. When MEEAO bit of MTL_ECC_Control register is set, this field holds the last valid address of memory for which correctable error or address mismatch is detected. When MEEAO bit of MTL_ECC_Control register is reset, this field holds the first address of the memory for which correctable error is detected.

10.2.366 MTL_ECC_ERR_CNTR_STATUS — Offset CD8h

The MTL_ECC_Err_Cntr_Status register provides ECC Error count for Correctable and uncorrectable errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CD8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**MTL ECC Uncorrectable Error Counter Status (EUECS):** Based on the EMS field of MTL_ECC_Err_Cntr_Rctl register, this field holds the respective memory's uncorrectable error count value.
15:8	0h RO	**Reserved**
7:0	00h RO	**MTL ECC Correctable Error Counter Status (ECECS):** Based on the EMS field of MTL_ECC_Err_Cntr_Rctl register, this field holds the respective memory's correctable error count value.

10.2.367 MTL_DPP_CONTROL — Offset CE0h

The MTL_DPP_Control establishes the operating mode of Data Parity protection and error injection.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CE0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW	**Insert Parity error in CSR Read data parity generator (IPECW):** When set to 1, parity bit of first valid data generated by the CSR parity generator (or at PG10 as shown in AXI slave Interface Data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity error in CSR Read data parity generator is disabled. 0x1 (ENABLE): Insert Parity error in CSR Read data parity generator is enabled.
12	0h RW	**Insert Parity error in AXI Slave Write data parity generator (IPEASW):** When set to 1, parity bit of first valid data generated by the AXI parity generator is (or at PG9 as shown in AXI slave Interface Data path parity protection diagram) flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity error in AXI Slave Write data parity generator is disabled. 0x1 (ENABLE): Insert Parity error in AXI Slave Write data parity generator is enabled.
11	0h RW	**Insert Parity error in Rx write-back Descriptor parity generator (IPERD):** When set to 1, parity bit of first valid data generated by the DMA Rx write-back descriptor parity generator(or at PG8 as shown in Receive data path parity protection diagram) is flipped. 0x0 (DISABLE): Insert Parity error in Rx write-back Descriptor parity generator is disabled. 0x1 (ENABLE): Insert Parity error in Rx write-back Descriptor parity generator is enabled.
10	0h RW	**Insert Parity error in Tx write-back Descriptor parity generator (IPETD):** When set to 1, parity bit of first valid data generated by the DMA Tx write-back descriptor parity generator(or at PG4 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity error in Tx write-back Descriptor parity generator is disabled. 0x1 (ENABLE): Insert Parity error in Tx write-back Descriptor parity generator is enabled.
9	0h RW	**Insert Parity Error in DMA TSO parity generator (IPETSO):** When set to 1, parity bit of first valid data generated by the DMA TSO parity generator is (or at PG3 as shown in Transmit data path parity protection diagram) flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in DMA TSO parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in DMA TSO parity generator is enabled.
8	0h RW	**Insert Parity Error in DMA DTX Control word parity generator (IPEDDC):** When set to 1, parity bit of first valid data generated by the DMA DTX Control word parity generator (or at PG2 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in DMA DTX Control word parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in DMA DTX Control word parity generator is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Insert Parity Error in MTL Rx FIFO read control parity generator (IPEMRF):** When set to 1, parity bit of first valid data generated by the MTL Rx FIFO read control parity generator (or at PG7 as shown in Receive data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in MTL Rx FIFO read control parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in MTL Rx FIFO read control parity generator is enabled.
6	0h RW	**Insert Parity Error in MTL Tx Status parity generator (IPEMTS):** When set to 1, parity bit of first valid data generated by the MTL Tx Status parity generator (or at PG6 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in MTL Tx Status parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in MTL Tx Status parity generator is enabled.
5	0h RW	**Insert Parity Error in MTL checksum parity generator (IPEMC):** When set to 1, parity bit of first valid data generated by the MTL checksum parity generator (or at PG5 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once the respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in MTL checksum parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in MTL checksum parity generator is enabled.
4	0h RW	**Insert Parity Error in Interface Data parity generator (IPEID):** When set to 1, parity bit of first valid input data generated by the Interface data parity generator (or at PG1 as shown in Transmit data path parity protection diagram) is flipped. Following are the input data bus on which parity bits are generated based on configuration selected In AHB Config, hrdata_i In AXI config, rdata_m_i In DMA Config, mdc_rdata_i In MTL Config, ati_data_i Hardware clears this bit once the respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in Interface Data parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in Interface Data parity generator is enabled.
3:2	0h RO	**Reserved**
1	0h RW	**Odd Parity Enable (OPE):** When set to 1, enables odd parity protection on all the external interfaces and when set to 0, enables even parity protection on all the external interfaces. 0x0 (DISABLE): Odd Parity is disabled. 0x1 (ENABLE): Odd Parity is enabled.
0	0h RW	**Enable Data path Parity Protection (EDPP):** When set to 1, enables the parity protection for EQOS datapath by generating and checking the parity on EQOS datapath. When set to 0, disables the parity protection for EQOS datapath. 0x0 (DISABLE): Data path Parity Protection is disabled. 0x1 (ENABLE): Data path Parity Protection is enabled.

10.2.368 MTL_TXQ0_OPERATION_MODE — Offset D00h

The Queue 0 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D00h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW	**Transmit Queue Size (TQS):** This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	0h RO	**Reserved**
6:4	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RW	**Transmit Queue Enable (TXQEN):** This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Reserved - 2'b10: Enabled - 2'b11: Reserved This field is Read Only in Single Queue configurations and Read Write in Multiple Queue configurations. Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.
1	0h RW	**Transmit Store and Forward (TSF):** When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should always be set as we do not support cut through mode.
0	0h RW	**Flush Transmit Queue (FTQ):** When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flush Transmit Queue is disabled. 0x1 (ENABLE): Flush Transmit Queue is enabled.

10.2.369 MTL_TXQ0_UNDERFLOW — Offset D04h

The Queue 0 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	BAR + D04h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO	**Overflow Bit for Underflow Packet Counter (UFCNTOVF):** This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter. 0x1 (ACTIVE): Overflow detected for Underflow Packet Counter.
10:0	000h RO	**Underflow Packet Counter (UFFRMCNT):** This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.370 MTL_TXQ0_DEBUG — Offset D08h

The Queue 0 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D08h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RO	**Number of Status Words in Tx Status FIFO of Queue (STXSTSF):** This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	0h RO	**Reserved**
18:16	0h RO	**Number of Packets in the Transmit Queue (PTXQ):** This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.
15:6	0h RO	**Reserved**
5	0h RO	**MTL Tx Status FIFO Full Status (TXSTSFSTS):** When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected. 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**MTL Tx Queue Not Empty Status (TXQSTS):** When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected. 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected.
3	0h RO	**MTL Tx Queue Write Controller Status (TWCSTS):** When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected. 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected.
2:1	0h RO	**MTL Tx Queue Read Controller Status (TRCSTS):** This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state. 0x1 (READ): Read state (transferring data to the MAC transmitter). 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter. 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC.
0	0h RO	**Transmit Queue in Pause (TXQPAUSED):** When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled 0x0 (INACTIVE): Transmit Queue in Pause status is not detected. 0x1 (ACTIVE): Transmit Queue in Pause status is detected.

10.2.371 MTL_TXQ0_ETS_STATUS — Offset D14h

The Queue 0 ETS Status register provides the average traffic transmitted in Queue 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO	**Average Bits per Slot (ABS):** This field contains the average transmitted bits per slot. When the DCB operation is enabled for Queue 0, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

10.2.372 MTL_TXQ0_QUANTUM_WEIGHT — Offset D18h

The Queue 0 Quantum or Weights register contains the quantum value for Deficit Weighted Round Robin (DWRR), weights for the Weighted Round Robin (WRR), and Weighted Fair Queuing (WFQ) for Queue 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**Quantum or Weights (ISCQW):** When the DCB operation is enabled with DWRR algorithm for Queue 0 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. When DCB operation is enabled with WFQ algorithm for Queue 0 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. The higher the programmed weights lesser the bandwidth allocated for the particular Transmit Queue. This is because the weights are used to compute the packet finish time (weights*packet_size). Lesser the finish time, higher the probability of the packet getting scheduled first and using more bandwidth. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 0 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero.

10.2.373 MTL_Q0_INTERRUPT_CONTROL_STATUS — Offset D2Ch

This register contains the interrupt enable and status bits for the queue 0 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Receive Queue Overflow Interrupt Enable (RXOIE):** When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	**Reserved**
16	0h RW	**Receive Queue Overflow Interrupt Status (RXOVFIS):** This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Average Bits Per Slot Interrupt Enable (ABPSIE):** When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	**Transmit Queue Underflow Interrupt Enable (TXUIE):** When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.
7:2	0h RO	**Reserved**
1	0h RW	**Average Bits Per Slot Interrupt Status (ABPSIS):** When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	**Transmit Queue Underflow Interrupt Status (TXUNFIS):** This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

10.2.374 MTL_RXQ0_OPERATION_MODE — Offset D30h

The Queue 0 Receive Operation Mode register establishes the Receive queue operating modes and command.

The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + D30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:20	00h RW	**Receive Queue Size (RQS):** This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
19:14	00h RW	**Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD):** These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:8	00h RW	**Threshold for Activating Flow Control (in half-duplex and full-duplex (RFA):** These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.
7	0h RW	**Enable Hardware Flow Control (EHFC):** When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. 0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.
6	0h RW	**Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF):** When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Receive Queue Store and Forward (RSF):** When this bit is set, the GbE Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.
4	0h RW	**Forward Error Packets (FEP):** When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA. 0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.
3	0h RW	**Forward Undersized Good Packets (FUP):** When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.
2	0h RO	**Reserved**
1:0	0h RW	**Receive Queue Threshold Control (RTC):** These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.

10.2.375 MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT — Offset D34h

The Queue 0 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**Missed Packet Counter Overflow Bit (MISCNTOVF):** When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO	**Missed Packet Counter (MISPKTCNT):** This field indicates the number of packets missed by the GbE Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	**Reserved**
11	0h RO	**Overflow Counter Overflow Bit (OVFCNTOVF):** When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO	**Overflow Packet Counter (OVFPKTCNT):** This field indicates the number of packets discarded by the GbE Controller because of Receive queue overflow. This counter is incremented each time the GbE Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.376 MTL_RXQ0_DEBUG — Offset D38h

The Queue 0 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO	**Number of Packets in Receive Queue (PRXQ):** This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/ Min_Packet_Size.
15:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**MTL Rx Queue Fill-Level Status (RXQSTS):** This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty. 0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.
3	0h RO	**Reserved**
2:1	0h RO	**MTL Rx Queue Read Controller State (RRCSTS):** This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO	**MTL Rx Queue Write Controller Active Status (RWCSTS):** When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

10.2.377 MTL_RXQ0_CONTROL — Offset D3Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**Receive Queue Packet Arbitration (RXQ_FRM_ARBIT):** When this bit is set, the GbE Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the GbE Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the GbE Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	**Receive Queue Weight (RXQ_WEGT):** This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

10.2.378 MTL_TXQ1_OPERATION_MODE — Offset D40h

The Queue 1 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW	**Transmit Queue Size (TQS):** This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	0h RO	**Reserved**
6:4	0h RO	**Reserved**
3:2	0h RW	**Transmit Queue Enable (TXQEN):** This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Enable in AV mode - 2'b10: Enabled - 2'b11: Reserved Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.
1	0h RW	**Transmit Store and Forward (TSF):** When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should always be set as we do not support cut through mode.
0	0h RW	**Flush Transmit Queue (FTQ):** When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flush Transmit Queue is disabled. 0x1 (ENABLE): Flush Transmit Queue is enabled.

10.2.379 MTL_TXQ1_UNDERFLOW — Offset D44h

The Queue 1 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	BAR + D44h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO	**Overflow Bit for Underflow Packet Counter (UFCNTOVF):** This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter. 0x1 (ACTIVE): Overflow detected for Underflow Packet Counter.
10:0	000h RO	**Underflow Packet Counter (UFFRMCNT):** This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.380 MTL_TXQ1_DEBUG — Offset D48h

The Queue 1 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RO	**Number of Status Words in Tx Status FIFO of Queue (STXSTSF):** This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	0h RO	**Reserved**
18:16	0h RO	**Number of Packets in the Transmit Queue (PTXQ):** This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RO	**MTL Tx Status FIFO Full Status (TXSTSFSTS):** When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected. 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected.
4	0h RO	**MTL Tx Queue Not Empty Status (TXQSTS):** When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected. 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected.
3	0h RO	**MTL Tx Queue Write Controller Status (TWCSTS):** When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected. 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected.
2:1	0h RO	**MTL Tx Queue Read Controller Status (TRCSTS):** This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state. 0x1 (READ): Read state (transferring data to the MAC transmitter). 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter. 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC.
0	0h RO	**Transmit Queue in Pause (TXQPAUSED):** When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled 0x0 (INACTIVE): Transmit Queue in Pause status is not detected. 0x1 (ACTIVE): Transmit Queue in Pause status is detected.

10.2.381 MTL_TXQ1_ETS_CONTROL — Offset D50h

The Queue ETS Control register controls the enhanced transmission selection operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:4	0h RW	**Slot Count (SLC):** If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH(#i)_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_TxQ(#i)_ETS_Status register, need to be computed for Queue. The encoding is as follows: 0x0 (M_1_SLOT): 1 slot. 0x1 (M_2_SLOT): 2 slots. 0x2 (M_4_SLOT): 4 slots. 0x3 (M_8_SLOT): 8 slots. 0x4 (M_16_SLOT): 16 slots. 0x5 (RSVD): Reserved.
3	0h RW	**Credit Control (CC):** When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting. When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated. 0x0 (DISABLE): Credit Control is disabled. 0x1 (ENABLE): Credit Control is enabled.
2	0h RW	**AV Algorithm (AVALG):** When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue: This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected. 0x0 (DISABLE): CBS Algorithm is disabled. 0x1 (ENABLE): CBS Algorithm is enabled.
1:0	0h RO	**Reserved**

10.2.382 MTL_TXQ1_ETS_STATUS — Offset D54h

The Queue 1 ETS Status register provides the average traffic transmitted in Queue 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D54h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO	**Average Bits per Slot (ABS):** This field contains the average transmitted bits per slot. If AV operation is enabled, this field is computed over number of slots, programmed in the SLC field of MTL_TxQ(#i)_ETS_CONTROL register. The maximum value of this field is 0x6_4000 in 100 Mbps, 0x3E_8000 in 1000 Mbps and 9C_4000 in 2500 Mbps mode respectively. When the DCB operation is enabled for Queue, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

10.2.383 MTL_TXQ1_QUANTUM_WEIGHT — Offset D58h

The Queue 1 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**ISCQW:** idleSlopeCredit, Quantum or Weights - idleSlopeCredit When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero. - Quantum When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. - Weights When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero. - Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register. - Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size)) - Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time.

10.2.384 MTL_TXQ1_SENDSLOPECREDIT — Offset D5Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D5Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:0	0000h RW	**sendSlopeCredit Value (SSC):** When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission.

10.2.385 MTL_TXQ1_HICREDIT — Offset D60h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**hiCredit Value (HC):** When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is 131,072 * 1,024 = 134,217,728 or 0x0800_0000.

10.2.386 MTL_TXQ1_LOCREDIT — Offset D64h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**loCredit Value (LC):** When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed is corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then (8192*2) * 8 * 1024 = 134,217,728 or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000.

10.2.387 MTL_Q1_INTERRUPT_CONTROL_STATUS — Offset D6Ch

This register contains the interrupt enable and status bits for the queue 1 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D6Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Receive Queue Overflow Interrupt Enable (RXOIE):** When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	**Reserved**
16	0h RW	**Receive Queue Overflow Interrupt Status (RXOVFIS):** This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	**Reserved**
9	0h RW	**Average Bits Per Slot Interrupt Enable (ABPSIE):** When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	**Transmit Queue Underflow Interrupt Enable (TXUIE):** When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW	**Average Bits Per Slot Interrupt Status (ABPSIS):** When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	**Transmit Queue Underflow Interrupt Status (TXUNFIS):** This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

10.2.388 MTL_RXQ1_OPERATION_MODE — Offset D70h

The Queue 1 Receive Operation Mode register establishes the Receive queue operating modes and command.

The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + D70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:20	00h RW	**Receive Queue Size (RQS):** This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
19:14	00h RW	**Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD):** These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:8	00h RW	**Threshold for Activating Flow Control (in half-duplex and full-duplex (RFA):** These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.
7	0h RW	**Enable Hardware Flow Control (EHFC):** When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. 0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.
6	0h RW	**Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF):** When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Receive Queue Store and Forward (RSF):** When this bit is set, the GbE Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.
4	0h RW	**Forward Error Packets (FEP):** When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA. 0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.
3	0h RW	**Forward Undersized Good Packets (FUP):** When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.
2	0h RO	**Reserved**
1:0	0h RW	**Receive Queue Threshold Control (RTC):** These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.

10.2.389 MTL_RXQ1_MISSED_PACKET_OVERFLOW_CNT — Offset D74h

The Queue 1 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D74h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**Missed Packet Counter Overflow Bit (MISCNTOVF):** When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO	**Missed Packet Counter (MISPKTCNT):** This field indicates the number of packets missed by the GbE Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	**Reserved**
11	0h RO	**Overflow Counter Overflow Bit (OVFCNTOVF):** When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO	**Overflow Packet Counter (OVFPKTCNT):** This field indicates the number of packets discarded by the GbE Controller because of Receive queue overflow. This counter is incremented each time the GbE Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.390 MTL_RXQ1_DEBUG — Offset D78h

The Queue 1 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D78h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO	**Number of Packets in Receive Queue (PRXQ):** This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/ Min_Packet_Size.
15:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**MTL Rx Queue Fill-Level Status (RXQSTS):** This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty. 0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.
3	0h RO	**Reserved**
2:1	0h RO	**MTL Rx Queue Read Controller State (RRCSTS):** This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO	**MTL Rx Queue Write Controller Active Status (RWCSTS):** When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

10.2.391 MTL_RXQ1_CONTROL — Offset D7Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D7Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**Receive Queue Packet Arbitration (RXQ_FRM_ARBIT):** When this bit is set, the GbE Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the GbE Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the GbE Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	**Receive Queue Weight (RXQ_WEGT):** This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

10.2.392 MTL_TXQ2_OPERATION_MODE — Offset D80h

The Queue 2 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW	**Transmit Queue Size (TQS):** This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	0h RO	**Reserved**
6:4	0h RO	**Reserved**
3:2	0h RW	**Transmit Queue Enable (TXQEN):** This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Enable in AV mode - 2'b10: Enabled - 2'b11: Reserved Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.
1	0h RW	**Transmit Store and Forward (TSF):** When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should always be set as we do not support cut through mode.
0	0h RW	**Flush Transmit Queue (FTQ):** When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flush Transmit Queue is disabled. 0x1 (ENABLE): Flush Transmit Queue is enabled.

10.2.393 MTL_TXQ2_UNDERFLOW — Offset D84h

The Queue 2 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	BAR + D84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO	**Overflow Bit for Underflow Packet Counter (UFCNTOVF):** This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter. 0x1 (ACTIVE): Overflow detected for Underflow Packet Counter.
10:0	000h RO	**Underflow Packet Counter (UFFRMCNT):** This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.394 MTL_TXQ2_DEBUG — Offset D88h

The Queue 2 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RO	**Number of Status Words in Tx Status FIFO of Queue (STXSTSF):** This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	0h RO	**Reserved**
18:16	0h RO	**Number of Packets in the Transmit Queue (PTXQ):** This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RO	**MTL Tx Status FIFO Full Status (TXSTSFSTS):** When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected. 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected.
4	0h RO	**MTL Tx Queue Not Empty Status (TXQSTS):** When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected. 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected.
3	0h RO	**MTL Tx Queue Write Controller Status (TWCSTS):** When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected. 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected.
2:1	0h RO	**MTL Tx Queue Read Controller Status (TRCSTS):** This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state. 0x1 (READ): Read state (transferring data to the MAC transmitter). 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter. 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC.
0	0h RO	**Transmit Queue in Pause (TXQPAUSED):** When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled 0x0 (INACTIVE): Transmit Queue in Pause status is not detected. 0x1 (ACTIVE): Transmit Queue in Pause status is detected.

10.2.395 MTL_TXQ2_ETS_CONTROL — Offset D90h

The Queue ETS Control register controls the enhanced transmission selection operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:4	0h RW	**Slot Count (SLC):** If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH(#i)_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_TxQ(#i)_ETS_Status register, need to be computed for Queue. The encoding is as follows: 0x0 (M_1_SLOT): 1 slot. 0x1 (M_2_SLOT): 2 slots. 0x2 (M_4_SLOT): 4 slots. 0x3 (M_8_SLOT): 8 slots. 0x4 (M_16_SLOT): 16 slots. 0x5 (RSVD): Reserved.
3	0h RW	**Credit Control (CC):** When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting. When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated. 0x0 (DISABLE): Credit Control is disabled. 0x1 (ENABLE): Credit Control is enabled.
2	0h RW	**AV Algorithm (AVALG):** When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue: This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected. 0x0 (DISABLE): CBS Algorithm is disabled. 0x1 (ENABLE): CBS Algorithm is enabled.
1:0	0h RO	**Reserved**

10.2.396 MTL_TXQ2_ETS_STATUS — Offset D94h

The Queue 2 ETS Status register provides the average traffic transmitted in Queue 2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO	**Average Bits per Slot (ABS):** This field contains the average transmitted bits per slot. If AV operation is enabled, this field is computed over number of slots, programmed in the SLC field of MTL_TxQ(#i)_ETS_CONTROL register. The maximum value of this field is 0x6_4000 in 100 Mbps, 0x3E_8000 in 1000 Mbps and 9C_4000 in 2500 Mbps mode respectively. When the DCB operation is enabled for Queue, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

10.2.397 MTL_TXQ2_QUANTUM_WEIGHT — Offset D98h

The Queue 2 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**ISCQW:** idleSlopeCredit, Quantum or Weights - idleSlopeCredit When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero. - Quantum When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. - Weights When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero. - Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register. - Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size)) - Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time.

10.2.398 MTL_TXQ2_SENDSLOPECREDIT — Offset D9Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:0	0000h RW	**sendSlopeCredit Value (SSC):** When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission.

10.2.399 MTL_TXQ2_HICREDIT — Offset DA0h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DA0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**hiCredit Value (HC):** When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is 131,072 * 1,024 = 134,217,728 or 0x0800_0000.

10.2.400 MTL_TXQ2_LOCREDIT — Offset DA4h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DA4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**loCredit Value (LC):** When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed is corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then (8192*2) * 8 * 1024 = 134,217,728 or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000.

10.2.401 MTL_Q2_INTERRUPT_CONTROL_STATUS — Offset DACh

This register contains the interrupt enable and status bits for the queue 2 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Receive Queue Overflow Interrupt Enable (RXOIE):** When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	**Reserved**
16	0h RW	**Receive Queue Overflow Interrupt Status (RXOVFIS):** This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	**Reserved**
9	0h RW	**Average Bits Per Slot Interrupt Enable (ABPSIE):** When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	**Transmit Queue Underflow Interrupt Enable (TXUIE):** When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW	**Average Bits Per Slot Interrupt Status (ABPSIS):** When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	**Transmit Queue Underflow Interrupt Status (TXUNFIS):** This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

10.2.402 MTL_RXQ2_OPERATION_MODE — Offset DB0h

The Queue 2 Receive Operation Mode register establishes the Receive queue operating modes and command.

The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + DB0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:20	00h RW	**Receive Queue Size (RQS):** This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
19:14	00h RW	**Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD):** These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:8	00h RW	**Threshold for Activating Flow Control (in half-duplex and full-duplex (RFA):** These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.
7	0h RW	**Enable Hardware Flow Control (EHFC):** When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. 0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.
6	0h RW	**Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF):** When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Receive Queue Store and Forward (RSF):** When this bit is set, the GbE Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.
4	0h RW	**Forward Error Packets (FEP):** When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA. 0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.
3	0h RW	**Forward Undersized Good Packets (FUP):** When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.
2	0h RO	**Reserved**
1:0	0h RW	**Receive Queue Threshold Control (RTC):** These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.

10.2.403 MTL_RXQ2_MISSED_PACKET_OVERFLOW_CNT — Offset DB4h

The Queue 2 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DB4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**Missed Packet Counter Overflow Bit (MISCNTOVF):** When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO	**Missed Packet Counter (MISPKTCNT):** This field indicates the number of packets missed by the GbE Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	**Reserved**
11	0h RO	**Overflow Counter Overflow Bit (OVFCNTOVF):** When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO	**Overflow Packet Counter (OVFPKTCNT):** This field indicates the number of packets discarded by the GbE Controller because of Receive queue overflow. This counter is incremented each time the GbE Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.404 MTL_RXQ2_DEBUG — Offset DB8h

The Queue 2 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DB8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO	**Number of Packets in Receive Queue (PRXQ):** This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/ Min_Packet_Size.
15:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**MTL Rx Queue Fill-Level Status (RXQSTS):** This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty. 0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.
3	0h RO	**Reserved**
2:1	0h RO	**MTL Rx Queue Read Controller State (RRCSTS):** This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO	**MTL Rx Queue Write Controller Active Status (RWCSTS):** When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

10.2.405 MTL_RXQ2_CONTROL — Offset DBCh

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DBCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**Receive Queue Packet Arbitration (RXQ_FRM_ARBIT):** When this bit is set, the GbE Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the GbE Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the GbE Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	**Receive Queue Weight (RXQ_WEGT):** This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

10.2.406 MTL_TXQ3_OPERATION_MODE — Offset DC0h

The Queue 3 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DC0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW	**Transmit Queue Size (TQS):** This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	0h RO	**Reserved**
6:4	0h RO	**Reserved**
3:2	0h RW	**Transmit Queue Enable (TXQEN):** This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Enable in AV mode - 2'b10: Enabled - 2'b11: Reserved Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.
1	0h RW	**Transmit Store and Forward (TSF):** When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should always be set as we do not support cut through mode.
0	0h RW	**Flush Transmit Queue (FTQ):** When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flush Transmit Queue is disabled. 0x1 (ENABLE): Flush Transmit Queue is enabled.

10.2.407 MTL_TXQ3_UNDERFLOW — Offset DC4h

The Queue 3 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	BAR + DC4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO	**Overflow Bit for Underflow Packet Counter (UFCNTOVF):** This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter. 0x1 (ACTIVE): Overflow detected for Underflow Packet Counter.
10:0	000h RO	**Underflow Packet Counter (UFFRMCNT):** This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.408 MTL_TXQ3_DEBUG — Offset DC8h

The Queue 3 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DC8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RO	**Number of Status Words in Tx Status FIFO of Queue (STXSTSF):** This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	0h RO	**Reserved**
18:16	0h RO	**Number of Packets in the Transmit Queue (PTXQ):** This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RO	**MTL Tx Status FIFO Full Status (TXSTSFSTS):** When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected. 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected.
4	0h RO	**MTL Tx Queue Not Empty Status (TXQSTS):** When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected. 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected.
3	0h RO	**MTL Tx Queue Write Controller Status (TWCSTS):** When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected. 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected.
2:1	0h RO	**MTL Tx Queue Read Controller Status (TRCSTS):** This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state. 0x1 (READ): Read state (transferring data to the MAC transmitter). 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter. 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC.
0	0h RO	**Transmit Queue in Pause (TXQPAUSED):** When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled 0x0 (INACTIVE): Transmit Queue in Pause status is not detected. 0x1 (ACTIVE): Transmit Queue in Pause status is detected.

10.2.409 MTL_TXQ3_ETS_CONTROL — Offset DD0h

The Queue ETS Control register controls the enhanced transmission selection operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DD0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:4	0h RW	**Slot Count (SLC):** If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH(#i)_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_TxQ(#i)_ETS_Status register, need to be computed for Queue. The encoding is as follows: 0x0 (M_1_SLOT): 1 slot. 0x1 (M_2_SLOT): 2 slots. 0x2 (M_4_SLOT): 4 slots. 0x3 (M_8_SLOT): 8 slots. 0x4 (M_16_SLOT): 16 slots. 0x5 (RSVD): Reserved.
3	0h RW	**Credit Control (CC):** When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting. When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated. 0x0 (DISABLE): Credit Control is disabled. 0x1 (ENABLE): Credit Control is enabled.
2	0h RW	**AV Algorithm (AVALG):** When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue: This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected. 0x0 (DISABLE): CBS Algorithm is disabled. 0x1 (ENABLE): CBS Algorithm is enabled.
1:0	0h RO	**Reserved**

10.2.410 MTL_TXQ3_ETS_STATUS — Offset DD4h

The Queue 3 ETS Status register provides the average traffic transmitted in Queue 3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DD4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO	**Average Bits per Slot (ABS):** This field contains the average transmitted bits per slot. If AV operation is enabled, this field is computed over number of slots, programmed in the SLC field of MTL_TxQ(#i)_ETS_CONTROL register. The maximum value of this field is 0x6_4000 in 100 Mbps, 0x3E_8000 in 1000 Mbps and 9C_4000 in 2500 Mbps mode respectively. When the DCB operation is enabled for Queue, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

10.2.411 MTL_TXQ3_QUANTUM_WEIGHT — Offset DD8h

The Queue 3 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DD8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**ISCQW:** idleSlopeCredit, Quantum or Weights - idleSlopeCredit When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero. - Quantum When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. - Weights When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero. - Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register. - Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size)) - Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time.

10.2.412 MTL_TXQ3_SENDSLOPECREDIT — Offset DDCh

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DDCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:0	0000h RW	**sendSlopeCredit Value (SSC):** When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission.

10.2.413 MTL_TXQ3_HICREDIT — Offset DE0h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DE0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**hiCredit Value (HC):** When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is 131,072 * 1,024 = 134,217,728 or 0x0800_0000.

10.2.414 MTL_TXQ3_LOCREDIT — Offset DE4h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DE4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**loCredit Value (LC):** When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed is corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then (8192*2) * 8 * 1024 = 134,217,728 or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000.

10.2.415 MTL_Q3_INTERRUPT_CONTROL_STATUS — Offset DECh

This register contains the interrupt enable and status bits for the queue 3 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Receive Queue Overflow Interrupt Enable (RXOIE):** When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	**Reserved**
16	0h RW	**Receive Queue Overflow Interrupt Status (RXOVFIS):** This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	**Reserved**
9	0h RW	**Average Bits Per Slot Interrupt Enable (ABPSIE):** When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	**Transmit Queue Underflow Interrupt Enable (TXUIE):** When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW	**Average Bits Per Slot Interrupt Status (ABPSIS):** When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	**Transmit Queue Underflow Interrupt Status (TXUNFIS):** This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

10.2.416 MTL_RXQ3_OPERATION_MODE — Offset DF0h

The Queue 3 Receive Operation Mode register establishes the Receive queue operating modes and command.

The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + DF0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:20	00h RW	**Receive Queue Size (RQS):** This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
19:14	00h RW	**Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD):** These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:8	00h RW	**Threshold for Activating Flow Control (in half-duplex and full-duplex (RFA):** These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.
7	0h RW	**Enable Hardware Flow Control (EHFC):** When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. 0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.
6	0h RW	**Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF):** When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Receive Queue Store and Forward (RSF):** When this bit is set, the GbE Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.
4	0h RW	**Forward Error Packets (FEP):** When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA. 0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.
3	0h RW	**Forward Undersized Good Packets (FUP):** When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.
2	0h RO	**Reserved**
1:0	0h RW	**Receive Queue Threshold Control (RTC):** These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.

10.2.417 MTL_RXQ3_MISSED_PACKET_OVERFLOW_CNT — Offset DF4h

The Queue 3 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DF4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**Missed Packet Counter Overflow Bit (MISCNTOVF):** When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO	**Missed Packet Counter (MISPKTCNT):** This field indicates the number of packets missed by the GbE Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	**Reserved**
11	0h RO	**Overflow Counter Overflow Bit (OVFCNTOVF):** When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO	**Overflow Packet Counter (OVFPKTCNT):** This field indicates the number of packets discarded by the GbE Controller because of Receive queue overflow. This counter is incremented each time the GbE Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.418 MTL_RXQ3_DEBUG — Offset DF8h

The Queue 3 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DF8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO	**Number of Packets in Receive Queue (PRXQ):** This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/ Min_Packet_Size.
15:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**MTL Rx Queue Fill-Level Status (RXQSTS):** This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty. 0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.
3	0h RO	**Reserved**
2:1	0h RO	**MTL Rx Queue Read Controller State (RRCSTS):** This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO	**MTL Rx Queue Write Controller Active Status (RWCSTS):** When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

10.2.419 MTL_RXQ3_CONTROL — Offset DFCh

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DFCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**Receive Queue Packet Arbitration (RXQ_FRM_ARBIT):** When this bit is set, the GbE Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the GbE Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the GbE Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	**Receive Queue Weight (RXQ_WEGT):** This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

10.2.420 MTL_TXQ4_OPERATION_MODE — Offset E00h

The Queue 4 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E00h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW	**Transmit Queue Size (TQS):** This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	0h RO	**Reserved**
6:4	0h RO	**Reserved**
3:2	0h RW	**Transmit Queue Enable (TXQEN):** This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Enable in AV mode - 2'b10: Enabled - 2'b11: Reserved Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.
1	0h RW	**Transmit Store and Forward (TSF):** When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should always be set as we do not support cut through mode.
0	0h RW	**Flush Transmit Queue (FTQ):** When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flush Transmit Queue is disabled. 0x1 (ENABLE): Flush Transmit Queue is enabled.

10.2.421 MTL_TXQ4_UNDERFLOW — Offset E04h

The Queue 4 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	BAR + E04h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO	**Overflow Bit for Underflow Packet Counter (UFCNTOVF):** This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter. 0x1 (ACTIVE): Overflow detected for Underflow Packet Counter.
10:0	000h RO	**Underflow Packet Counter (UFFRMCNT):** This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.422 MTL_TXQ4_DEBUG — Offset E08h

The Queue 4 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E08h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RO	**Number of Status Words in Tx Status FIFO of Queue (STXSTSF):** This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	0h RO	**Reserved**
18:16	0h RO	**Number of Packets in the Transmit Queue (PTXQ):** This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RO	**MTL Tx Status FIFO Full Status (TXSTSFSTS):** When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected. 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected.
4	0h RO	**MTL Tx Queue Not Empty Status (TXQSTS):** When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected. 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected.
3	0h RO	**MTL Tx Queue Write Controller Status (TWCSTS):** When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected. 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected.
2:1	0h RO	**MTL Tx Queue Read Controller Status (TRCSTS):** This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state. 0x1 (READ): Read state (transferring data to the MAC transmitter). 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter. 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC.
0	0h RO	**Transmit Queue in Pause (TXQPAUSED):** When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled 0x0 (INACTIVE): Transmit Queue in Pause status is not detected. 0x1 (ACTIVE): Transmit Queue in Pause status is detected.

10.2.423 MTL_TXQ4_ETS_CONTROL — Offset E10h

The Queue ETS Control register controls the enhanced transmission selection operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:4	0h RW	**Slot Count (SLC):** If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH(#i)_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_TxQ(#i)_ETS_Status register, need to be computed for Queue. The encoding is as follows: 0x0 (M_1_SLOT): 1 slot. 0x1 (M_2_SLOT): 2 slots. 0x2 (M_4_SLOT): 4 slots. 0x3 (M_8_SLOT): 8 slots. 0x4 (M_16_SLOT): 16 slots. 0x5 (RSVD): Reserved.
3	0h RW	**Credit Control (CC):** When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting. When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated. 0x0 (DISABLE): Credit Control is disabled. 0x1 (ENABLE): Credit Control is enabled.
2	0h RW	**AV Algorithm (AVALG):** When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue: This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected. 0x0 (DISABLE): CBS Algorithm is disabled. 0x1 (ENABLE): CBS Algorithm is enabled.
1:0	0h RO	**Reserved**

10.2.424 MTL_TXQ4_ETS_STATUS — Offset E14h

The Queue 4 ETS Status register provides the average traffic transmitted in Queue 4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO	**Average Bits per Slot (ABS):** This field contains the average transmitted bits per slot. If AV operation is enabled, this field is computed over number of slots, programmed in the SLC field of MTL_TxQ(#i)_ETS_CONTROL register. The maximum value of this field is 0x6_4000 in 100 Mbps, 0x3E_8000 in 1000 Mbps and 9C_4000 in 2500 Mbps mode respectively. When the DCB operation is enabled for Queue, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

10.2.425 MTL_TXQ4_QUANTUM_WEIGHT — Offset E18h

The Queue 4 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**ISCQW:** idleSlopeCredit, Quantum or Weights - idleSlopeCredit When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero. - Quantum When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. - Weights When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero. - Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register. - Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size)) - Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time.

10.2.426 MTL_TXQ4_SENDSLOPECREDIT — Offset E1Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:0	0000h RW	**sendSlopeCredit Value (SSC):** When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission.

10.2.427 MTL_TXQ4_HICREDIT — Offset E20h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**hiCredit Value (HC):** When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is 131,072 * 1,024 = 134,217,728 or 0x0800_0000.

10.2.428 MTL_TXQ4_LOCREDIT — Offset E24h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E24h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**loCredit Value (LC):** When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed is corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then (8192*2) * 8 * 1024 = 134,217,728 or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000.

10.2.429 MTL_Q4_INTERRUPT_CONTROL_STATUS — Offset E2Ch

This register contains the interrupt enable and status bits for the queue 4 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Receive Queue Overflow Interrupt Enable (RXOIE):** When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	**Reserved**
16	0h RW	**Receive Queue Overflow Interrupt Status (RXOVFIS):** This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	**Reserved**
9	0h RW	**Average Bits Per Slot Interrupt Enable (ABPSIE):** When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	**Transmit Queue Underflow Interrupt Enable (TXUIE):** When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW	**Average Bits Per Slot Interrupt Status (ABPSIS):** When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	**Transmit Queue Underflow Interrupt Status (TXUNFIS):** This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

10.2.430 MTL_RXQ4_OPERATION_MODE — Offset E30h

The Queue 4 Receive Operation Mode register establishes the Receive queue operating modes and command.

The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + E30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:20	00h RW	**Receive Queue Size (RQS):** This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
19:14	00h RW	**Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD):** These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:8	00h RW	**Threshold for Activating Flow Control (in half-duplex and full-duplex (RFA):** These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.
7	0h RW	**Enable Hardware Flow Control (EHFC):** When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. 0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.
6	0h RW	**Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF):** When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Receive Queue Store and Forward (RSF):** When this bit is set, the GbE Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.
4	0h RW	**Forward Error Packets (FEP):** When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA. 0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.
3	0h RW	**Forward Undersized Good Packets (FUP):** When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.
2	0h RO	**Reserved**
1:0	0h RW	**Receive Queue Threshold Control (RTC):** These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.

10.2.431 MTL_RXQ4_MISSED_PACKET_OVERFLOW_CNT — Offset E34h

The Queue 4 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**Missed Packet Counter Overflow Bit (MISCNTOVF):** When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO	**Missed Packet Counter (MISPKTCNT):** This field indicates the number of packets missed by the GbE Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	**Reserved**
11	0h RO	**Overflow Counter Overflow Bit (OVFCNTOVF):** When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO	**Overflow Packet Counter (OVFPKTCNT):** This field indicates the number of packets discarded by the GbE Controller because of Receive queue overflow. This counter is incremented each time the GbE Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.432 MTL_RXQ4_DEBUG — Offset E38h

The Queue 4 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO	**Number of Packets in Receive Queue (PRXQ):** This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/ Min_Packet_Size.
15:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**MTL Rx Queue Fill-Level Status (RXQSTS):** This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty. 0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.
3	0h RO	**Reserved**
2:1	0h RO	**MTL Rx Queue Read Controller State (RRCSTS):** This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO	**MTL Rx Queue Write Controller Active Status (RWCSTS):** When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

10.2.433 MTL_RXQ4_CONTROL — Offset E3Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**Receive Queue Packet Arbitration (RXQ_FRM_ARBIT):** When this bit is set, the GbE Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the GbE Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the GbE Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	**Receive Queue Weight (RXQ_WEGT):** This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

10.2.434 MTL_TXQ5_OPERATION_MODE — Offset E40h

The Queue 5 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW	**Transmit Queue Size (TQS):** This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	0h RO	**Reserved**
6:4	0h RO	**Reserved**
3:2	0h RW	**Transmit Queue Enable (TXQEN):** This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Enable in AV mode - 2'b10: Enabled - 2'b11: Reserved Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.
1	0h RW	**Transmit Store and Forward (TSF):** When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should always be set as we do not support cut through mode.
0	0h RW	**Flush Transmit Queue (FTQ):** When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flush Transmit Queue is disabled. 0x1 (ENABLE): Flush Transmit Queue is enabled.

10.2.435 MTL_TXQ5_UNDERFLOW — Offset E44h

The Queue 5 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	BAR + E44h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO	**Overflow Bit for Underflow Packet Counter (UFCNTOVF):** This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter. 0x1 (ACTIVE): Overflow detected for Underflow Packet Counter.
10:0	000h RO	**Underflow Packet Counter (UFFRMCNT):** This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.436 MTL_TXQ5_DEBUG — Offset E48h

The Queue 5 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RO	**Number of Status Words in Tx Status FIFO of Queue (STXSTSF):** This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	0h RO	**Reserved**
18:16	0h RO	**Number of Packets in the Transmit Queue (PTXQ):** This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RO	**MTL Tx Status FIFO Full Status (TXSTSFSTS):** When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected. 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected.
4	0h RO	**MTL Tx Queue Not Empty Status (TXQSTS):** When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected. 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected.
3	0h RO	**MTL Tx Queue Write Controller Status (TWCSTS):** When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected. 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected.
2:1	0h RO	**MTL Tx Queue Read Controller Status (TRCSTS):** This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state. 0x1 (READ): Read state (transferring data to the MAC transmitter). 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter. 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC.
0	0h RO	**Transmit Queue in Pause (TXQPAUSED):** When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled 0x0 (INACTIVE): Transmit Queue in Pause status is not detected. 0x1 (ACTIVE): Transmit Queue in Pause status is detected.

10.2.437 MTL_TXQ5_ETS_CONTROL — Offset E50h

The Queue ETS Control register controls the enhanced transmission selection operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:4	0h RW	**Slot Count (SLC):** If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH(#i)_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_TxQ(#i)_ETS_Status register, need to be computed for Queue. The encoding is as follows: 0x0 (M_1_SLOT): 1 slot. 0x1 (M_2_SLOT): 2 slots. 0x2 (M_4_SLOT): 4 slots. 0x3 (M_8_SLOT): 8 slots. 0x4 (M_16_SLOT): 16 slots. 0x5 (RSVD): Reserved.
3	0h RW	**Credit Control (CC):** When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting. When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated. 0x0 (DISABLE): Credit Control is disabled. 0x1 (ENABLE): Credit Control is enabled.
2	0h RW	**AV Algorithm (AVALG):** When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue: This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected. 0x0 (DISABLE): CBS Algorithm is disabled. 0x1 (ENABLE): CBS Algorithm is enabled.
1:0	0h RO	**Reserved**

10.2.438 MTL_TXQ5_ETS_STATUS — Offset E54h

The Queue 5 ETS Status register provides the average traffic transmitted in Queue 5.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E54h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO	**Average Bits per Slot (ABS):** This field contains the average transmitted bits per slot. If AV operation is enabled, this field is computed over number of slots, programmed in the SLC field of MTL_TxQ(#i)_ETS_CONTROL register. The maximum value of this field is 0x6_4000 in 100 Mbps, 0x3E_8000 in 1000 Mbps and 9C_4000 in 2500 Mbps mode respectively. When the DCB operation is enabled for Queue, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

10.2.439 MTL_TXQ5_QUANTUM_WEIGHT — Offset E58h

The Queue 5 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 5.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**ISCQW:** idleSlopeCredit, Quantum or Weights - idleSlopeCredit When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero. - Quantum When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. - Weights When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero. - Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register. - Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size)) - Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time.

10.2.440 MTL_TXQ5_SENDSLOPECREDIT — Offset E5Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E5Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:0	0000h RW	**sendSlopeCredit Value (SSC):** When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission.

10.2.441 MTL_TXQ5_HICREDIT — Offset E60h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**hiCredit Value (HC):** When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is 131,072 * 1,024 = 134,217,728 or 0x0800_0000.

10.2.442 MTL_TXQ5_LOCREDIT — Offset E64h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**loCredit Value (LC):** When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed is corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then (8192*2) * 8 * 1024 = 134,217,728 or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000.

10.2.443 MTL_Q5_INTERRUPT_CONTROL_STATUS — Offset E6Ch

This register contains the interrupt enable and status bits for the queue 5 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E6Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Receive Queue Overflow Interrupt Enable (RXOIE):** When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	**Reserved**
16	0h RW	**Receive Queue Overflow Interrupt Status (RXOVFIS):** This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	**Reserved**
9	0h RW	**Average Bits Per Slot Interrupt Enable (ABPSIE):** When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	**Transmit Queue Underflow Interrupt Enable (TXUIE):** When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW	**Average Bits Per Slot Interrupt Status (ABPSIS):** When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	**Transmit Queue Underflow Interrupt Status (TXUNFIS):** This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

10.2.444 MTL_RXQ5_OPERATION_MODE — Offset E70h

The Queue 5 Receive Operation Mode register establishes the Receive queue operating modes and command.

The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + E70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:20	00h RW	**Receive Queue Size (RQS):** This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
19:14	00h RW	**Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD):** These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:8	00h RW	**Threshold for Activating Flow Control (in half-duplex and full-duplex (RFA):** These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.
7	0h RW	**Enable Hardware Flow Control (EHFC):** When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. 0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.
6	0h RW	**Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF):** When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Receive Queue Store and Forward (RSF):** When this bit is set, the GbE Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.
4	0h RW	**Forward Error Packets (FEP):** When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA. 0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.
3	0h RW	**Forward Undersized Good Packets (FUP):** When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.
2	0h RO	**Reserved**
1:0	0h RW	**Receive Queue Threshold Control (RTC):** These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.

10.2.445 MTL_RXQ5_MISSED_PACKET_OVERFLOW_CNT — Offset E74h

The Queue 5 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E74h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**Missed Packet Counter Overflow Bit (MISCNTOVF):** When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO	**Missed Packet Counter (MISPKTCNT):** This field indicates the number of packets missed by the GbE Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	**Reserved**
11	0h RO	**Overflow Counter Overflow Bit (OVFCNTOVF):** When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO	**Overflow Packet Counter (OVFPKTCNT):** This field indicates the number of packets discarded by the GbE Controller because of Receive queue overflow. This counter is incremented each time the GbE Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.446 MTL_RXQ5_DEBUG — Offset E78h

The Queue 5 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E78h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO	**Number of Packets in Receive Queue (PRXQ):** This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/ Min_Packet_Size.
15:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**MTL Rx Queue Fill-Level Status (RXQSTS):** This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty. 0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.
3	0h RO	**Reserved**
2:1	0h RO	**MTL Rx Queue Read Controller State (RRCSTS):** This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO	**MTL Rx Queue Write Controller Active Status (RWCSTS):** When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

10.2.447 MTL_RXQ5_CONTROL — Offset E7Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E7Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**Receive Queue Packet Arbitration (RXQ_FRM_ARBIT):** When this bit is set, the GbE Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the GbE Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the GbE Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	**Receive Queue Weight (RXQ_WEGT):** This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

10.2.448 MTL_TXQ6_OPERATION_MODE — Offset E80h

The Queue 6 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW	**Transmit Queue Size (TQS):** This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	0h RO	**Reserved**
6:4	0h RW	**Reserved**
3:2	0h RW	**Transmit Queue Enable (TXQEN):** This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Enable in AV mode - 2'b10: Enabled - 2'b11: Reserved Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.
1	0h RW	**Transmit Store and Forward (TSF):** When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should be always be set as we do not support cut through mode.
0	0h RW	**Flush Transmit Queue (FTQ):** When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flush Transmit Queue is disabled. 0x1 (ENABLE): Flush Transmit Queue is enabled.

10.2.449 MTL_TXQ6_UNDERFLOW — Offset E84h

The Queue 6 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	BAR + E84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO	**Overflow Bit for Underflow Packet Counter (UFCNTOVF):** This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter. 0x1 (ACTIVE): Overflow detected for Underflow Packet Counter.
10:0	000h RO	**Underflow Packet Counter (UFFRMCNT):** This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.450 MTL_TXQ6_DEBUG — Offset E88h

The Queue 6 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RO	**Number of Status Words in Tx Status FIFO of Queue (STXSTSF):** This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	0h RO	**Reserved**
18:16	0h RO	**Number of Packets in the Transmit Queue (PTXQ):** This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RO	**MTL Tx Status FIFO Full Status (TXSTSFSTS):** When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected. 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected.
4	0h RO	**MTL Tx Queue Not Empty Status (TXQSTS):** When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected. 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected.
3	0h RO	**MTL Tx Queue Write Controller Status (TWCSTS):** When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected. 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected.
2:1	0h RO	**MTL Tx Queue Read Controller Status (TRCSTS):** This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state. 0x1 (READ): Read state (transferring data to the MAC transmitter). 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter. 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC.
0	0h RO	**Transmit Queue in Pause (TXQPAUSED):** When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled 0x0 (INACTIVE): Transmit Queue in Pause status is not detected. 0x1 (ACTIVE): Transmit Queue in Pause status is detected.

10.2.451 MTL_TXQ6_ETS_CONTROL — Offset E90h

The Queue ETS Control register controls the enhanced transmission selection operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:4	0h RW	**Slot Count (SLC):** If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH(#i)_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_TxQ(#i)_ETS_Status register, need to be computed for Queue. The encoding is as follows: 0x0 (M_1_SLOT): 1 slot. 0x1 (M_2_SLOT): 2 slots. 0x2 (M_4_SLOT): 4 slots. 0x3 (M_8_SLOT): 8 slots. 0x4 (M_16_SLOT): 16 slots. 0x5 (RSVD): Reserved.
3	0h RW	**Credit Control (CC):** When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting. When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated. 0x0 (DISABLE): Credit Control is disabled. 0x1 (ENABLE): Credit Control is enabled.
2	0h RW	**AV Algorithm (AVALG):** When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue: This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected. 0x0 (DISABLE): CBS Algorithm is disabled. 0x1 (ENABLE): CBS Algorithm is enabled.
1:0	0h RO	**Reserved**

10.2.452 MTL_TXQ6_ETS_STATUS — Offset E94h

The Queue 6 ETS Status register provides the average traffic transmitted in Queue 6.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO	**Average Bits per Slot (ABS):** This field contains the average transmitted bits per slot. If AV operation is enabled, this field is computed over number of slots, programmed in the SLC field of MTL_TxQ(#i)_ETS_CONTROL register. The maximum value of this field is 0x6_4000 in 100 Mbps, 0x3E_8000 in 1000 Mbps and 9C_4000 in 2500 Mbps mode respectively. When the DCB operation is enabled for Queue, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

10.2.453 MTL_TXQ6_QUANTUM_WEIGHT — Offset E98h

The Queue 6 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 6.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**ISCQW:** idleSlopeCredit, Quantum or Weights - idleSlopeCredit When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero. - Quantum When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. - Weights When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero. - Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register. - Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size)) - Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time.

10.2.454 MTL_TXQ6_SENDSLOPECREDIT — Offset E9Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:0	0000h RW	**sendSlopeCredit Value (SSC):** When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission.

10.2.455 MTL_TXQ6_HICREDIT — Offset EA0h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EA0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**hiCredit Value (HC):** When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is 131,072 * 1,024 = 134,217,728 or 0x0800_0000.

10.2.456 MTL_TXQ6_LOCREDIT — Offset EA4h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EA4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**loCredit Value (LC):** When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed is corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then (8192*2) * 8 * 1024 = 134,217,728 or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000.

10.2.457 MTL_Q6_INTERRUPT_CONTROL_STATUS — Offset EACh

This register contains the interrupt enable and status bits for the queue 6 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Receive Queue Overflow Interrupt Enable (RXOIE):** When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	**Reserved**
16	0h RW	**Receive Queue Overflow Interrupt Status (RXOVFIS):** This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	**Reserved**
9	0h RW	**Average Bits Per Slot Interrupt Enable (ABPSIE):** When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	**Transmit Queue Underflow Interrupt Enable (TXUIE):** When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW	**Average Bits Per Slot Interrupt Status (ABPSIS):** When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	**Transmit Queue Underflow Interrupt Status (TXUNFIS):** This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

10.2.458 MTL_RXQ6_OPERATION_MODE — Offset EB0h

The Queue 6 Receive Operation Mode register establishes the Receive queue operating modes and command.

The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + EB0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:20	00h RW	**Receive Queue Size (RQS):** This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
19:14	00h RW	**Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD):** These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:8	00h RW	**Threshold for Activating Flow Control (in half-duplex and full-duplex (RFA):** These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.
7	0h RW	**Enable Hardware Flow Control (EHFC):** When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. 0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.
6	0h RW	**Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF):** When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Receive Queue Store and Forward (RSF):** When this bit is set, the GbE Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.
4	0h RW	**Forward Error Packets (FEP):** When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA. 0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.
3	0h RW	**Forward Undersized Good Packets (FUP):** When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.
2	0h RO	**Reserved**
1:0	0h RW	**Receive Queue Threshold Control (RTC):** These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.

10.2.459 MTL_RXQ6_MISSED_PACKET_OVERFLOW_CNT — Offset EB4h

The Queue 6 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EB4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**Missed Packet Counter Overflow Bit (MISCNTOVF):** When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO	**Missed Packet Counter (MISPKTCNT):** This field indicates the number of packets missed by the GbE Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	**Reserved**
11	0h RO	**Overflow Counter Overflow Bit (OVFCNTOVF):** When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO	**Overflow Packet Counter (OVFPKTCNT):** This field indicates the number of packets discarded by the GbE Controller because of Receive queue overflow. This counter is incremented each time the GbE Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.460 MTL_RXQ6_DEBUG — Offset EB8h

The Queue 6 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EB8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO	**Number of Packets in Receive Queue (PRXQ):** This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/ Min_Packet_Size.
15:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**MTL Rx Queue Fill-Level Status (RXQSTS):** This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty. 0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.
3	0h RO	**Reserved**
2:1	0h RO	**MTL Rx Queue Read Controller State (RRCSTS):** This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO	**MTL Rx Queue Write Controller Active Status (RWCSTS):** When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

10.2.461 MTL_RXQ6_CONTROL — Offset EBCh

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EBCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**Receive Queue Packet Arbitration (RXQ_FRM_ARBIT):** When this bit is set, the GbE Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the GbE Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the GbE Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	**Receive Queue Weight (RXQ_WEGT):** This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

10.2.462 MTL_TXQ7_OPERATION_MODE — Offset EC0h

The Queue 7 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EC0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW	**Transmit Queue Size (TQS):** This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	0h RO	**Reserved**
6:4	0h RO	**Reserved**
3:2	0h RW	**Transmit Queue Enable (TXQEN):** This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Enable in AV mode - 2'b10: Enabled - 2'b11: Reserved Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.
1	0h RW	**Transmit Store and Forward (TSF):** When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should always be set as we do not support cut through mode.
0	0h RW	**Flush Transmit Queue (FTQ):** When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flush Transmit Queue is disabled. 0x1 (ENABLE): Flush Transmit Queue is enabled.

10.2.463 MTL_TXQ7_UNDERFLOW — Offset EC4h

The Queue 7 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	BAR + EC4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO	**Overflow Bit for Underflow Packet Counter (UFCNTOVF):** This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter. 0x1 (ACTIVE): Overflow detected for Underflow Packet Counter.
10:0	000h RO	**Underflow Packet Counter (UFFRMCNT):** This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.464 MTL_TXQ7_DEBUG — Offset EC8h

The Queue 7 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EC8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RO	**Number of Status Words in Tx Status FIFO of Queue (STXSTSF):** This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	0h RO	**Reserved**
18:16	0h RO	**Number of Packets in the Transmit Queue (PTXQ):** This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RO	**MTL Tx Status FIFO Full Status (TXSTSFSTS):** When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected. 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected.
4	0h RO	**MTL Tx Queue Not Empty Status (TXQSTS):** When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected. 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected.
3	0h RO	**MTL Tx Queue Write Controller Status (TWCSTS):** When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected. 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected.
2:1	0h RO	**MTL Tx Queue Read Controller Status (TRCSTS):** This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state. 0x1 (READ): Read state (transferring data to the MAC transmitter). 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter. 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC.
0	0h RO	**Transmit Queue in Pause (TXQPAUSED):** When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled 0x0 (INACTIVE): Transmit Queue in Pause status is not detected. 0x1 (ACTIVE): Transmit Queue in Pause status is detected.

10.2.465 MTL_TXQ7_ETS_CONTROL — Offset ED0h

The Queue ETS Control register controls the enhanced transmission selection operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + ED0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:4	0h RW	**Slot Count (SLC):** If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH(#i)_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_TxQ(#i)_ETS_Status register, need to be computed for Queue. The encoding is as follows: 0x0 (M_1_SLOT): 1 slot. 0x1 (M_2_SLOT): 2 slots. 0x2 (M_4_SLOT): 4 slots. 0x3 (M_8_SLOT): 8 slots. 0x4 (M_16_SLOT): 16 slots. 0x5 (RSVD): Reserved.
3	0h RW	**Credit Control (CC):** When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting. When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated. 0x0 (DISABLE): Credit Control is disabled. 0x1 (ENABLE): Credit Control is enabled.
2	0h RW	**AV Algorithm (AVALG):** When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue: This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected. 0x0 (DISABLE): CBS Algorithm is disabled. 0x1 (ENABLE): CBS Algorithm is enabled.
1:0	0h RO	**Reserved**

10.2.466 MTL_TXQ7_ETS_STATUS — Offset ED4h

The Queue 7 ETS Status register provides the average traffic transmitted in Queue 7.

Type	Size	Offset	Default
MMIO	32 bit	BAR + ED4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO	**Average Bits per Slot (ABS):** This field contains the average transmitted bits per slot. If AV operation is enabled, this field is computed over number of slots, programmed in the SLC field of MTL_TxQ(#i)_ETS_CONTROL register. The maximum value of this field is 0x6_4000 in 100 Mbps, 0x3E_8000 in 1000 Mbps and 9C_4000 in 2500 Mbps mode respectively. When the DCB operation is enabled for Queue, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

10.2.467 MTL_TXQ7_QUANTUM_WEIGHT — Offset ED8h

The Queue 7 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 7.

Type	Size	Offset	Default
MMIO	32 bit	BAR + ED8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**ISCQW:** idleSlopeCredit, Quantum or Weights - idleSlopeCredit When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero. - Quantum When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. - Weights When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero. - Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register. - Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size)) - Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time.

10.2.468 MTL_TXQ7_SENDSLOPECREDIT — Offset EDCh

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EDCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:0	0000h RW	**sendSlopeCredit Value (SSC):** When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission.

10.2.469 MTL_TXQ7_HICREDIT — Offset EE0h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EE0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**hiCredit Value (HC):** When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is 131,072 * 1,024 = 134,217,728 or 0x0800_0000.

10.2.470 MTL_TXQ7_LOCREDIT — Offset EE4h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EE4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**loCredit Value (LC):** When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed is corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then (8192*2) * 8 * 1024 = 134,217,728 or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000.

10.2.471 MTL_Q7_INTERRUPT_CONTROL_STATUS — Offset EECh

This register contains the interrupt enable and status bits for the queue 7 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Receive Queue Overflow Interrupt Enable (RXOIE):** When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	**Reserved**
16	0h RW	**Receive Queue Overflow Interrupt Status (RXOVFIS):** This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	**Reserved**
9	0h RW	**Average Bits Per Slot Interrupt Enable (ABPSIE):** When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	**Transmit Queue Underflow Interrupt Enable (TXUIE):** When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW	**Average Bits Per Slot Interrupt Status (ABPSIS):** When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	**Transmit Queue Underflow Interrupt Status (TXUNFIS):** This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

10.2.472 MTL_RXQ7_OPERATION_MODE — Offset EF0h

The Queue 7 Receive Operation Mode register establishes the Receive queue operating modes and command.

The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + EF0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:20	00h RW	**Receive Queue Size (RQS):** This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
19:14	00h RW	**Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD):** These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:8	00h RW	**Threshold for Activating Flow Control (in half-duplex and full-duplex (RFA):** These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.
7	0h RW	**Enable Hardware Flow Control (EHFC):** When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. 0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.
6	0h RW	**Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF):** When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Receive Queue Store and Forward (RSF):** When this bit is set, the GbE Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.
4	0h RW	**Forward Error Packets (FEP):** When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA. 0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.
3	0h RW	**Forward Undersized Good Packets (FUP):** When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.
2	0h RO	**Reserved**
1:0	0h RW	**Receive Queue Threshold Control (RTC):** These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.

10.2.473 MTL_RXQ7_MISSED_PACKET_OVERFLOW_CNT — Offset EF4h

The Queue 7 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EF4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**Missed Packet Counter Overflow Bit (MISCNTOVF):** When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO	**Missed Packet Counter (MISPKTCNT):** This field indicates the number of packets missed by the GbE Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	**Reserved**
11	0h RO	**Overflow Counter Overflow Bit (OVFCNTOVF):** When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO	**Overflow Packet Counter (OVFPKTCNT):** This field indicates the number of packets discarded by the GbE Controller because of Receive queue overflow. This counter is incremented each time the GbE Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.474 MTL_RXQ7_DEBUG — Offset EF8h

The Queue 7 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EF8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO	**Number of Packets in Receive Queue (PRXQ):** This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/ Min_Packet_Size.
15:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**MTL Rx Queue Fill-Level Status (RXQSTS):** This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty. 0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.
3	0h RO	**Reserved**
2:1	0h RO	**MTL Rx Queue Read Controller State (RRCSTS):** This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO	**MTL Rx Queue Write Controller Active Status (RWCSTS):** When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

10.2.475 MTL_RXQ7_CONTROL — Offset EFCh

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EFCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**Receive Queue Packet Arbitration (RXQ_FRM_ARBIT):** When this bit is set, the GbE Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the GbE Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the GbE Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	**Receive Queue Weight (RXQ_WEGT):** This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

10.2.476 DMA_MODE — Offset 1000h

The Bus Mode register establishes the bus operating modes for the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1000h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:22	0h RW	**Rx DMA's Maximum Number of Descriptors to be fetched in a burst (RNDF):** 0x0 (MODE0): 16 0x1 (MODE1): 8 0x2 (MODE2): 4 0x3 (MODE3): 2
21:20	0h RW	**Tx DMA's Maximum Number of Descriptors to be fetched in a burst (TNDF):** 0x0 (MODE0): 16 0x1 (MODE1): 8 0x2 (MODE2): 4 0x3 (MODE3): 2

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Descriptor Cache Enable (DCHE):** When set enables prefetching of descriptors to the Descriptor Cache. When reset descriptor cache feature is disabled. 0x0 (DISABLE): Descriptor Cache Support is disabled. 0x1 (ENABLE): Descriptor Cache Support is enabled.
18	0h RO	**Reserved**
17:16	0h RW	**Interrupt Mode (INTM):** This field defines the interrupt mode of GbE Controller. The behavior of the following outputs changes depending on the following settings: - sbd_perch_tx_intr_o[] (Transmit Per Channel Interrupt) - sbd_perch_rx_intr_o[] (Receive Per Channel Interrupt) - sbd_intr_o (Common Interrupt) It also changes the behavior of the RI/TI bits in the DMA_CH0_Status. - 00: sbd_perch_* are pulse signals for each TX/RX packet transfer completion events (irrespective of whether corresponding interrupts are enabled) for which IOC bits are enabled in descriptor. sbd_intr_o is also asserted when corresponding interrupts are enabled and cleared only when software clears the corresponding RI/TI status bits. - 01: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. - 10: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. However, the signal is asserted again if the same event occurred again before it was cleared. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. - 11: Reserved 0x0 (MODE0): See above description. 0x1 (MODE1): See above description. 0x2 (MODE2): See above description. 0x3 (RSVD): Reserved.
15:11	0h RO	**Reserved**
10	0h RW	**Reserved**
9	0h RO	**Reserved**
8	0h RW	**Descriptor Posted Write (DSPW):** When this bit is set to 0, the descriptor writes are always non-posted. When this bit is set to 1, the descriptor writes are non-posted only when IOC (Interrupt on completion) is set in last descriptor, otherwise the descriptor writes are always posted. 0x0 (DISABLE): Descriptor Posted Write is disabled. 0x1 (ENABLE): Descriptor Posted Write is enabled.
7:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4:2	0h RW	**Transmit Arbitration Algorithm (TAA):** This field is used to select the arbitration algorithm for the Transmit side when multiple Tx DMAs are selected. 0x0 (FP): Fixed priority (Channel 0 has the lowest priority and the last channel has the highest priority). 0x1 (WSP): Weighted Strict Priority (WSP). 0x2 (WRR): Weighted Round-Robin (WRR). 0x3 (RSVD): Reserved (for 3'b011 to 3'b111).
1	0h RO	**Reserved**
0	0h RW	**Software Reset (SWR):** When this bit is set, the MAC and the DMA controller reset the logic and all internal registers of the DMA, MTL, and MAC. This bit is automatically cleared after the reset operation is complete in all GbE Controller clock domains. Before reprogramming any GbE Controller register, a value of zero should be read in this bit. This bit must be read at least 4 CSR clock cycles after it is written to 1. Note: The reset operation is complete only when all resets in all active clock domains are de-asserted. Therefore, it is essential that all PHY inputs clocks (applicable for the selected PHY interface) are present for software reset completion. The time to complete the software reset operation depends on the frequency of the slowest active clock. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Software Reset is disabled. 0x1 (ENABLE): Software Reset is enabled.

10.2.477 DMA_SYSBUS_MODE — Offset 1004h

The System Bus mode register controls the behavior of the AHB or AXI master. It mainly controls burst splitting and number of outstanding requests.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1004h	01010000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Low Power Interface (LPI) (EN_LPI):** When set to 1, this bit enables the LPI mode supported by the EQOS-AXI configuration and accepts the LPI request from the AXI System Clock controller. When set to 0, this bit disables the LPI mode and always denies the LPI request from the AXI System Clock controller. 0x0 (DISABLE): Low Power Interface (LPI) is disabled. 0x1 (ENABLE): Low Power Interface (LPI) is enabled.
30	0h RW	**Unlock on Magic Packet or Remote Wake-Up Packet (LPI_XIT_PKT):** When set to 1, this bit enables the AXI master to come out of the LPI mode only when the magic packet or remote wake-up packet is received. When set to 0, this bit enables the AXI master to come out of the LPI mode when any packet is received. 0x0 (DISABLE): Unlock on Magic Packet or Remote Wake-Up Packet is disabled. 0x1 (ENABLE): Unlock on Magic Packet or Remote Wake-Up Packet is enabled.
29:28	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
27:24	1h RW	**AXI Maximum Write Outstanding Request Limit (WR_OSR_LMT):** This value limits the maximum outstanding request on the AXI write interface. Maximum outstanding requests = WR_OSR_LMT + 1
23:20	0h RO	**Reserved**
19:16	1h RW	**AXI Maximum Read Outstanding Request Limit (RD_OSR_LMT):** This value limits the maximum outstanding request on the AXI read interface. Maximum outstanding requests = RD_OSR_LMT + 1
15:14	0h RO	**Reserved**
13	0h RW	**1 KB Boundary Crossing Enable for the EQOS-AXI Master (ONEKBBE):** When set, the burst transfers performed by the EQOS-AXI master do not cross 1 KB boundary. When reset, the burst transfers performed by the EQOS-AXI master do not cross 4 KB boundary. 0x0 (DISABLE): 1 KB Boundary Crossing for the EQOS-AXI Master Beats is disabled. 0x1 (ENABLE): 1 KB Boundary Crossing for the EQOS-AXI Master Beats is enabled.
12	0h RW	**Address-Aligned Beats (AAL):** When this bit is set to 1, the EQOS-AXI or EQOS-AHB master performs address-aligned burst transfers on Read and Write channels. 0x0 (DISABLE): Address-Aligned Beats is disabled. 0x1 (ENABLE): Address-Aligned Beats is enabled.
11	0h RW	**Enhanced Address Mode Enable. (EAME):** When this bit is set to 1, the DMA master enables the enhanced address mode (40-bit or 48-bit addressing mode). In this mode, the DMA engine uses either the 40- or 48-bit address, depending on the configuration. 0x0 (DISABLE): Enhanced Address Mode is disabled. 0x1 (ENABLE): Enhanced Address Mode is enabled.
10	0h RW	**Automatic AXI LPI enable (AALE):** When set to 1, enables the AXI master to enter into LPI state when there is no activity in the GbE Controller for number of system clock cycles programmed in the LPIEI field of AXI_LPI_Entry_Interval register. 0x0 (DISABLE): Automatic AXI LPI is disabled. 0x1 (ENABLE): Automatic AXI LPI is enabled.
9:8	0h RO	**Reserved**
7	0h RW	**AXI Burst Length 256 (BLEN256):** When this bit is set to 1, the EQOS-AXI master can select a burst length of 256 on the AXI interface. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 256.
6	0h RW	**AXI Burst Length 128 (BLEN128):** When this bit is set to 1, the EQOS-AXI master can select a burst length of 128 on the AXI interface. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 128.
5	0h RW	**AXI Burst Length 64 (BLEN64):** When this bit is set to 1, the EQOS-AXI master can select a burst length of 64 on the AXI interface. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 64.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**AXI Burst Length 32 (BLEN32):** When this bit is set to 1, the EQOS-AXI master can select a burst length of 32 on the AXI interface. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 32.
3	0h RW	**AXI Burst Length 16 (BLEN16):** When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 16 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 16.
2	0h RW	**AXI Burst Length 8 (BLEN8):** When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 8 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 8.
1	0h RW	**AXI Burst Length 4 (BLEN4):** When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 4 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 4.
0	0h RW	**FB:** Fixed Burst Length When this bit is set to 1, the EQOS-AXI master initiates burst transfers of specified lengths as given below. - Burst transfers of fixed burst lengths as indicated by the BLEN256, BLEN128, BLEN64, BLEN32, BLEN16, BLEN8, or BLEN4 field - Burst transfers of length 1 When this bit is set to 0, the EQOS-AXI master initiates burst transfers that are equal to or less than the maximum allowed burst length programmed in Bits[7:1]. 0x0 (DISABLE): Fixed Burst Length is disabled. 0x1 (ENABLE): Fixed Burst Length is enabled.

10.2.478 DMA_INTERRUPT_STATUS — Offset 1008h

The application reads this Interrupt Status register during interrupt service routine or polling to determine the interrupt status of DMA channels, MTL queues, and the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1008h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RO	**MAC Interrupt Status (MACIS):** This bit indicates an interrupt event in the MAC. To reset this bit to 1'b0, the software must read the corresponding register in the MAC to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): MAC Interrupt Status not detected. 0x1 (ACTIVE): MAC Interrupt Status detected.
16	0h RO	**MTL Interrupt Status (MTLIS):** This bit indicates an interrupt event in the MTL. To reset this bit to 1'b0, the software must read the corresponding register in the MTL to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): MTL Interrupt Status not detected. 0x1 (ACTIVE): MTL Interrupt Status detected.
15:8	0h RO	**Reserved**
7	0h RO	**DMA Channel 7 Interrupt Status (DC7IS):** This bit indicates an interrupt event in DMA Channel 7. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 7 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 7 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 7 Interrupt Status detected.
6	0h RO	**DMA Channel 6 Interrupt Status (DC6IS):** This bit indicates an interrupt event in DMA Channel 6. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 6 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 6 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 6 Interrupt Status detected.
5	0h RO	**DMA Channel 5 Interrupt Status (DC5IS):** This bit indicates an interrupt event in DMA Channel 5. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 5 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 5 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 5 Interrupt Status detected.
4	0h RO	**DMA Channel 4 Interrupt Status (DC4IS):** This bit indicates an interrupt event in DMA Channel 4. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 4 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 4 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 4 Interrupt Status detected.
3	0h RO	**DMA Channel 3 Interrupt Status (DC3IS):** This bit indicates an interrupt event in DMA Channel 3. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 3 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 3 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 3 Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**DMA Channel 2 Interrupt Status (DC2IS):** This bit indicates an interrupt event in DMA Channel 2. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 2 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 2 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 2 Interrupt Status detected.
1	0h RO	**DMA Channel 1 Interrupt Status (DC1IS):** This bit indicates an interrupt event in DMA Channel 1. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 1 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 1 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 1 Interrupt Status detected.
0	0h RO	**DMA Channel 0 Interrupt Status (DC0IS):** This bit indicates an interrupt event in DMA Channel 0. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 0 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 0 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 0 Interrupt Status detected.

10.2.479 DMA_DEBUG_STATUS0 — Offset 100Ch

The Debug Status 0 register gives the Receive and Transmit process status for DMA Channel 0-Channel 2 for debugging purpose.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 100Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**DMA Channel 2 Transmit Process State (TPS2):** This field indicates the Tx DMA FSM state for Channel 2. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
27:24	0h RO	**DMA Channel 2 Receive Process State (RPS2):** This field indicates the Rx DMA FSM state for Channel 2. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
23:20	0h RO	**DMA Channel 1 Transmit Process State (TPS1):** This field indicates the Tx DMA FSM state for Channel 1. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
19:16	0h RO	**DMA Channel 1 Receive Process State (RPS1):** This field indicates the Rx DMA FSM state for Channel 1. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**DMA Channel 0 Transmit Process State (TPS0):** This field indicates the Tx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
11:8	0h RO	**DMA Channel 0 Receive Process State (RPS0):** This field indicates the Rx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
7:2	0h RO	**Reserved**
1	0h RO	**AXI Master Read Channel Status (AXRHSTS):** When high, this bit indicates that the read channel of the AXI master is active, and it is transferring the data. 0x0 (INACTIVE): AXI Master Read Channel Status not detected. 0x1 (ACTIVE): AXI Master Read Channel Status detected.
0	0h RO	**AXI Master Write Channel (AXWHSTS):** When high, this bit indicates that the write channel of the AXI master is active, and it is transferring data. 0x0 (INACTIVE): AXI Master Write Channel or AHB Master Status not detected. 0x1 (ACTIVE): AXI Master Write Channel or AHB Master Status detected.

10.2.480 DMA_DEBUG_STATUS1 — Offset 1010h

The Debug Status1 register gives the Receive and Transmit process status for DMA Channel 3-Channel 6.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1010h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**DMA Channel 6 Transmit Process State (TPS6):** This field indicates the Tx DMA FSM state for Channel 6. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
27:24	0h RO	**DMA Channel 6 Receive Process State (RPS6):** This field indicates the Rx DMA FSM state for Channel 6. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
23:20	0h RO	**DMA Channel 5 Transmit Process State (TPS5):** This field indicates the Tx DMA FSM state for Channel 5. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
19:16	0h RO	**DMA Channel 5 Receive Process State (RPS5):** This field indicates the Rx DMA FSM state for Channel 5. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**DMA Channel 4 Transmit Process State (TPS4):** This field indicates the Tx DMA FSM state for Channel 4. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
11:8	0h RO	**DMA Channel 4 Receive Process State (RPS4):** This field indicates the Rx DMA FSM state for Channel 4. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
7:4	0h RO	**DMA Channel 3 Transmit Process State (TPS3):** This field indicates the Tx DMA FSM state for Channel 3. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
3:0	0h RO	**DMA Channel 3 Receive Process State (RPS3):** This field indicates the Rx DMA FSM state for Channel 3. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).

10.2.481 DMA_DEBUG_STATUS2 — Offset 1014h

The Debug Status Register 2 gives the Receive and Transmit process status for DMA Channel 7.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1014h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:4	0h RO	**DMA Channel 7 Transmit Process State (TPS7):** This field indicates the Tx DMA FSM state for Channel 7. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
3:0	0h RO	**DMA Channel 7 Receive Process State (RPS7):** This field indicates the Rx DMA FSM state for Channel 7. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).

10.2.482 AXI4_TX_AR_ACE_CONTROL — Offset 1020h

This register is used to control the AXI4 Cache Coherency Signals for read transactions by all the Transmit DMA channels. The following signals of the AXI4 interface are driven with different values as programmed

for corresponding type (descriptor, buffer1, buffer2) of access.

- arcache_m_o[3:0]

- ardomain_m_o[1:0]

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1020h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:20	0h RW	**Transmit DMA First Packet Buffer or TSO Header Domain Control (THD):** When TSO is NOT enabled, This field is used to drive ardomain_o[1:0] signal when Transmit DMA is accessing First Buffer of the Packet (First valid buffer with FD being set in the TDES3 of the Descriptor). When TSO is enabled, This field is used to drive ardomain_o[1:0] signal when the Transmit DMA is accessing the TSO Header data.
19:16	0h RW	**Transmit DMA First Packet Buffer or TSO Header Cache Control (THC):** When TSO is NOT enabled, This field is used to drive arcache_o[3:0] signal when Transmit DMA is accessing First Buffer of the Packet (First valid buffer with FD being set in the TDES3 of the Descriptor).. When TSO is enabled, This field is used to drive arcache_o[3:0] signal when the Transmit DMA is accessing the TSO Header data.
15:14	0h RO	**Reserved**
13:12	0h RW	**Transmit DMA Extended Packet Buffer or TSO Payload Domain Control (TED):** When TSO is NOT enabled, This field is used to drive ardomain_o[1:0] signal when Transmit DMA is accessing the extended buffers (when packet is distributed across multiple buffers). When TSO is enabled, This field is used to drive ardomain_o[1:0] signal when the Transmit DMA is accessing the TSO payload data.
11:8	0h RW	**Transmit DMA Extended Packet Buffer or TSO Payload Cache Control (TEC):** When TSO is NOT enabled, This field is used to drive arcache_o[3:0] signal when Transmit DMA is accessing the extended buffers (when packet is distributed across multiple buffers). When TSO is enabled, This field is used to drive arcache_o[3:0] signal when the Transmit DMA is accessing the TSO payload data.
7:6	0h RO	**Reserved**
5:4	0h RW	**Transmit DMA Read Descriptor Domain Control (TDRD):** This field is used to drive ardomain_o[1:0] signal when Transmit DMA engines access the Descriptor.
3:0	0h RW	**Transmit DMA Read Descriptor Cache Control (TDRC):** This field is used to drive arcache_o[3:0] signal when Transmit DMA engines access the Descriptor.

10.2.483 AXI4_RX_AW_ACE_CONTROL — Offset 1024h

This register is used to control the AXI4 Cache Coherency Signals for write transactions by all the Receive DMA channels. The following signals of the AXI4 interface are driven with different values as programmed

for corresponding type (descriptor, buffer1, buffer2) of access.

- awcache_m_o[3:0]

- awdomain_m_o[1:0]

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1024h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Receive DMA Buffer Domain Control (RDD):** This field is used to drive the awdomain_o[1:0] signal when Receive DMA is accessing the Buffer when Header and payload are NOT separated.
27:24	0h RW	**Receive DMA Buffer Cache Control (RDC):** This field is used to drive awcache_o[3:0] signal when Receive DMA is accessing the Buffer when Header and payload are NOT separated.
23:22	0h RO	**Reserved**
21:20	0h RW	**Receive DMA Header Domain Control (RHD):** This field is used to drive awdomain_o[1:0] and signal when Receive DMA is accessing the header Buffer when Header and payload are separated.
19:16	0h RW	**Receive DMA Header Cache Control (RHC):** This field is used to drive awcache_o[3:0] and signal when Receive DMA is accessing the header Buffer when Header and payload are separated.
15:14	0h RO	**Reserved**
13:12	0h RW	**Receive DMA Payload Domain Control (RPD):** This field is used to drive awdomain_o[1:0] signal when Receive DMA is accessing the Payload Buffer when Header and payload are separated.
11:8	0h RW	**Receive DMA Payload Cache Control (RPC):** This field is used to drive awcache_o[3:0] signal when Receive DMA is accessing the Payload Buffer when Header and payload are separated.
7:6	0h RO	**Reserved**
5:4	0h RW	**Receive DMA Write Descriptor Domain Control (RDWD):** This field is used to drive awdomain_o[1:0] signal when Receive DMA accesses the Descriptor.
3:0	0h RW	**Receive DMA Write Descriptor Cache Control (RDWC):** This field is used to drive awcache_o[3:0] signal when Receive DMA accesses the Descriptor.

10.2.484 AXI4_TXRX_AWAR_ACE_CONTROL — Offset 1028h

This register is used to control the AXI4 Cache Coherency Signals for Descriptor write transactions by all the TxDMA channels and Descriptor read transactions by all the RxDMA channels. It also controls the values to be driven on awprot_m_o and arprot_m_o.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1028h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RW	**DMA Write Protection control (WRP):** This field is used to drive awprot_m_o[2:0] signal on the AXI Write Channel.
19	0h RO	**Reserved**
18:16	0h RW	**DMA Read Protection control (RDP):** This field is used to drive arprot_m_o[2:0] signal during all read requests.
15:14	0h RO	**Reserved**
13:12	0h RW	**Receive DMA Read Descriptor Domain control (RDRD):** This field is used to drive ardomain_o[1:0] signal when Receive DMA engines read the Descriptor.
11:8	0h RW	**Receive DMA Read Descriptor Cache control (RDRC):** This field is used to drive arcache_o[3:0] signal when Receive DMA engines read the Descriptor.
7:6	0h RO	**Reserved**
5:4	0h RW	**Transmit DMA Write Descriptor Domain control (TDWD):** This field is used to drive awdomain_o[1:0] signal when Transmit DMA write to the Descriptor.
3:0	0h RW	**Transmit DMA Write Descriptor Cache control (TDWC):** This field is used to drive awcache_o[3:0] signal when Transmit DMA writes to the Descriptor.

10.2.485 AXI_LPI_ENTRY_INTERVAL — Offset 1040h

This register is used to control the AXI LPI entry interval.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1040h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**LPI Entry Interval (LPIEI):** Contains the number of system clock cycles, multiplied by 64, to wait for an activity in the GbE Controller to enter into the AXI low power state 0 indicates 64 clock cycles

10.2.486 DMA_TBS_CTRL0 — Offset 1050h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1050h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Fetch Time Offset (FTOS):** The value in units of 256 nanoseconds, that has to be deducted from the Launch time to compute the Fetch Time. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value.
7	0h RO	**Reserved**
6:4	0h RW	**Fetch GSN Offset (FGOS):** The number GSN slots that must be deducted from the Launch GSN to compute the Fetch GSN. Value valid only when FTOV is set.
3:1	0h RO	**Reserved**
0	0h RW	**Fetch Time Offset Valid (FTOV):** Valid When set indicates the FTOS field is valid. When not set, indicates the Fetch Offset is not valid and the DMA engine can fetch the frames from host memory without any time restrictions. 0x0 (INVALID): Fetch Time Offset is invalid. 0x1 (VALID): Fetch Time Offset is valid.

10.2.487 DMA_TBS_CTRL1 — Offset 1054h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1054h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Fetch Time Offset (FTOS):** The value in units of 256 nanoseconds, that has to be deducted from the Launch time to compute the Fetch Time. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value.
7	0h RO	**Reserved**
6:4	0h RW	**Fetch GSN Offset (FGOS):** The number GSN slots that must be deducted from the Launch GSN to compute the Fetch GSN. Value valid only when FTOV is set.
3:1	0h RO	**Reserved**
0	0h RW	**Fetch Time Offset Valid (FTOV):** Valid When set indicates the FTOS field is valid. When not set, indicates the Fetch Offset is not valid and the DMA engine can fetch the frames from host memory without any time restrictions. 0x0 (INVALID): Fetch Time Offset is invalid. 0x1 (VALID): Fetch Time Offset is valid.

10.2.488 DMA_TBS_CTRL2 — Offset 1058h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1058h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Fetch Time Offset (FTOS):** The value in units of 256 nanoseconds, that has to be deducted from the Launch time to compute the Fetch Time. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value.
7	0h RO	**Reserved**
6:4	0h RW	**Fetch GSN Offset (FGOS):** The number GSN slots that must be deducted from the Launch GSN to compute the Fetch GSN. Value valid only when FTOV is set.
3:1	0h RO	**Reserved**
0	0h RW	**Fetch Time Offset Valid (FTOV):** Valid When set indicates the FTOS field is valid. When not set, indicates the Fetch Offset is not valid and the DMA engine can fetch the frames from host memory without any time restrictions. 0x0 (INVALID): Fetch Time Offset is invalid. 0x1 (VALID): Fetch Time Offset is valid.

10.2.489 DMA_TBS_CTRL3 — Offset 105Ch

Type	Size	Offset	Default
MMIO	32 bit	BAR + 105Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Fetch Time Offset (FTOS):** The value in units of 256 nanoseconds, that has to be deducted from the Launch time to compute the Fetch Time. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value.
7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6:4	0h RW	**Fetch GSN Offset (FGOS):** The number GSN slots that must be deducted from the Launch GSN to compute the Fetch GSN. Value valid only when FTOV is set.
3:1	0h RO	**Reserved**
0	0h RW	**Fetch Time Offset Valid (FTOV):** Valid When set indicates the FTOS field is valid. When not set, indicates the Fetch Offset is not valid and the DMA engine can fetch the frames from host memory without any time restrictions. 0x0 (INVALID): Fetch Time Offset is invalid. 0x1 (VALID): Fetch Time Offset is valid.

10.2.490 DMA_SAFETY_INTERRUPT_STATUS — Offset 1080h

This register indicates summary (whether error occured in DMA/MTL/MAC and correctable/uncorrectable) of the Automotive Safety related error interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1080h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**MAC Safety Uncorrectable Interrupt Status (MCSIS):** Indicates a uncorrectable Safety related Interrupt is set in the MAC module. MAC_DPP_FSM_Interrupt_Status register should be read when this bit is set, to get the cause of the Safety Interrupt in MAC. 0x0 (INACTIVE): MAC Safety Uncorrectable Interrupt Status not detected. 0x1 (ACTIVE): MAC Safety Uncorrectable Interrupt Status detected.
30	0h RO	**Reserved**
29	0h RO	**MTL Safety Uncorrectable error Interrupt Status (MSUIS):** This bit indicates an uncorrectable error interrupt event in MTL. To get exact cause of the interrupt the software should read the MTL_Safety_Interrupt_Status register. 0x0 (INACTIVE): MTL Safety Uncorrectable error Interrupt Status not detected. 0x1 (ACTIVE): MTL Safety Uncorrectable error Interrupt Status detected.
28	0h RO	**MTL Safety Correctable error Interrupt Status (MSCIS):** This bit indicates a correctable error interrupt event in MTL. To get exact cause of the interrupt the software should read the MTL_Safety_Interrupt_Status register. 0x0 (INACTIVE): MTL Safety Correctable error Interrupt Status not detected. 0x1 (ACTIVE): MTL Safety Correctable error Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
27:2	0h RO	**Reserved**
1	0h RO	**DMA ECC Uncorrectable error Interrupt Status (DEUIS):** This bit indicates an interrupt event in the DMA ECC safety feature. To get the exact cause of the interrupt the application should read the DMA_ECC_Interrupt_Status register. 0x0 (INACTIVE): DMA ECC Uncorrectable error Interrupt Status not detected. 0x1 (ACTIVE): DMA ECC Uncorrectable error Interrupt Status detected.
0	0h RO	**DMA ECC Correctable error Interrupt Status (DECIS):** This bit indicates an interrupt event in the DMA ECC safety feature. To get the exact cause of the interrupt the application should read the DMA_ECC_Interrupt_Status register. 0x0 (INACTIVE): DMA ECC Correctable error Interrupt Status not detected. 0x1 (ACTIVE): DMA ECC Correctable error Interrupt Status detected.

10.2.491 DMA_ECC_INTERRUPT_ENABLE — Offset 1084h

This register is used to enable the Automotive Safety related TSO memory ECC error interrupt.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1084h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**TSO memory Correctable Error Interrupt Enable (TCEIE):** When set, generates an interrupt when a correctable error is detected at the DMA TSO memory interface. It is indicated in the TCES bit of DMA_ECC_Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): TSO memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): TSO memory Correctable Error Interrupt is enabled.

10.2.492 DMA_ECC_INTERRUPT_STATUS — Offset 1088h

This register indicates the Automotive Safety related TSO memory ECC error interrupt status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1088h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW	**DMA TSO memory Uncorrectable Error status (TUES):** When set, indicates that an uncorrectable error is detected at DMA TSO memory interface. 0x0 (INACTIVE): DMA TSO memory Uncorrectable Error status not detected. 0x1 (ACTIVE): DMA TSO memory Uncorrectable Error status detected.
1	0h RW	**DMA TSO memory Address Mismatch status (TAMS):** This bit when set indicates that address mismatch is found for address bus of DMA TSO memory. 0x0 (INACTIVE): DMA TSO memory Address Mismatch status not detected. 0x1 (ACTIVE): DMA TSO memory Address Mismatch status detected.
0	0h RW	**DMA TSO memory Correctable Error status (TCES):** This bit when set indicates that correctable error is detected at DMA TSO memory interface. 0x0 (INACTIVE): DMA TSO memory Correctable Error status not detected. 0x1 (ACTIVE): DMA TSO memory Correctable Error status detected.

10.2.493 DMA_CH0_CONTROL — Offset 1100h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1100h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Split Headers (SPH):** When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. 0x0 (DISABLE): Split Headers feature is disabled. 0x1 (ENABLE): Split Headers feature is enabled.
23:21	0h RO	**Reserved**
20:18	0h RW	**Descriptor Skip Length (DSL):** This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**Reserved**
16	0h RW	**8xPBL mode (PBLX8):** When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:14	0h RO	**Reserved**
13:0	0000h RW	**Maximum Segment Size (MSS):** This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH0_Tx_Control register is set. The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more.

10.2.494 DMA_CH0_TX_CONTROL — Offset 1104h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1104h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:29	0h RW	**Time Select (TFSEL):** Select bits for one of the four DMA_TBS_CTRL register fields (FTOS, FGSN, FTOV) for the channel. 0x0: DMA_TBS_CTRL0 selected. 0x1: DMA_TBS_CTRL1 selected. 0x2: DMA_TBS_CTRL2 selected. 0x3: DMA_TBS_CTRL3 selected.
28	0h RW	**Enhanced Descriptor Enable (EDSE):** When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes. 0x0 (DISABLE): Enhanced Descriptor is disabled. 0x1 (ENABLE): Enhanced Descriptor is enabled.
27:24	0h RW	**Transmit QOS. (TQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:16	00h RW	**Transmit Programmable Burst Length (TXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RW	**Ignore PBL Requirement (IPBL):** When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled. 0x1 (ENABLE): Ignore PBL Requirement is enabled.
14:13	0h RW	**TSE_MODE:** TSE Mode - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved 0x0 (TSO_USO): TSO/USO. 0x1 (UFOWC): UFO with Checksum. 0x2 (UFOWOC): UFO without Checksum. 0x3 (RSVD): Reserved.
12	0h RW	**TCP Segmentation Enabled (TSE):** When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/ Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled. 0x1 (ENABLE): TCP Segmentation is enabled.
11:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Operate on Second Packet (OSF):** When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled. 0x1 (ENABLE): Operate on Second Packet enabled.
3:1	0h RW	**Transmit Channel Weight (TCW):** This field indicates the weight assigned to the corresponding Transmit channel. When reset is complete, this field is set to 0 for all channels by default, resulting in equal weights to all channels.
0	0h RW	**Start or Stop Transmission Command (ST):** When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command. 0x1 (START): Start Transmission Command.

10.2.495 DMA_CH0_RX_CONTROL — Offset 1108h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1108h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Rx Packet Flush. (RPF):** When this bit is set to 1, then GbE Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the GbE Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled. 0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	**Reserved**
27:24	0h RW	**Rx AXI4 QOS. (RQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Receive Programmable Burst Length (RXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:4	000h RW	**Receive Buffer size High (RBSZ_13_Y):** RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO	**Receive Buffer size Low (RBSZ_X_0):** RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	**Start or Stop Receive (SR):** When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.

10.2.496 DMA_CH0_TXDESC_LIST_HADDRESS — Offset 1110h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1110h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Transmit List (TDESHA):** This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

10.2.497 DMA_CH0_TXDESC_LIST_ADDRESS — Offset 1114h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1114h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Transmit List (TDESLA):** This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.498 DMA_CH0_RXDESC_LIST_HADDRESS — Offset 1118h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list.

Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1118h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Receive List (RDESHA):** This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

10.2.499 DMA_CH0_RXDESC_LIST_ADDRESS — Offset 111Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list.

This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 111Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Receive List (RDESLA):** This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.500 DMA_CH0_TXDESC_TAIL_POINTER — Offset 1120h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1120h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Transmit Descriptor Tail Pointer (TDTP):** This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.501 DMA_CH0_RXDESC_TAIL_POINTER — Offset 1128h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1128h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Receive Descriptor Tail Pointer (RDTP):** This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.502 DMA_CH0_TXDESC_RING_LENGTH — Offset 112Ch

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 112Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Transmit Descriptor Ring Length (TDRL):** This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

10.2.503 DMA_CH0_RXDESC_RING_LENGTH — Offset 1130h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1130h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Receive Descriptor Ring Length (RDRL):** This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

10.2.504 DMA_CH0_INTERRUPT_ENABLE — Offset 1134h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1134h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Normal Interrupt Summary Enable (NIE):** When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.
14	0h RW	**Abnormal Interrupt Summary Enable (AIE):** When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.
13	0h RW	**Context Descriptor Error Enable (CDEE):** When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.
12	0h RW	**Fatal Bus Error Enable (FBEE):** When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.
11	0h RW	**Early Receive Interrupt Enable (ERIE):** When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.
10	0h RW	**Early Transmit Interrupt Enable (ETIE):** When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled. 0x1 (ENABLE): Early Transmit Interrupt is enabled.
9	0h RW	**Receive Watchdog Timeout Enable (RWTE):** When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Receive Stopped Enable (RSE):** When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	**Receive Buffer Unavailable Enable (RBUE):** When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	**Receive Interrupt Enable (RIE):** When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:3	0h RO	**Reserved**
2	0h RW	**Transmit Buffer Unavailable Enable (TBUE):** When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled. 0x1 (ENABLE): Transmit Buffer Unavailable is enabled.
1	0h RW	**Transmit Stopped Enable (TXSE):** When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled. 0x1 (ENABLE): Transmit Stopped is enabled.
0	0h RW	**Transmit Interrupt Enable (TIE):** When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled. 0x1 (ENABLE): Transmit Interrupt is enabled.

10.2.505 DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER — Offset 1138h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1138h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RW	**Receive Interrupt Watchdog Timer Count Units (RWTU):** This fields indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	**Reserved**
7:0	00h RW	**Receive Interrupt Watchdog Timer Count (RWT):** This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

10.2.506 DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS — Offset 113Ch

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 113Ch	000007C0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**Reference Slot Number (RSN):** This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	07Ch RW	**Slot Interval Value (SIV):** This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Advance Slot Check (ASC):** When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set. 0x0 (DISABLE): Advance Slot Check is disabled. 0x1 (ENABLE): Advance Slot Check is enabled.
0	0h RW	**Enable Slot Comparison (ESC):** When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is - equal to the reference slot number or - ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets. 0x0 (DISABLE): Slot Comparison is disabled. 0x1 (ENABLE): Slot Comparison is enabled.

10.2.507 DMA_CH0_CURRENT_APP_TXDESC — Offset 1144h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1144h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Descriptor Address Pointer (CURTDESAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.508 DMA_CH0_CURRENT_APP_RXDESC — Offset 114Ch

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 114Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Descriptor Address Pointer (CURRDESAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.509 DMA_CH0_CURRENT_APP_TXBUFFER_H — Offset 1150h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1150h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTRH):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.510 DMA_CH0_CURRENT_APP_TXBUFFER — Offset 1154h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1154h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.511 DMA_CH0_CURRENT_APP_RXBUFFER_H — Offset 1158h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1158h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTRH):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.512 DMA_CH0_CURRENT_APP_RXBUFFER — Offset 115Ch

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 115Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.513 DMA_CH0_STATUS — Offset 1160h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1160h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:19	0h RO	**Rx DMA Error Bits (REB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	0h RO	**Tx DMA Error Bits (TEB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	0h RW	**Normal Interrupt Summary (NIS):** Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected. 0x1 (ACTIVE): Normal Interrupt Summary status detected.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Abnormal Interrupt Summary (AIS):** Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected. 0x1 (ACTIVE): Abnormal Interrupt Summary status detected.
13	0h RW	**Context Descriptor Error (CDE):** This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected. 0x1 (ACTIVE): Context Descriptor Error status detected.
12	0h RW	**Fatal Bus Error (FBE):** This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected. 0x1 (ACTIVE): Fatal Bus Error status detected.
11	0h RW	**Early Receive Interrupt (ERI):** This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected. 0x1 (ACTIVE): Early Receive Interrupt status detected.
10	0h RW	**Early Transmit Interrupt (ETI):** This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected. 0x1 (ACTIVE): Early Transmit Interrupt status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Receive Watchdog Timeout (RWT):** This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected. 0x1 (ACTIVE): Receive Watchdog Timeout status detected.
8	0h RW	**Receive Process Stopped (RPS):** This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected. 0x1 (ACTIVE): Receive Process Stopped status detected.
7	0h RW	**Receive Buffer Unavailable (RBU):** This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected. 0x1 (ACTIVE): Receive Buffer Unavailable status detected.
6	0h RW	**Receive Interrupt (RI):** This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected. 0x1 (ACTIVE): Receive Interrupt status detected.
5:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Transmit Buffer Unavailable (TBU):** This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected. 0x1 (ACTIVE): Transmit Buffer Unavailable status detected.
1	0h RW	**Transmit Process Stopped (TPS):** This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected. 0x1 (ACTIVE): Transmit Process Stopped status detected.
0	0h RW	**Transmit Interrupt (TI):** This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected. 0x1 (ACTIVE): Transmit Interrupt status detected.

10.2.514 DMA_CH0_MISS_FRAME_CNT — Offset 1164h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1164h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Overflow status of the MFC Counter (MFCO):** When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred. 0x1 (ACTIVE): Miss Frame Counter overflow occurred.
14:11	0h RO	**Reserved**
10:0	000h RO	**Dropped Packet Counters (MFC):** This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.515 DMA_CH0_RXP_ACCEPT_CNT — Offset 1168h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1168h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Accept Counter Overflow Bit (RXPACOF):** When set, this bit indicates that the RXPAC Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Accept Counter overflow not occurred. 0x1 (ACTIVE): Rx Parser Accept Counter overflow occurred.
30:0	00000000h RO	**Rx Parser Accept Counter (RXPAC):** This 31-bit counter is implemented whenever a Rx Parser Accept a packet due to AF =1. The counter is cleared when the register is read.

10.2.516 DMA_CH0_RX_ERI_CNT — Offset 116Ch

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 116Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RO	**ERI Counter (ECNT):** When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

10.2.517 DMA_CH1_CONTROL — Offset 1180h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1180h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Split Headers (SPH):** When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. 0x0 (DISABLE): Split Headers feature is disabled. 0x1 (ENABLE): Split Headers feature is enabled.
23:21	0h RO	**Reserved**
20:18	0h RW	**Descriptor Skip Length (DSL):** This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**8xPBL mode (PBLX8):** When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:14	0h RO	**Reserved**
13:0	0000h RW	**Maximum Segment Size (MSS):** This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH0_Tx_Control register is set. The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more.

10.2.518 DMA_CH1_TX_CONTROL — Offset 1184h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1184h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:29	0h RW	**Time Select (TFSEL):** Select bits for one of the four DMA_TBS_CTRL register fields (FTOS, FGSN, FTOV) for the channel. 0x0: DMA_TBS_CTRL0 selected. 0x1: DMA_TBS_CTRL1 selected. 0x2: DMA_TBS_CTRL2 selected. 0x3: DMA_TBS_CTRL3 selected.
28	0h RW	**Enhanced Descriptor Enable (EDSE):** When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes. 0x0 (DISABLE): Enhanced Descriptor is disabled. 0x1 (ENABLE): Enhanced Descriptor is enabled.
27:24	0h RW	**Transmit QOS. (TQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:16	00h RW	**Transmit Programmable Burst Length (TXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RW	**Ignore PBL Requirement (IPBL):** When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled. 0x1 (ENABLE): Ignore PBL Requirement is enabled.
14:13	0h RW	**TSE_MODE:** TSE Mode - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved 0x0 (TSO_USO): TSO/USO. 0x1 (UFOWC): UFO with Checksum. 0x2 (UFOWOC): UFO without Checksum. 0x3 (RSVD): Reserved.
12	0h RW	**TCP Segmentation Enabled (TSE):** When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/ Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled. 0x1 (ENABLE): TCP Segmentation is enabled.
11:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Operate on Second Packet (OSF):** When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled. 0x1 (ENABLE): Operate on Second Packet enabled.
3:1	0h RW	**Transmit Channel Weight (TCW):** This field indicates the weight assigned to the corresponding Transmit channel. When reset is complete, this field is set to 0 for all channels by default, resulting in equal weights to all channels.
0	0h RW	**Start or Stop Transmission Command (ST):** When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command. 0x1 (START): Start Transmission Command.

10.2.519 DMA_CH1_RX_CONTROL — Offset 1188h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1188h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Rx Packet Flush. (RPF):** When this bit is set to 1, then GbE Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the GbE Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled. 0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	**Reserved**
27:24	0h RW	**Rx AXI4 QOS. (RQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Receive Programmable Burst Length (RXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:4	000h RW	**Receive Buffer size High (RBSZ_13_Y):** RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO	**Receive Buffer size Low (RBSZ_X_0):** RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	**Start or Stop Receive (SR):** When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.

10.2.520 DMA_CH1_TXDESC_LIST_HADDRESS — Offset 1190h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1190h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Transmit List (TDESHA):** This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

10.2.521 DMA_CH1_TXDESC_LIST_ADDRESS — Offset 1194h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1194h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Transmit List (TDESLA):** This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.522 DMA_CH1_RXDESC_LIST_HADDRESS — Offset 1198h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list.

Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1198h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Receive List (RDESHA):** This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

10.2.523 DMA_CH1_RXDESC_LIST_ADDRESS — Offset 119Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list.

This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 119Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Receive List (RDESLA):** This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.524 DMA_CH1_TXDESC_TAIL_POINTER — Offset 11A0h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Transmit Descriptor Tail Pointer (TDTP):** This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.525 DMA_CH1_RXDESC_TAIL_POINTER — Offset 11A8h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Receive Descriptor Tail Pointer (RDTP):** This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.526 DMA_CH1_TXDESC_RING_LENGTH — Offset 11ACh

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Transmit Descriptor Ring Length (TDRL):** This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

10.2.527 DMA_CH1_RXDESC_RING_LENGTH — Offset 11B0h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Receive Descriptor Ring Length (RDRL):** This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

10.2.528 DMA_CH1_INTERRUPT_ENABLE — Offset 11B4h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Normal Interrupt Summary Enable (NIE):** When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.
14	0h RW	**Abnormal Interrupt Summary Enable (AIE):** When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.
13	0h RW	**Context Descriptor Error Enable (CDEE):** When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.
12	0h RW	**Fatal Bus Error Enable (FBEE):** When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.
11	0h RW	**Early Receive Interrupt Enable (ERIE):** When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.
10	0h RW	**Early Transmit Interrupt Enable (ETIE):** When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled. 0x1 (ENABLE): Early Transmit Interrupt is enabled.
9	0h RW	**Receive Watchdog Timeout Enable (RWTE):** When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Receive Stopped Enable (RSE):** When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	**Receive Buffer Unavailable Enable (RBUE):** When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	**Receive Interrupt Enable (RIE):** When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:3	0h RO	**Reserved**
2	0h RW	**Transmit Buffer Unavailable Enable (TBUE):** When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled. 0x1 (ENABLE): Transmit Buffer Unavailable is enabled.
1	0h RW	**Transmit Stopped Enable (TXSE):** When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled. 0x1 (ENABLE): Transmit Stopped is enabled.
0	0h RW	**Transmit Interrupt Enable (TIE):** When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled. 0x1 (ENABLE): Transmit Interrupt is enabled.

10.2.529 DMA_CH1_RX_INTERRUPT_WATCHDOG_TIMER — Offset 11B8h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RW	**Receive Interrupt Watchdog Timer Count Units (RWTU):** This fields indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	**Reserved**
7:0	00h RW	**Receive Interrupt Watchdog Timer Count (RWT):** This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

10.2.530 DMA_CH1_SLOT_FUNCTION_CONTROL_STATUS — Offset 11BCh

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11BCh	000007C0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**Reference Slot Number (RSN):** This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	07Ch RW	**Slot Interval Value (SIV):** This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Advance Slot Check (ASC):** When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set. 0x0 (DISABLE): Advance Slot Check is disabled. 0x1 (ENABLE): Advance Slot Check is enabled.
0	0h RW	**Enable Slot Comparison (ESC):** When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is - equal to the reference slot number or - ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets. 0x0 (DISABLE): Slot Comparison is disabled. 0x1 (ENABLE): Slot Comparison is enabled.

10.2.531 DMA_CH1_CURRENT_APP_TXDESC — Offset 11C4h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Descriptor Address Pointer (CURTDESAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.532 DMA_CH1_CURRENT_APP_RXDESC — Offset 11CCh

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Descriptor Address Pointer (CURRDESAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.533 DMA_CH1_CURRENT_APP_TXBUFFER_H — Offset 11D0h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTRH):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.534 DMA_CH1_CURRENT_APP_TXBUFFER — Offset 11D4h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.535 DMA_CH1_CURRENT_APP_RXBUFFER_H — Offset 11D8h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTRH):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.536 DMA_CH1_CURRENT_APP_RXBUFFER — Offset 11DCh

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.537 DMA_CH1_STATUS — Offset 11E0h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:19	0h RO	**Rx DMA Error Bits (REB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	0h RO	**Tx DMA Error Bits (TEB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	0h RW	**Normal Interrupt Summary (NIS):** Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected. 0x1 (ACTIVE): Normal Interrupt Summary status detected.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Abnormal Interrupt Summary (AIS):** Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected. 0x1 (ACTIVE): Abnormal Interrupt Summary status detected.
13	0h RW	**Context Descriptor Error (CDE):** This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected. 0x1 (ACTIVE): Context Descriptor Error status detected.
12	0h RW	**Fatal Bus Error (FBE):** This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected. 0x1 (ACTIVE): Fatal Bus Error status detected.
11	0h RW	**Early Receive Interrupt (ERI):** This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected. 0x1 (ACTIVE): Early Receive Interrupt status detected.
10	0h RW	**Early Transmit Interrupt (ETI):** This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected. 0x1 (ACTIVE): Early Transmit Interrupt status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Receive Watchdog Timeout (RWT):** This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected. 0x1 (ACTIVE): Receive Watchdog Timeout status detected.
8	0h RW	**Receive Process Stopped (RPS):** This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected. 0x1 (ACTIVE): Receive Process Stopped status detected.
7	0h RW	**Receive Buffer Unavailable (RBU):** This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected. 0x1 (ACTIVE): Receive Buffer Unavailable status detected.
6	0h RW	**Receive Interrupt (RI):** This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected. 0x1 (ACTIVE): Receive Interrupt status detected.
5:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Transmit Buffer Unavailable (TBU):** This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected. 0x1 (ACTIVE): Transmit Buffer Unavailable status detected.
1	0h RW	**Transmit Process Stopped (TPS):** This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected. 0x1 (ACTIVE): Transmit Process Stopped status detected.
0	0h RW	**Transmit Interrupt (TI):** This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected. 0x1 (ACTIVE): Transmit Interrupt status detected.

10.2.538 DMA_CH1_MISS_FRAME_CNT — Offset 11E4h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Overflow status of the MFC Counter (MFCO):** When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred. 0x1 (ACTIVE): Miss Frame Counter overflow occurred.
14:11	0h RO	**Reserved**
10:0	000h RO	**Dropped Packet Counters (MFC):** This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.539 DMA_CH1_RXP_ACCEPT_CNT — Offset 11E8h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Accept Counter Overflow Bit (RXPACOF):** When set, this bit indicates that the RXPAC Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Accept Counter overflow not occurred. 0x1 (ACTIVE): Rx Parser Accept Counter overflow occurred.
30:0	00000000h RO	**Rx Parser Accept Counter (RXPAC):** This 31-bit counter is implemented whenever a Rx Parser Accept a packet due to AF =1. The counter is cleared when the register is read.

10.2.540 DMA_CH1_RX_ERI_CNT — Offset 11ECh

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RO	**ERI Counter (ECNT):** When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

10.2.541 DMA_CH2_CONTROL — Offset 1200h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1200h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Split Headers (SPH):** When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. 0x0 (DISABLE): Split Headers feature is disabled. 0x1 (ENABLE): Split Headers feature is enabled.
23:21	0h RO	**Reserved**
20:18	0h RW	**Descriptor Skip Length (DSL):** This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**8xPBL mode (PBLX8):** When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:14	0h RO	**Reserved**
13:0	0000h RW	**Maximum Segment Size (MSS):** This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH0_Tx_Control register is set. The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more.

10.2.542 DMA_CH2_TX_CONTROL — Offset 1204h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1204h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:29	0h RW	**Time Select (TFSEL):** Select bits for one of the four DMA_TBS_CTRL register fields (FTOS, FGSN, FTOV) for the channel. 0x0: DMA_TBS_CTRL0 selected. 0x1: DMA_TBS_CTRL1 selected. 0x2: DMA_TBS_CTRL2 selected. 0x3: DMA_TBS_CTRL3 selected.
28	0h RW	**Enhanced Descriptor Enable (EDSE):** When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes. 0x0 (DISABLE): Enhanced Descriptor is disabled. 0x1 (ENABLE): Enhanced Descriptor is enabled.
27:24	0h RW	**Transmit QOS. (TQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:16	00h RW	**Transmit Programmable Burst Length (TXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RW	**Ignore PBL Requirement (IPBL):** When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled. 0x1 (ENABLE): Ignore PBL Requirement is enabled.
14:13	0h RW	**TSE_MODE:** TSE Mode - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved 0x0 (TSO_USO): TSO/USO. 0x1 (UFOWC): UFO with Checksum. 0x2 (UFOWOC): UFO without Checksum. 0x3 (RSVD): Reserved.
12	0h RW	**TCP Segmentation Enabled (TSE):** When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/ Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled. 0x1 (ENABLE): TCP Segmentation is enabled.
11:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Operate on Second Packet (OSF):** When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled. 0x1 (ENABLE): Operate on Second Packet enabled.
3:1	0h RW	**Transmit Channel Weight (TCW):** This field indicates the weight assigned to the corresponding Transmit channel. When reset is complete, this field is set to 0 for all channels by default, resulting in equal weights to all channels.
0	0h RW	**Start or Stop Transmission Command (ST):** When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command. 0x1 (START): Start Transmission Command.

10.2.543 DMA_CH2_RX_CONTROL — Offset 1208h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1208h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Rx Packet Flush. (RPF):** When this bit is set to 1, then GbE Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the GbE Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled. 0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	**Reserved**
27:24	0h RW	**Rx AXI4 QOS. (RQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Receive Programmable Burst Length (RXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:4	000h RW	**Receive Buffer size High (RBSZ_13_Y):** RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO	**Receive Buffer size Low (RBSZ_X_0):** RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	**Start or Stop Receive (SR):** When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.

10.2.544 DMA_CH2_TXDESC_LIST_HADDRESS — Offset 1210h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1210h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Transmit List (TDESHA):** This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

10.2.545 DMA_CH2_TXDESC_LIST_ADDRESS — Offset 1214h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1214h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Transmit List (TDESLA):** This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.546 DMA_CH2_RXDESC_LIST_HADDRESS — Offset 1218h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list.

Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1218h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Receive List (RDESHA):** This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

10.2.547 DMA_CH2_RXDESC_LIST_ADDRESS — Offset 121Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list.

This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 121Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Receive List (RDESLA):** This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.548 DMA_CH2_TXDESC_TAIL_POINTER — Offset 1220h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1220h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Transmit Descriptor Tail Pointer (TDTP):** This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.549 DMA_CH2_RXDESC_TAIL_POINTER — Offset 1228h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1228h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Receive Descriptor Tail Pointer (RDTP):** This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.550 DMA_CH2_TXDESC_RING_LENGTH — Offset 122Ch

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 122Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Transmit Descriptor Ring Length (TDRL):** This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

10.2.551 DMA_CH2_RXDESC_RING_LENGTH — Offset 1230h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1230h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Receive Descriptor Ring Length (RDRL):** This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

10.2.552 DMA_CH2_INTERRUPT_ENABLE — Offset 1234h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1234h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Normal Interrupt Summary Enable (NIE):** When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.
14	0h RW	**Abnormal Interrupt Summary Enable (AIE):** When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.
13	0h RW	**Context Descriptor Error Enable (CDEE):** When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.
12	0h RW	**Fatal Bus Error Enable (FBEE):** When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.
11	0h RW	**Early Receive Interrupt Enable (ERIE):** When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.
10	0h RW	**Early Transmit Interrupt Enable (ETIE):** When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled. 0x1 (ENABLE): Early Transmit Interrupt is enabled.
9	0h RW	**Receive Watchdog Timeout Enable (RWTE):** When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Receive Stopped Enable (RSE):** When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	**Receive Buffer Unavailable Enable (RBUE):** When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	**Receive Interrupt Enable (RIE):** When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:3	0h RO	**Reserved**
2	0h RW	**Transmit Buffer Unavailable Enable (TBUE):** When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled. 0x1 (ENABLE): Transmit Buffer Unavailable is enabled.
1	0h RW	**Transmit Stopped Enable (TXSE):** When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled. 0x1 (ENABLE): Transmit Stopped is enabled.
0	0h RW	**Transmit Interrupt Enable (TIE):** When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled. 0x1 (ENABLE): Transmit Interrupt is enabled.

10.2.553 DMA_CH2_RX_INTERRUPT_WATCHDOG_TIMER — Offset 1238h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1238h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RW	**Receive Interrupt Watchdog Timer Count Units (RWTU):** This fields indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	**Reserved**
7:0	00h RW	**Receive Interrupt Watchdog Timer Count (RWT):** This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

10.2.554 DMA_CH2_SLOT_FUNCTION_CONTROL_STATUS — Offset 123Ch

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 123Ch	000007C0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**Reference Slot Number (RSN):** This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	07Ch RW	**Slot Interval Value (SIV):** This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Advance Slot Check (ASC):** When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set. 0x0 (DISABLE): Advance Slot Check is disabled. 0x1 (ENABLE): Advance Slot Check is enabled.
0	0h RW	**Enable Slot Comparison (ESC):** When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is - equal to the reference slot number or - ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets. 0x0 (DISABLE): Slot Comparison is disabled. 0x1 (ENABLE): Slot Comparison is enabled.

10.2.555 DMA_CH2_CURRENT_APP_TXDESC — Offset 1244h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1244h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Descriptor Address Pointer (CURTDESAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.556 DMA_CH2_CURRENT_APP_RXDESC — Offset 124Ch

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 124Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Descriptor Address Pointer (CURRDESAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.557 DMA_CH2_CURRENT_APP_TXBUFFER_H — Offset 1250h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1250h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTRH):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.558 DMA_CH2_CURRENT_APP_TXBUFFER — Offset 1254h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1254h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.559 DMA_CH2_CURRENT_APP_RXBUFFER_H — Offset 1258h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1258h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTRH):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.560 DMA_CH2_CURRENT_APP_RXBUFFER — Offset 125Ch

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 125Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.561 DMA_CH2_STATUS — Offset 1260h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1260h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:19	0h RO	**Rx DMA Error Bits (REB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	0h RO	**Tx DMA Error Bits (TEB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	0h RW	**Normal Interrupt Summary (NIS):** Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected. 0x1 (ACTIVE): Normal Interrupt Summary status detected.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Abnormal Interrupt Summary (AIS):** Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected. 0x1 (ACTIVE): Abnormal Interrupt Summary status detected.
13	0h RW	**Context Descriptor Error (CDE):** This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected. 0x1 (ACTIVE): Context Descriptor Error status detected.
12	0h RW	**Fatal Bus Error (FBE):** This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected. 0x1 (ACTIVE): Fatal Bus Error status detected.
11	0h RW	**Early Receive Interrupt (ERI):** This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected. 0x1 (ACTIVE): Early Receive Interrupt status detected.
10	0h RW	**Early Transmit Interrupt (ETI):** This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected. 0x1 (ACTIVE): Early Transmit Interrupt status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Receive Watchdog Timeout (RWT):** This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected. 0x1 (ACTIVE): Receive Watchdog Timeout status detected.
8	0h RW	**Receive Process Stopped (RPS):** This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected. 0x1 (ACTIVE): Receive Process Stopped status detected.
7	0h RW	**Receive Buffer Unavailable (RBU):** This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected. 0x1 (ACTIVE): Receive Buffer Unavailable status detected.
6	0h RW	**Receive Interrupt (RI):** This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected. 0x1 (ACTIVE): Receive Interrupt status detected.
5:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Transmit Buffer Unavailable (TBU):** This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected. 0x1 (ACTIVE): Transmit Buffer Unavailable status detected.
1	0h RW	**Transmit Process Stopped (TPS):** This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected. 0x1 (ACTIVE): Transmit Process Stopped status detected.
0	0h RW	**Transmit Interrupt (TI):** This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected. 0x1 (ACTIVE): Transmit Interrupt status detected.

10.2.562 DMA_CH2_MISS_FRAME_CNT — Offset 1264h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1264h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Overflow status of the MFC Counter (MFCO):** When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred. 0x1 (ACTIVE): Miss Frame Counter overflow occurred.
14:11	0h RO	**Reserved**
10:0	000h RO	**Dropped Packet Counters (MFC):** This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.563 DMA_CH2_RXP_ACCEPT_CNT — Offset 1268h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1268h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Accept Counter Overflow Bit (RXPACOF):** When set, this bit indicates that the RXPAC Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Accept Counter overflow not occurred. 0x1 (ACTIVE): Rx Parser Accept Counter overflow occurred.
30:0	00000000h RO	**Rx Parser Accept Counter (RXPAC):** This 31-bit counter is implemented whenever a Rx Parser Accept a packet due to AF =1. The counter is cleared when the register is read.

10.2.564 DMA_CH2_RX_ERI_CNT — Offset 126Ch

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 126Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RO	**ERI Counter (ECNT):** When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

10.2.565 DMA_CH3_CONTROL — Offset 1280h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1280h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Split Headers (SPH):** When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. 0x0 (DISABLE): Split Headers feature is disabled. 0x1 (ENABLE): Split Headers feature is enabled.
23:21	0h RO	**Reserved**
20:18	0h RW	**Descriptor Skip Length (DSL):** This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**8xPBL mode (PBLX8):** When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:14	0h RO	**Reserved**
13:0	0000h RW	**Maximum Segment Size (MSS):** This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH0_Tx_Control register is set. The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more.

10.2.566 DMA_CH3_TX_CONTROL — Offset 1284h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1284h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:29	0h RW	**Time Select (TFSEL):** Select bits for one of the four DMA_TBS_CTRL register fields (FTOS, FGSN, FTOV) for the channel. 0x0: DMA_TBS_CTRL0 selected. 0x1: DMA_TBS_CTRL1 selected. 0x2: DMA_TBS_CTRL2 selected. 0x3: DMA_TBS_CTRL3 selected.
28	0h RW	**Enhanced Descriptor Enable (EDSE):** When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes. 0x0 (DISABLE): Enhanced Descriptor is disabled. 0x1 (ENABLE): Enhanced Descriptor is enabled.
27:24	0h RW	**Transmit QOS. (TQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:16	00h RW	**Transmit Programmable Burst Length (TXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RW	**Ignore PBL Requirement (IPBL):** When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled. 0x1 (ENABLE): Ignore PBL Requirement is enabled.
14:13	0h RW	**TSE_MODE:** TSE Mode - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved 0x0 (TSO_USO): TSO/USO. 0x1 (UFOWC): UFO with Checksum. 0x2 (UFOWOC): UFO without Checksum. 0x3 (RSVD): Reserved.
12	0h RW	**TCP Segmentation Enabled (TSE):** When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/ Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled. 0x1 (ENABLE): TCP Segmentation is enabled.
11:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Operate on Second Packet (OSF):** When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled. 0x1 (ENABLE): Operate on Second Packet enabled.
3:1	0h RW	**Transmit Channel Weight (TCW):** This field indicates the weight assigned to the corresponding Transmit channel. When reset is complete, this field is set to 0 for all channels by default, resulting in equal weights to all channels.
0	0h RW	**Start or Stop Transmission Command (ST):** When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command. 0x1 (START): Start Transmission Command.

10.2.567 DMA_CH3_RX_CONTROL — Offset 1288h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1288h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Rx Packet Flush. (RPF):** When this bit is set to 1, then GbE Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the GbE Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled. 0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	**Reserved**
27:24	0h RW	**Rx AXI4 QOS. (RQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Receive Programmable Burst Length (RXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:4	000h RW	**Receive Buffer size High (RBSZ_13_Y):** RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO	**Receive Buffer size Low (RBSZ_X_0):** RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	**Start or Stop Receive (SR):** When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.

10.2.568 DMA_CH3_TXDESC_LIST_HADDRESS — Offset 1290h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1290h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Transmit List (TDESHA):** This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

10.2.569 DMA_CH3_TXDESC_LIST_ADDRESS — Offset 1294h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1294h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Transmit List (TDESLA):** This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.570 DMA_CH3_RXDESC_LIST_HADDRESS — Offset 1298h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list.

Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1298h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Receive List (RDESHA):** This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

10.2.571 DMA_CH3_RXDESC_LIST_ADDRESS — Offset 129Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list.

This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 129Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Receive List (RDESLA):** This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.572 DMA_CH3_TXDESC_TAIL_POINTER — Offset 12A0h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Transmit Descriptor Tail Pointer (TDTP):** This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.573 DMA_CH3_RXDESC_TAIL_POINTER — Offset 12A8h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Receive Descriptor Tail Pointer (RDTP):** This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.574 DMA_CH3_TXDESC_RING_LENGTH — Offset 12ACh

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Transmit Descriptor Ring Length (TDRL):** This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

10.2.575 DMA_CH3_RXDESC_RING_LENGTH — Offset 12B0h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Receive Descriptor Ring Length (RDRL):** This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

10.2.576 DMA_CH3_INTERRUPT_ENABLE — Offset 12B4h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Normal Interrupt Summary Enable (NIE):** When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.
14	0h RW	**Abnormal Interrupt Summary Enable (AIE):** When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.
13	0h RW	**Context Descriptor Error Enable (CDEE):** When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.
12	0h RW	**Fatal Bus Error Enable (FBEE):** When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.
11	0h RW	**Early Receive Interrupt Enable (ERIE):** When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.
10	0h RW	**Early Transmit Interrupt Enable (ETIE):** When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled. 0x1 (ENABLE): Early Transmit Interrupt is enabled.
9	0h RW	**Receive Watchdog Timeout Enable (RWTE):** When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Receive Stopped Enable (RSE):** When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	**Receive Buffer Unavailable Enable (RBUE):** When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	**Receive Interrupt Enable (RIE):** When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:3	0h RO	**Reserved**
2	0h RW	**Transmit Buffer Unavailable Enable (TBUE):** When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled. 0x1 (ENABLE): Transmit Buffer Unavailable is enabled.
1	0h RW	**Transmit Stopped Enable (TXSE):** When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled. 0x1 (ENABLE): Transmit Stopped is enabled.
0	0h RW	**Transmit Interrupt Enable (TIE):** When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled. 0x1 (ENABLE): Transmit Interrupt is enabled.

10.2.577 DMA_CH3_RX_INTERRUPT_WATCHDOG_TIMER — Offset 12B8h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RW	**Receive Interrupt Watchdog Timer Count Units (RWTU):** This fields indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	**Reserved**
7:0	00h RW	**Receive Interrupt Watchdog Timer Count (RWT):** This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

10.2.578 DMA_CH3_SLOT_FUNCTION_CONTROL_STATUS — Offset 12BCh

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12BCh	000007C0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**Reference Slot Number (RSN):** This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	07Ch RW	**Slot Interval Value (SIV):** This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Advance Slot Check (ASC):** When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set. 0x0 (DISABLE): Advance Slot Check is disabled. 0x1 (ENABLE): Advance Slot Check is enabled.
0	0h RW	**Enable Slot Comparison (ESC):** When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is - equal to the reference slot number or - ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets. 0x0 (DISABLE): Slot Comparison is disabled. 0x1 (ENABLE): Slot Comparison is enabled.

10.2.579 DMA_CH3_CURRENT_APP_TXDESC — Offset 12C4h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Descriptor Address Pointer (CURTDESAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.580 DMA_CH3_CURRENT_APP_RXDESC — Offset 12CCh

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Descriptor Address Pointer (CURRDESAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.581 DMA_CH3_CURRENT_APP_TXBUFFER_H — Offset 12D0h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTRH):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.582 DMA_CH3_CURRENT_APP_TXBUFFER — Offset 12D4h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.583 DMA_CH3_CURRENT_APP_RXBUFFER_H — Offset 12D8h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTRH):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.584 DMA_CH3_CURRENT_APP_RXBUFFER — Offset 12DCh

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.585 DMA_CH3_STATUS — Offset 12E0h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:19	0h RO	**Rx DMA Error Bits (REB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	0h RO	**Tx DMA Error Bits (TEB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	0h RW	**Normal Interrupt Summary (NIS):** Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected. 0x1 (ACTIVE): Normal Interrupt Summary status detected.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Abnormal Interrupt Summary (AIS):** Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected. 0x1 (ACTIVE): Abnormal Interrupt Summary status detected.
13	0h RW	**Context Descriptor Error (CDE):** This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected. 0x1 (ACTIVE): Context Descriptor Error status detected.
12	0h RW	**Fatal Bus Error (FBE):** This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected. 0x1 (ACTIVE): Fatal Bus Error status detected.
11	0h RW	**Early Receive Interrupt (ERI):** This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected. 0x1 (ACTIVE): Early Receive Interrupt status detected.
10	0h RW	**Early Transmit Interrupt (ETI):** This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected. 0x1 (ACTIVE): Early Transmit Interrupt status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Receive Watchdog Timeout (RWT):** This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected. 0x1 (ACTIVE): Receive Watchdog Timeout status detected.
8	0h RW	**Receive Process Stopped (RPS):** This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected. 0x1 (ACTIVE): Receive Process Stopped status detected.
7	0h RW	**Receive Buffer Unavailable (RBU):** This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected. 0x1 (ACTIVE): Receive Buffer Unavailable status detected.
6	0h RW	**Receive Interrupt (RI):** This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected. 0x1 (ACTIVE): Receive Interrupt status detected.
5:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Transmit Buffer Unavailable (TBU):** This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected. 0x1 (ACTIVE): Transmit Buffer Unavailable status detected.
1	0h RW	**Transmit Process Stopped (TPS):** This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected. 0x1 (ACTIVE): Transmit Process Stopped status detected.
0	0h RW	**Transmit Interrupt (TI):** This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected. 0x1 (ACTIVE): Transmit Interrupt status detected.

10.2.586 DMA_CH3_MISS_FRAME_CNT — Offset 12E4h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Overflow status of the MFC Counter (MFCO):** When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred. 0x1 (ACTIVE): Miss Frame Counter overflow occurred.
14:11	0h RO	**Reserved**
10:0	000h RO	**Dropped Packet Counters (MFC):** This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.587 DMA_CH3_RXP_ACCEPT_CNT — Offset 12E8h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Accept Counter Overflow Bit (RXPACOF):** When set, this bit indicates that the RXPAC Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Accept Counter overflow not occurred. 0x1 (ACTIVE): Rx Parser Accept Counter overflow occurred.
30:0	00000000h RO	**Rx Parser Accept Counter (RXPAC):** This 31-bit counter is implemented whenever a Rx Parser Accept a packet due to AF =1. The counter is cleared when the register is read.

10.2.588 DMA_CH3_RX_ERI_CNT — Offset 12ECh

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RO	**ERI Counter (ECNT):** When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

10.2.589 DMA_CH4_CONTROL — Offset 1300h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1300h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Split Headers (SPH):** When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. 0x0 (DISABLE): Split Headers feature is disabled. 0x1 (ENABLE): Split Headers feature is enabled.
23:21	0h RO	**Reserved**
20:18	0h RW	**Descriptor Skip Length (DSL):** This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	**Reserved**
16	0h RW	**8xPBL mode (PBLX8):** When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:0	0h RO	**Reserved**

10.2.590 DMA_CH4_TX_CONTROL — Offset 1304h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1304h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:29	0h RW	**Time Select (TFSEL):** Select bits for one of the four DMA_TBS_CTRL register fields (FTOS, FGSN, FTOV) for the channel. 0x0: DMA_TBS_CTRL0 selected. 0x1: DMA_TBS_CTRL1 selected. 0x2: DMA_TBS_CTRL2 selected. 0x3: DMA_TBS_CTRL3 selected.
28	0h RW	**Enhanced Descriptor Enable (EDSE):** When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes. 0x0 (DISABLE): Enhanced Descriptor is disabled. 0x1 (ENABLE): Enhanced Descriptor is enabled.
27:24	0h RW	**Transmit QOS. (TQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Transmit Programmable Burst Length (TXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RW	**Ignore PBL Requirement (IPBL):** When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled. 0x1 (ENABLE): Ignore PBL Requirement is enabled.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RW	**TSE_MODE:** TSE Mode - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved 0x0 (TSO_USO): TSO/USO. 0x1 (UFOWC): UFO with Checksum. 0x2 (UFOWOC): UFO without Checksum. 0x3 (RSVD): Reserved.
12	0h RW	**TCP Segmentation Enabled (TSE):** When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/ Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled. 0x1 (ENABLE): TCP Segmentation is enabled.
11:5	0h RO	**Reserved**
4	0h RW	**Operate on Second Packet (OSF):** When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled. 0x1 (ENABLE): Operate on Second Packet enabled.
3:1	0h RW	**Transmit Channel Weight (TCW):** This field indicates the weight assigned to the corresponding Transmit channel. When reset is complete, this field is set to 0 for all channels by default, resulting in equal weights to all channels.
0	0h RW	**Start or Stop Transmission Command (ST):** When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command. 0x1 (START): Start Transmission Command.

10.2.591 DMA_CH4_RX_CONTROL — Offset 1308h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1308h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Rx Packet Flush. (RPF):** When this bit is set to 1, then GbE Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the GbE Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled. 0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	**Reserved**
27:24	0h RW	**Rx AXI4 QOS. (RQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Receive Programmable Burst Length (RXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:4	000h RW	**Receive Buffer size High (RBSZ_13_Y):** RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO	**Receive Buffer size Low (RBSZ_X_0):** RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	**Start or Stop Receive (SR):** When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.

10.2.592 DMA_CH4_TXDESC_LIST_HADDRESS — Offset 1310h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1310h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Transmit List (TDESHA):** This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

10.2.593 DMA_CH4_TXDESC_LIST_ADDRESS — Offset 1314h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1314h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Transmit List (TDESLA):** This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.594 DMA_CH4_RXDESC_LIST_HADDRESS — Offset 1318h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list.

Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1318h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Receive List (RDESHA):** This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

10.2.595 DMA_CH4_RXDESC_LIST_ADDRESS — Offset 131Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list.

This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 131Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Receive List (RDESLA):** This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.596 DMA_CH4_TXDESC_TAIL_POINTER — Offset 1320h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1320h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Transmit Descriptor Tail Pointer (TDTP):** This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.597 DMA_CH4_RXDESC_TAIL_POINTER — Offset 1328h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1328h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Receive Descriptor Tail Pointer (RDTP):** This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.598 DMA_CH4_TXDESC_RING_LENGTH — Offset 132Ch

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 132Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Transmit Descriptor Ring Length (TDRL):** This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

10.2.599 DMA_CH4_RXDESC_RING_LENGTH — Offset 1330h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1330h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Receive Descriptor Ring Length (RDRL):** This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

10.2.600 DMA_CH4_INTERRUPT_ENABLE — Offset 1334h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1334h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Normal Interrupt Summary Enable (NIE):** When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.
14	0h RW	**Abnormal Interrupt Summary Enable (AIE):** When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.
13	0h RW	**Context Descriptor Error Enable (CDEE):** When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.
12	0h RW	**Fatal Bus Error Enable (FBEE):** When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.
11	0h RW	**Early Receive Interrupt Enable (ERIE):** When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.
10	0h RW	**Early Transmit Interrupt Enable (ETIE):** When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled. 0x1 (ENABLE): Early Transmit Interrupt is enabled.
9	0h RW	**Receive Watchdog Timeout Enable (RWTE):** When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Receive Stopped Enable (RSE):** When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	**Receive Buffer Unavailable Enable (RBUE):** When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	**Receive Interrupt Enable (RIE):** When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:3	0h RO	**Reserved**
2	0h RW	**Transmit Buffer Unavailable Enable (TBUE):** When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled. 0x1 (ENABLE): Transmit Buffer Unavailable is enabled.
1	0h RW	**Transmit Stopped Enable (TXSE):** When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled. 0x1 (ENABLE): Transmit Stopped is enabled.
0	0h RW	**Transmit Interrupt Enable (TIE):** When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled. 0x1 (ENABLE): Transmit Interrupt is enabled.

10.2.601 DMA_CH4_RX_INTERRUPT_WATCHDOG_TIMER — Offset 1338h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1338h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RW	**Receive Interrupt Watchdog Timer Count Units (RWTU):** This fields indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	**Reserved**
7:0	00h RW	**Receive Interrupt Watchdog Timer Count (RWT):** This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

10.2.602 DMA_CH4_SLOT_FUNCTION_CONTROL_STATUS — Offset 133Ch

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 133Ch	000007C0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**Reference Slot Number (RSN):** This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	07Ch RW	**Slot Interval Value (SIV):** This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Advance Slot Check (ASC):** When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set. 0x0 (DISABLE): Advance Slot Check is disabled. 0x1 (ENABLE): Advance Slot Check is enabled.
0	0h RW	**Enable Slot Comparison (ESC):** When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is - equal to the reference slot number or - ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets. 0x0 (DISABLE): Slot Comparison is disabled. 0x1 (ENABLE): Slot Comparison is enabled.

10.2.603 DMA_CH4_CURRENT_APP_TXDESC — Offset 1344h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1344h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Descriptor Address Pointer (CURTDESAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.604 DMA_CH4_CURRENT_APP_RXDESC — Offset 134Ch

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 134Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Descriptor Address Pointer (CURRDESAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.605 DMA_CH4_CURRENT_APP_TXBUFFER_H — Offset 1350h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1350h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTRH):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.606 DMA_CH4_CURRENT_APP_TXBUFFER — Offset 1354h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1354h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.607 DMA_CH4_CURRENT_APP_RXBUFFER_H — Offset 1358h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1358h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTRH):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.608 DMA_CH4_CURRENT_APP_RXBUFFER — Offset 135Ch

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 135Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.609 DMA_CH4_STATUS — Offset 1360h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1360h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:19	0h RO	**Rx DMA Error Bits (REB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	0h RO	**Tx DMA Error Bits (TEB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	0h RW	**Normal Interrupt Summary (NIS):** Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected. 0x1 (ACTIVE): Normal Interrupt Summary status detected.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Abnormal Interrupt Summary (AIS):** Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected. 0x1 (ACTIVE): Abnormal Interrupt Summary status detected.
13	0h RW	**Context Descriptor Error (CDE):** This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected. 0x1 (ACTIVE): Context Descriptor Error status detected.
12	0h RW	**Fatal Bus Error (FBE):** This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected. 0x1 (ACTIVE): Fatal Bus Error status detected.
11	0h RW	**Early Receive Interrupt (ERI):** This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected. 0x1 (ACTIVE): Early Receive Interrupt status detected.
10	0h RW	**Early Transmit Interrupt (ETI):** This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected. 0x1 (ACTIVE): Early Transmit Interrupt status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Receive Watchdog Timeout (RWT):** This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected. 0x1 (ACTIVE): Receive Watchdog Timeout status detected.
8	0h RW	**Receive Process Stopped (RPS):** This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected. 0x1 (ACTIVE): Receive Process Stopped status detected.
7	0h RW	**Receive Buffer Unavailable (RBU):** This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected. 0x1 (ACTIVE): Receive Buffer Unavailable status detected.
6	0h RW	**Receive Interrupt (RI):** This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected. 0x1 (ACTIVE): Receive Interrupt status detected.
5:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Transmit Buffer Unavailable (TBU):** This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected. 0x1 (ACTIVE): Transmit Buffer Unavailable status detected.
1	0h RW	**Transmit Process Stopped (TPS):** This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected. 0x1 (ACTIVE): Transmit Process Stopped status detected.
0	0h RW	**Transmit Interrupt (TI):** This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected. 0x1 (ACTIVE): Transmit Interrupt status detected.

10.2.610 DMA_CH4_MISS_FRAME_CNT — Offset 1364h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1364h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Overflow status of the MFC Counter (MFCO):** When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred. 0x1 (ACTIVE): Miss Frame Counter overflow occurred.
14:11	0h RO	**Reserved**
10:0	000h RO	**Dropped Packet Counters (MFC):** This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.611 DMA_CH4_RXP_ACCEPT_CNT — Offset 1368h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1368h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Accept Counter Overflow Bit (RXPACOF):** When set, this bit indicates that the RXPAC Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Accept Counter overflow not occurred. 0x1 (ACTIVE): Rx Parser Accept Counter overflow occurred.
30:0	00000000h RO	**Rx Parser Accept Counter (RXPAC):** This 31-bit counter is implemented whenever a Rx Parser Accept a packet due to AF =1. The counter is cleared when the register is read.

10.2.612 DMA_CH4_RX_ERI_CNT — Offset 136Ch

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 136Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RO	**ERI Counter (ECNT):** When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

10.2.613 DMA_CH5_CONTROL — Offset 1380h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1380h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Split Headers (SPH):** When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. 0x0 (DISABLE): Split Headers feature is disabled. 0x1 (ENABLE): Split Headers feature is enabled.
23:21	0h RO	**Reserved**
20:18	0h RW	**Descriptor Skip Length (DSL):** This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	**Reserved**
16	0h RW	**8xPBL mode (PBLX8):** When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:0	0h RO	**Reserved**

10.2.614 DMA_CH5_TX_CONTROL — Offset 1384h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1384h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:29	0h RW	**Time Select (TFSEL):** Select bits for one of the four DMA_TBS_CTRL register fields (FTOS, FGSN, FTOV) for the channel. 0x0: DMA_TBS_CTRL0 selected. 0x1: DMA_TBS_CTRL1 selected. 0x2: DMA_TBS_CTRL2 selected. 0x3: DMA_TBS_CTRL3 selected.
28	0h RW	**Enhanced Descriptor Enable (EDSE):** When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes. 0x0 (DISABLE): Enhanced Descriptor is disabled. 0x1 (ENABLE): Enhanced Descriptor is enabled.
27:24	0h RW	**Transmit QOS. (TQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Transmit Programmable Burst Length (TXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RW	**Ignore PBL Requirement (IPBL):** When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled. 0x1 (ENABLE): Ignore PBL Requirement is enabled.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RW	**TSE_MODE:** TSE Mode - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved 0x0 (TSO_USO): TSO/USO. 0x1 (UFOWC): UFO with Checksum. 0x2 (UFOWOC): UFO without Checksum. 0x3 (RSVD): Reserved.
12	0h RW	**TCP Segmentation Enabled (TSE):** When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/ Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled. 0x1 (ENABLE): TCP Segmentation is enabled.
11:5	0h RO	**Reserved**
4	0h RW	**Operate on Second Packet (OSF):** When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled. 0x1 (ENABLE): Operate on Second Packet enabled.
3:1	0h RW	**Transmit Channel Weight (TCW):** This field indicates the weight assigned to the corresponding Transmit channel. When reset is complete, this field is set to 0 for all channels by default, resulting in equal weights to all channels.
0	0h RW	**Start or Stop Transmission Command (ST):** When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command. 0x1 (START): Start Transmission Command.

10.2.615 DMA_CH5_RX_CONTROL — Offset 1388h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1388h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Rx Packet Flush. (RPF):** When this bit is set to 1, then GbE Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the GbE Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled. 0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	**Reserved**
27:24	0h RW	**Rx AXI4 QOS. (RQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Receive Programmable Burst Length (RXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:4	000h RW	**Receive Buffer size High (RBSZ_13_Y):** RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO	**Receive Buffer size Low (RBSZ_X_0):** RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	**Start or Stop Receive (SR):** When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.

10.2.616 DMA_CH5_TXDESC_LIST_HADDRESS — Offset 1390h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1390h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Transmit List (TDESHA):** This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

10.2.617 DMA_CH5_TXDESC_LIST_ADDRESS — Offset 1394h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1394h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Transmit List (TDESLA):** This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.618 DMA_CH5_RXDESC_LIST_HADDRESS — Offset 1398h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list.

Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1398h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Receive List (RDESHA):** This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

10.2.619 DMA_CH5_RXDESC_LIST_ADDRESS — Offset 139Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list.

This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 139Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Receive List (RDESLA):** This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.620 DMA_CH5_TXDESC_TAIL_POINTER — Offset 13A0h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Transmit Descriptor Tail Pointer (TDTP):** This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.621 DMA_CH5_RXDESC_TAIL_POINTER — Offset 13A8h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Receive Descriptor Tail Pointer (RDTP):** This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.622 DMA_CH5_TXDESC_RING_LENGTH — Offset 13ACh

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Transmit Descriptor Ring Length (TDRL):** This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

10.2.623 DMA_CH5_RXDESC_RING_LENGTH — Offset 13B0h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Receive Descriptor Ring Length (RDRL):** This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

10.2.624 DMA_CH5_INTERRUPT_ENABLE — Offset 13B4h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Normal Interrupt Summary Enable (NIE):** When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.
14	0h RW	**Abnormal Interrupt Summary Enable (AIE):** When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.
13	0h RW	**Context Descriptor Error Enable (CDEE):** When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.
12	0h RW	**Fatal Bus Error Enable (FBEE):** When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.
11	0h RW	**Early Receive Interrupt Enable (ERIE):** When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.
10	0h RW	**Early Transmit Interrupt Enable (ETIE):** When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled. 0x1 (ENABLE): Early Transmit Interrupt is enabled.
9	0h RW	**Receive Watchdog Timeout Enable (RWTE):** When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Receive Stopped Enable (RSE):** When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	**Receive Buffer Unavailable Enable (RBUE):** When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	**Receive Interrupt Enable (RIE):** When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:3	0h RO	**Reserved**
2	0h RW	**Transmit Buffer Unavailable Enable (TBUE):** When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled. 0x1 (ENABLE): Transmit Buffer Unavailable is enabled.
1	0h RW	**Transmit Stopped Enable (TXSE):** When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled. 0x1 (ENABLE): Transmit Stopped is enabled.
0	0h RW	**Transmit Interrupt Enable (TIE):** When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled. 0x1 (ENABLE): Transmit Interrupt is enabled.

10.2.625 DMA_CH5_RX_INTERRUPT_WATCHDOG_TIMER — Offset 13B8h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RW	**Receive Interrupt Watchdog Timer Count Units (RWTU):** This fields indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	**Reserved**
7:0	00h RW	**Receive Interrupt Watchdog Timer Count (RWT):** This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

10.2.626 DMA_CH5_SLOT_FUNCTION_CONTROL_STATUS — Offset 13BCh

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13BCh	000007C0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**Reference Slot Number (RSN):** This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	07Ch RW	**Slot Interval Value (SIV):** This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Advance Slot Check (ASC):** When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set. 0x0 (DISABLE): Advance Slot Check is disabled. 0x1 (ENABLE): Advance Slot Check is enabled.
0	0h RW	**Enable Slot Comparison (ESC):** When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is - equal to the reference slot number or - ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets. 0x0 (DISABLE): Slot Comparison is disabled. 0x1 (ENABLE): Slot Comparison is enabled.

10.2.627 DMA_CH5_CURRENT_APP_TXDESC — Offset 13C4h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Descriptor Address Pointer (CURTDESAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.628 DMA_CH5_CURRENT_APP_RXDESC — Offset 13CCh

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Descriptor Address Pointer (CURRDESAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.629 DMA_CH5_CURRENT_APP_TXBUFFER_H — Offset 13D0h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTRH):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.630 DMA_CH5_CURRENT_APP_TXBUFFER — Offset 13D4h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.631 DMA_CH5_CURRENT_APP_RXBUFFER_H — Offset 13D8h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTRH):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.632 DMA_CH5_CURRENT_APP_RXBUFFER — Offset 13DCh

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.633 DMA_CH5_STATUS — Offset 13E0h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:19	0h RO	**Rx DMA Error Bits (REB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	0h RO	**Tx DMA Error Bits (TEB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	0h RW	**Normal Interrupt Summary (NIS):** Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected. 0x1 (ACTIVE): Normal Interrupt Summary status detected.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Abnormal Interrupt Summary (AIS):** Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected. 0x1 (ACTIVE): Abnormal Interrupt Summary status detected.
13	0h RW	**Context Descriptor Error (CDE):** This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected. 0x1 (ACTIVE): Context Descriptor Error status detected.
12	0h RW	**Fatal Bus Error (FBE):** This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected. 0x1 (ACTIVE): Fatal Bus Error status detected.
11	0h RW	**Early Receive Interrupt (ERI):** This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected. 0x1 (ACTIVE): Early Receive Interrupt status detected.
10	0h RW	**Early Transmit Interrupt (ETI):** This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected. 0x1 (ACTIVE): Early Transmit Interrupt status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Receive Watchdog Timeout (RWT):** This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected. 0x1 (ACTIVE): Receive Watchdog Timeout status detected.
8	0h RW	**Receive Process Stopped (RPS):** This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected. 0x1 (ACTIVE): Receive Process Stopped status detected.
7	0h RW	**Receive Buffer Unavailable (RBU):** This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected. 0x1 (ACTIVE): Receive Buffer Unavailable status detected.
6	0h RW	**Receive Interrupt (RI):** This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected. 0x1 (ACTIVE): Receive Interrupt status detected.
5:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Transmit Buffer Unavailable (TBU):** This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected. 0x1 (ACTIVE): Transmit Buffer Unavailable status detected.
1	0h RW	**Transmit Process Stopped (TPS):** This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected. 0x1 (ACTIVE): Transmit Process Stopped status detected.
0	0h RW	**Transmit Interrupt (TI):** This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected. 0x1 (ACTIVE): Transmit Interrupt status detected.

10.2.634 DMA_CH5_MISS_FRAME_CNT — Offset 13E4h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Overflow status of the MFC Counter (MFCO):** When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred. 0x1 (ACTIVE): Miss Frame Counter overflow occurred.
14:11	0h RO	**Reserved**
10:0	000h RO	**Dropped Packet Counters (MFC):** This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.635 DMA_CH5_RXP_ACCEPT_CNT — Offset 13E8h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Accept Counter Overflow Bit (RXPACOF):** When set, this bit indicates that the RXPAC Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Accept Counter overflow not occurred. 0x1 (ACTIVE): Rx Parser Accept Counter overflow occurred.
30:0	00000000h RO	**Rx Parser Accept Counter (RXPAC):** This 31-bit counter is implemented whenever a Rx Parser Accept a packet due to AF =1. The counter is cleared when the register is read.

10.2.636 DMA_CH5_RX_ERI_CNT — Offset 13ECh

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RO	**ERI Counter (ECNT):** When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

10.2.637 DMA_CH6_CONTROL — Offset 1400h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1400h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Split Headers (SPH):** When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. 0x0 (DISABLE): Split Headers feature is disabled. 0x1 (ENABLE): Split Headers feature is enabled.
23:21	0h RO	**Reserved**
20:18	0h RW	**Descriptor Skip Length (DSL):** This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	**Reserved**
16	0h RW	**8xPBL mode (PBLX8):** When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:0	0h RO	**Reserved**

10.2.638 DMA_CH6_TX_CONTROL — Offset 1404h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1404h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:29	0h RW	**Time Select (TFSEL):** Select bits for one of the four DMA_TBS_CTRL register fields (FTOS, FGSN, FTOV) for the channel. 0x0: DMA_TBS_CTRL0 selected. 0x1: DMA_TBS_CTRL1 selected. 0x2: DMA_TBS_CTRL2 selected. 0x3: DMA_TBS_CTRL3 selected.
28	0h RW	**Enhanced Descriptor Enable (EDSE):** When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes. 0x0 (DISABLE): Enhanced Descriptor is disabled. 0x1 (ENABLE): Enhanced Descriptor is enabled.
27:24	0h RW	**Transmit QOS. (TQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Transmit Programmable Burst Length (TXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RW	**Ignore PBL Requirement (IPBL):** When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled. 0x1 (ENABLE): Ignore PBL Requirement is enabled.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RW	**TSE_MODE:** TSE Mode - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved 0x0 (TSO_USO): TSO/USO. 0x1 (UFOWC): UFO with Checksum. 0x2 (UFOWOC): UFO without Checksum. 0x3 (RSVD): Reserved.
12	0h RW	**TCP Segmentation Enabled (TSE):** When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/ Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled. 0x1 (ENABLE): TCP Segmentation is enabled.
11:5	0h RO	**Reserved**
4	0h RW	**Operate on Second Packet (OSF):** When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled. 0x1 (ENABLE): Operate on Second Packet enabled.
3:1	0h RW	**Transmit Channel Weight (TCW):** This field indicates the weight assigned to the corresponding Transmit channel. When reset is complete, this field is set to 0 for all channels by default, resulting in equal weights to all channels.
0	0h RW	**Start or Stop Transmission Command (ST):** When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command. 0x1 (START): Start Transmission Command.

10.2.639 DMA_CH6_RX_CONTROL — Offset 1408h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1408h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Rx Packet Flush. (RPF):** When this bit is set to 1, then GbE Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the GbE Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled. 0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	**Reserved**
27:24	0h RW	**Rx AXI4 QOS. (RQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Receive Programmable Burst Length (RXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:4	000h RW	**Receive Buffer size High (RBSZ_13_Y):** RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO	**Receive Buffer size Low (RBSZ_X_0):** RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	**Start or Stop Receive (SR):** When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.

10.2.640 DMA_CH6_TXDESC_LIST_HADDRESS — Offset 1410h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1410h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Transmit List (TDESHA):** This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

10.2.641 DMA_CH6_TXDESC_LIST_ADDRESS — Offset 1414h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1414h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Transmit List (TDESLA):** This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.642 DMA_CH6_RXDESC_LIST_HADDRESS — Offset 1418h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list.

Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1418h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Receive List (RDESHA):** This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

10.2.643 DMA_CH6_RXDESC_LIST_ADDRESS — Offset 141Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list.

This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 141Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Receive List (RDESLA):** This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.644 DMA_CH6_TXDESC_TAIL_POINTER — Offset 1420h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1420h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Transmit Descriptor Tail Pointer (TDTP):** This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.645 DMA_CH6_RXDESC_TAIL_POINTER — Offset 1428h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1428h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Receive Descriptor Tail Pointer (RDTP):** This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.646 DMA_CH6_TXDESC_RING_LENGTH — Offset 142Ch

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 142Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Transmit Descriptor Ring Length (TDRL):** This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

10.2.647 DMA_CH6_RXDESC_RING_LENGTH — Offset 1430h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1430h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Receive Descriptor Ring Length (RDRL):** This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

10.2.648 DMA_CH6_INTERRUPT_ENABLE — Offset 1434h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1434h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Normal Interrupt Summary Enable (NIE):** When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.
14	0h RW	**Abnormal Interrupt Summary Enable (AIE):** When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.
13	0h RW	**Context Descriptor Error Enable (CDEE):** When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.
12	0h RW	**Fatal Bus Error Enable (FBEE):** When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.
11	0h RW	**Early Receive Interrupt Enable (ERIE):** When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.
10	0h RW	**Early Transmit Interrupt Enable (ETIE):** When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled. 0x1 (ENABLE): Early Transmit Interrupt is enabled.
9	0h RW	**Receive Watchdog Timeout Enable (RWTE):** When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Receive Stopped Enable (RSE):** When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	**Receive Buffer Unavailable Enable (RBUE):** When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	**Receive Interrupt Enable (RIE):** When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:3	0h RO	**Reserved**
2	0h RW	**Transmit Buffer Unavailable Enable (TBUE):** When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled. 0x1 (ENABLE): Transmit Buffer Unavailable is enabled.
1	0h RW	**Transmit Stopped Enable (TXSE):** When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled. 0x1 (ENABLE): Transmit Stopped is enabled.
0	0h RW	**Transmit Interrupt Enable (TIE):** When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled. 0x1 (ENABLE): Transmit Interrupt is enabled.

10.2.649 DMA_CH6_RX_INTERRUPT_WATCHDOG_TIMER — Offset 1438h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1438h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RW	**Receive Interrupt Watchdog Timer Count Units (RWTU):** This fields indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	**Reserved**
7:0	00h RW	**Receive Interrupt Watchdog Timer Count (RWT):** This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

10.2.650 DMA_CH6_SLOT_FUNCTION_CONTROL_STATUS — Offset 143Ch

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 143Ch	000007C0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**Reference Slot Number (RSN):** This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	07Ch RW	**Slot Interval Value (SIV):** This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Advance Slot Check (ASC):** When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set. 0x0 (DISABLE): Advance Slot Check is disabled. 0x1 (ENABLE): Advance Slot Check is enabled.
0	0h RW	**Enable Slot Comparison (ESC):** When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is - equal to the reference slot number or - ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets. 0x0 (DISABLE): Slot Comparison is disabled. 0x1 (ENABLE): Slot Comparison is enabled.

10.2.651 DMA_CH6_CURRENT_APP_TXDESC — Offset 1444h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1444h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Descriptor Address Pointer (CURTDESAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.652 DMA_CH6_CURRENT_APP_RXDESC — Offset 144Ch

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 144Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Descriptor Address Pointer (CURRDESAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.653 DMA_CH6_CURRENT_APP_TXBUFFER_H — Offset 1450h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1450h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTRH):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.654 DMA_CH6_CURRENT_APP_TXBUFFER — Offset 1454h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1454h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.655 DMA_CH6_CURRENT_APP_RXBUFFER_H — Offset 1458h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1458h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTRH):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.656 DMA_CH6_CURRENT_APP_RXBUFFER — Offset 145Ch

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 145Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.657 DMA_CH6_STATUS — Offset 1460h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1460h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:19	0h RO	**Rx DMA Error Bits (REB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	0h RO	**Tx DMA Error Bits (TEB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	0h RW	**Normal Interrupt Summary (NIS):** Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected. 0x1 (ACTIVE): Normal Interrupt Summary status detected.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Abnormal Interrupt Summary (AIS):** Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected. 0x1 (ACTIVE): Abnormal Interrupt Summary status detected.
13	0h RW	**Context Descriptor Error (CDE):** This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected. 0x1 (ACTIVE): Context Descriptor Error status detected.
12	0h RW	**Fatal Bus Error (FBE):** This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected. 0x1 (ACTIVE): Fatal Bus Error status detected.
11	0h RW	**Early Receive Interrupt (ERI):** This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected. 0x1 (ACTIVE): Early Receive Interrupt status detected.
10	0h RW	**Early Transmit Interrupt (ETI):** This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected. 0x1 (ACTIVE): Early Transmit Interrupt status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Receive Watchdog Timeout (RWT):** This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected. 0x1 (ACTIVE): Receive Watchdog Timeout status detected.
8	0h RW	**Receive Process Stopped (RPS):** This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected. 0x1 (ACTIVE): Receive Process Stopped status detected.
7	0h RW	**Receive Buffer Unavailable (RBU):** This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected. 0x1 (ACTIVE): Receive Buffer Unavailable status detected.
6	0h RW	**Receive Interrupt (RI):** This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected. 0x1 (ACTIVE): Receive Interrupt status detected.
5:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Transmit Buffer Unavailable (TBU):** This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected. 0x1 (ACTIVE): Transmit Buffer Unavailable status detected.
1	0h RW	**Transmit Process Stopped (TPS):** This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected. 0x1 (ACTIVE): Transmit Process Stopped status detected.
0	0h RW	**Transmit Interrupt (TI):** This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected. 0x1 (ACTIVE): Transmit Interrupt status detected.

10.2.658 DMA_CH6_MISS_FRAME_CNT — Offset 1464h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1464h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Overflow status of the MFC Counter (MFCO):** When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred. 0x1 (ACTIVE): Miss Frame Counter overflow occurred.
14:11	0h RO	**Reserved**
10:0	000h RO	**Dropped Packet Counters (MFC):** This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.659 DMA_CH6_RXP_ACCEPT_CNT — Offset 1468h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1468h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Accept Counter Overflow Bit (RXPACOF):** When set, this bit indicates that the RXPAC Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Accept Counter overflow not occurred. 0x1 (ACTIVE): Rx Parser Accept Counter overflow occurred.
30:0	00000000h RO	**Rx Parser Accept Counter (RXPAC):** This 31-bit counter is implemented whenever a Rx Parser Accept a packet due to AF =1. The counter is cleared when the register is read.

10.2.660 DMA_CH6_RX_ERI_CNT — Offset 146Ch

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 146Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RO	**ERI Counter (ECNT):** When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

10.2.661 DMA_CH7_CONTROL — Offset 1480h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1480h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Split Headers (SPH):** When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. 0x0 (DISABLE): Split Headers feature is disabled. 0x1 (ENABLE): Split Headers feature is enabled.
23:21	0h RO	**Reserved**
20:18	0h RW	**Descriptor Skip Length (DSL):** This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	**Reserved**
16	0h RW	**8xPBL mode (PBLX8):** When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:0	0h RO	**Reserved**

10.2.662 DMA_CH7_TX_CONTROL — Offset 1484h

The DMA Channel Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1484h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:29	0h RW	**TFSEL:**
28	0h RW	**Enhanced Descriptor Enable (EDSE):** When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes. 0x0 (DISABLE): Enhanced Descriptor is disabled. 0x1 (ENABLE): Enhanced Descriptor is enabled.
27:24	0h RW	**Transmit QOS. (TQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Transmit Programmable Burst Length (TXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RW	**Ignore PBL Requirement (IPBL):** When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled. 0x1 (ENABLE): Ignore PBL Requirement is enabled.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RW	**TSE_MODE:** TSE Mode - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved 0x0 (TSO_USO): TSO/USO. 0x1 (UFOWC): UFO with Checksum. 0x2 (UFOWOC): UFO without Checksum. 0x3 (RSVD): Reserved.
12	0h RW	**TCP Segmentation Enabled (TSE):** When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/ Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled. 0x1 (ENABLE): TCP Segmentation is enabled.
11:5	0h RO	**Reserved**
4	0h RW	**Operate on Second Packet (OSF):** When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled. 0x1 (ENABLE): Operate on Second Packet enabled.
3:1	0h RW	**Transmit Channel Weight (TCW):** This field indicates the weight assigned to the corresponding Transmit channel. When reset is complete, this field is set to 0 for all channels by default, resulting in equal weights to all channels.
0	0h RW	**Start or Stop Transmission Command (ST):** When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command. 0x1 (START): Start Transmission Command.

10.2.663 DMA_CH7_RX_CONTROL — Offset 1488h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1488h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Rx Packet Flush. (RPF):** When this bit is set to 1, then GbE Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the GbE Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled. 0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	**Reserved**
27:24	0h RW	**Rx AXI4 QOS. (RQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Receive Programmable Burst Length (RXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:4	000h RW	**Receive Buffer size High (RBSZ_13_Y):** RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO	**Receive Buffer size Low (RBSZ_X_0):** RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	**Start or Stop Receive (SR):** When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.

10.2.664 DMA_CH7_TXDESC_LIST_HADDRESS — Offset 1490h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1490h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Transmit List (TDESHA):** This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

10.2.665 DMA_CH7_TXDESC_LIST_ADDRESS — Offset 1494h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1494h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Transmit List (TDESLA):** This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.666 DMA_CH7_RXDESC_LIST_HADDRESS — Offset 1498h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list.

Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1498h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Receive List (RDESHA):** This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

10.2.667 DMA_CH7_RXDESC_LIST_ADDRESS — Offset 149Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list.

This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 149Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Receive List (RDESLA):** This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.668 DMA_CH7_TXDESC_TAIL_POINTER — Offset 14A0h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Transmit Descriptor Tail Pointer (TDTP):** This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.669 DMA_CH7_RXDESC_TAIL_POINTER — Offset 14A8h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Receive Descriptor Tail Pointer (RDTP):** This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

10.2.670 DMA_CH7_TXDESC_RING_LENGTH — Offset 14ACh

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Transmit Descriptor Ring Length (TDRL):** This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

10.2.671 DMA_CH7_RXDESC_RING_LENGTH — Offset 14B0h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Receive Descriptor Ring Length (RDRL):** This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

10.2.672 DMA_CH7_INTERRUPT_ENABLE — Offset 14B4h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Normal Interrupt Summary Enable (NIE):** When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.
14	0h RW	**Abnormal Interrupt Summary Enable (AIE):** When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.
13	0h RW	**Context Descriptor Error Enable (CDEE):** When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.
12	0h RW	**Fatal Bus Error Enable (FBEE):** When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.
11	0h RW	**Early Receive Interrupt Enable (ERIE):** When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.
10	0h RW	**Early Transmit Interrupt Enable (ETIE):** When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled. 0x1 (ENABLE): Early Transmit Interrupt is enabled.
9	0h RW	**Receive Watchdog Timeout Enable (RWTE):** When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Receive Stopped Enable (RSE):** When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	**Receive Buffer Unavailable Enable (RBUE):** When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	**Receive Interrupt Enable (RIE):** When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:3	0h RO	**Reserved**
2	0h RW	**Transmit Buffer Unavailable Enable (TBUE):** When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled. 0x1 (ENABLE): Transmit Buffer Unavailable is enabled.
1	0h RW	**Transmit Stopped Enable (TXSE):** When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled. 0x1 (ENABLE): Transmit Stopped is enabled.
0	0h RW	**Transmit Interrupt Enable (TIE):** When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled. 0x1 (ENABLE): Transmit Interrupt is enabled.

10.2.673 DMA_CH7_RX_INTERRUPT_WATCHDOG_TIMER — Offset 14B8h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RW	**Receive Interrupt Watchdog Timer Count Units (RWTU):** This fields indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	**Reserved**
7:0	00h RW	**Receive Interrupt Watchdog Timer Count (RWT):** This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

10.2.674 DMA_CH7_SLOT_FUNCTION_CONTROL_STATUS — Offset 14BCh

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14BCh	000007C0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**Reference Slot Number (RSN):** This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	07Ch RW	**Slot Interval Value (SIV):** This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Advance Slot Check (ASC):** When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set. 0x0 (DISABLE): Advance Slot Check is disabled. 0x1 (ENABLE): Advance Slot Check is enabled.
0	0h RW	**Enable Slot Comparison (ESC):** When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is - equal to the reference slot number or - ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets. 0x0 (DISABLE): Slot Comparison is disabled. 0x1 (ENABLE): Slot Comparison is enabled.

10.2.675 DMA_CH7_CURRENT_APP_TXDESC — Offset 14C4h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Descriptor Address Pointer (CURTDESAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.676 DMA_CH7_CURRENT_APP_RXDESC — Offset 14CCh

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Descriptor Address Pointer (CURRDESAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.677 DMA_CH7_CURRENT_APP_TXBUFFER_H — Offset 14D0h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTRH):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.678 DMA_CH7_CURRENT_APP_TXBUFFER — Offset 14D4h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

10.2.679 DMA_CH7_CURRENT_APP_RXBUFFER_H — Offset 14D8h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTRH):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.680 DMA_CH7_CURRENT_APP_RXBUFFER — Offset 14DCh

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

10.2.681 DMA_CH7_STATUS — Offset 14E0h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:19	0h RO	**Rx DMA Error Bits (REB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	0h RO	**Tx DMA Error Bits (TEB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	0h RW	**Normal Interrupt Summary (NIS):** Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected. 0x1 (ACTIVE): Normal Interrupt Summary status detected.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Abnormal Interrupt Summary (AIS):** Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected. 0x1 (ACTIVE): Abnormal Interrupt Summary status detected.
13	0h RW	**Context Descriptor Error (CDE):** This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected. 0x1 (ACTIVE): Context Descriptor Error status detected.
12	0h RW	**Fatal Bus Error (FBE):** This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected. 0x1 (ACTIVE): Fatal Bus Error status detected.
11	0h RW	**Early Receive Interrupt (ERI):** This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected. 0x1 (ACTIVE): Early Receive Interrupt status detected.
10	0h RW	**Early Transmit Interrupt (ETI):** This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected. 0x1 (ACTIVE): Early Transmit Interrupt status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Receive Watchdog Timeout (RWT):** This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected. 0x1 (ACTIVE): Receive Watchdog Timeout status detected.
8	0h RW	**Receive Process Stopped (RPS):** This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected. 0x1 (ACTIVE): Receive Process Stopped status detected.
7	0h RW	**Receive Buffer Unavailable (RBU):** This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected. 0x1 (ACTIVE): Receive Buffer Unavailable status detected.
6	0h RW	**Receive Interrupt (RI):** This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected. 0x1 (ACTIVE): Receive Interrupt status detected.
5:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Transmit Buffer Unavailable (TBU):** This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected. 0x1 (ACTIVE): Transmit Buffer Unavailable status detected.
1	0h RW	**Transmit Process Stopped (TPS):** This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected. 0x1 (ACTIVE): Transmit Process Stopped status detected.
0	0h RW	**Transmit Interrupt (TI):** This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected. 0x1 (ACTIVE): Transmit Interrupt status detected.

10.2.682 DMA_CH7_MISS_FRAME_CNT — Offset 14E4h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Overflow status of the MFC Counter (MFCO):** When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred. 0x1 (ACTIVE): Miss Frame Counter overflow occurred.
14:11	0h RO	**Reserved**
10:0	000h RO	**Dropped Packet Counters (MFC):** This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

10.2.683 DMA_CH7_RXP_ACCEPT_CNT — Offset 14E8h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Accept Counter Overflow Bit (RXPACOF):** When set, this bit indicates that the RXPAC Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Accept Counter overflow not occurred. 0x1 (ACTIVE): Rx Parser Accept Counter overflow occurred.
30:0	00000000h RO	**Rx Parser Accept Counter (RXPAC):** This 31-bit counter is implemented whenever a Rx Parser Accept a packet due to AF =1. The counter is cleared when the register is read.

10.2.684 DMA_CH7_RX_ERI_CNT — Offset 14ECh

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RO	**ERI Counter (ECNT):** When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

10.3 PHY Sublayer Registers Accessible via the MDIO Interface Controller

The Management Data Input/Output (MDIO) Interface is defined in IEEE Standard 802.3-2018:

Clause 22 – Chapter 22.2.4 of the IEEE standard specifies the MDIO interface and registers. The MAC device controlling the MDIO is called the Station Management (STA) entity. The STA issues MDIO frames that have the 2-bit, start-of-frame Symbol Time (ST) code of 01 to access registers. See Table below for the Clause 22 frame format and terminology.

Clause 45 – See Chapter 45 of the IEEE standard. This MDIO interface and register format are extensions to the two-signal MDIO Interface specified in Clause 22. For Clause 45, additional registers are added to the address space by defining MDIO frames that use a start-of-frame Symbol Time (ST) code of 00. See Table below for the Clause 45 frame format and terminology.

The TSN-GbE Controller supports both formats. The C45E bit (bit 1) of the MAC_MDIO_Address register at MMIO offset 200h can be programmed to select the Clause 22 or Clause 45 mode of operation of the STA for the particular MDIO frame. The C45E bit must be programmed to support the capability of the PHY that is connected to MDIO.

The PHY sublayer, or grouping of sublayers, is an individually manageable entity referred to as an MDIO Manageable Device (MMD).

Table 10-3. MDIO Clause 22 Management Frame Format

Operation	32-bit Preamble (1's)	Start of Frame (ST)	Operation Code (OP)	PHY Address (PHYAD)	PHY Register Address (REGAD)	2-Bit Turn-around (TA) Time	Data (16 bits)	High-Z (Idle)
Write	1111...1	01	01	AAAAA	RRRRR	10	16-bit Data to be written to the register	Z
Read	1111...1	01	10	AAAAA	RRRRR	Z0	16-bit Data read from the register	Z

For the Clause 22 frame, the PHY Address (PHYAD) selects one of 32 PHYs attached to the MDIO interface. The PHY Register Address (REGAD) selects one of 32 16-bit registers within each MMD.

Table 10-4. MDIO Clause 45 Management Frame Format

Operation	32-bit Preamble (1's)	Start of Frame (ST)	Operation Code (OP)	Port Address (PRTAD)	Device Address (DEVAD)	2-Bit Turn-around (TA) Time	Address /Data (16 bits)	High-Z (Idle)
Address	1111...1	00	00	PPPPP	EEEEE	Z0	16-bit Address of the register to be accessed on the next cycle	Z
Write	1111...1	00	01	PPPPP	EEEEE	Z0	16-bit Data to be written to the register	Z
Post-Read-Increment Address	1111...1	00	10	PPPPP	EEEEE	Z0	16-bit Data read from the register	Z
Read	1111...1	00	11	PPPPP	EEEEE	Z0	16-bit Data read from the register	Z

For the Clause 45 frame, the Port Address (PRTAD) selects one of 32 Ports attached to the MDIO interface. The Device Address (DEVAD) selects one of 32 unique MDDs per Port. Notice that the register address and register data are separate MDIO frames.

10.3.1 MDIO – PCS PHY Sublayer Registers – PHY Port Address 16h

The MAC uses the GMII as the data interface to the PHY sublayers of the Ethernet LAN Controller including the Physical Coding Sublayer (PCS). The MAC uses the MDIO as the configuration and management interface to the PHY sublayers. This section describes the PCS MDIO registers which follow the IEEE 802.3 standard register sets for the different MMIO Management Devices (MMD).

The PCS PHY sublayer is an IEEE Std 802.3 Clause-45-capable MDIO entity with the following IEEE 802.3 MDIO frame fields:

- Start-of-Frame Symbol Time (ST) 2-bit code: 00b – Indicates a Clause 45 MDIO frame.
- Port Address (PRTAD) 5-bit ID: 10110b (16h) – This Port contains two MMDs:

- MMD (DEVAD) 5-bit ID: 11110b (1Eh) – Vendor-Specific MMD with 65,535 addressable 16-bit registers. The valid register addresses range from 0000h though 000Fh. This MMD is named Vendor-Specific 1 (Control MMD). The registers are used to control the other MMDs of the LAN Controller.
- MMD (DEVAD) 5-bit ID: 11111b (1Fh) – Vendor-Specific MMD with 65,535 addressable 16-bit registers. The valid register addresses range from 0000h though 0E2h. This MMD is named Vendor-Specific MII MMD (VR MII MMD).

Table 10-5. Summary of PCS MDIO Registers, PRTAD = 16h, DEVAD = 1Eh

Register Address (Hex)	Data Size (Bits)	Register Name (Register Symbol)	Default Value [15:0]
0000	16	SR Control MMD PMA Device Identifier Register 1 (SR_VSMMD_PMA_ID1)	0000h
0001	16	SR Control MMD PMA Device Identifier Register 2 (SR_VSMMD_PMA_ID2)	0000h
0002	16	SR Control MMD Device Identifier Register 1 (SR_VSMMD_DEV_ID1)	0000h
0003	16	SR Control MMD Device Identifier Register 2 (SR_VSMMD_DEV_ID2)	000h
0004	16	SR Control MMD PCS Device Identifier Register 1 (SR_VSMMD_PCS_ID1)	7996h
0005	16	SR Control MMD PCS Device Identifier Register 2 (SR_VSMMD_PCS_ID2)	CED0h
0006	16	SR Control MMD AN Device Identifier Register 1 (SR_VSMMD_AN_ID1)	0000h
0007	16	SR Control MMD AN Device Identifier Register 2 (SR_VSMMD_AN_ID2)	0000h
0008	16	SR Control MMD Status Register (SR_VSMMD_STS)	8000h
0009	16	SR Control MMD Control Register (SR_VSMMD_CTRL)	0004h
000E	16	SR Control MMD Package Identifier Register 1 (SR_VSMMD_PKGID1)	0000h
000F	16	SR Control MMD Package Identifier Register 2 (SR_VSMMD_PKGID2)	0000h

Table 10-6. Summary of PCS MDIO Registers, PRTAD = 16h, DEVAD = 1Fh

Register Address (Hex)	Data Size (Bits)	Register Name (Register Symbol)	Default Value [15:0]
0000	16	SR MII MMD Control Register (SR_MII_CTRL)	1140h
0001	16	SR MII MMD Status Register (SR_MII_STS)	0189h
0002	16	SR MII MMD Device Identifier Register 1 (SR_MII_DEV_ID1)	7996h
0003	16	SR MII MMD Device Identifier Register 2 (SR_MII_DEV_ID2)	CED0h
0004	16	SR MII MMD AN Advertisement Register (SR_MII_AN_ADV)	0020h
0005	16	SR MII MMD AN Link Partner Base Ability Register (SR_MII_LP_BABL)	0000h

Table 10-6. Summary of PCS MDIO Registers, PRTAD = 16h, DEVAD = 1Fh

Register Address (Hex)	Data Size (Bits)	Register Name (Register Symbol)	Default Value [15:0]
0006	16	SR MII MMD AN Expansion Register (SR_MII_AN_EXPN)	0000h
000F	16	SR MII MMD Extended Status Register (SR_MII_EXT_STS)	C000h
0708	16	SR MII MMD Time Sync Capability Register (SR_MII_TIME_SYNC_ABL)	0003h
0709	16	SR MII MMD Time Sync Tx Max Delay Lower Register (SR_MII_TIME_SYNC_TX_MAX_DLY_LWR)	0038h
070A	16	SR MII MMD Time Sync Tx Max Delay Upper Register (SR_MII_TIME_SYNC_TX_MAX_DLY_UPR)	0000h
070B	16	SR MII MMD Time Sync Tx Min Delay Lower Register (SR_MII_TIME_SYNC_TX_MIN_DLY_LWR)	0038h
070C	16	SR MII MMD Time Sync Tx Min Delay Upper Register (SR_MII_TIME_SYNC_TX_MIN_DLY_UPR)	0000h
070D	16	SR MII MMD Time Sync Rx Max Delay Lower Register (SR_MII_TIME_SYNC_RX_MAX_DLY_LWR)	00B8h
070E	16	SR MII MMD Time Sync Rx Max Delay Upper Register (SR_MII_TIME_SYNC_RX_MAX_DLY_UPR)	0000h
070F	16	SR MII MMD Time Sync Rx Min Delay Lower Register (SR_MII_TIME_SYNC_RX_MIN_DLY_LWR)	0088h
0710	16	SR MII MMD Time Sync Rx Min Delay Upper Register (SR_MII_TIME_SYNC_RX_MIN_DLY_UPR)	0000h
8000	16	VR MII MMD Digital Control1 Register (VR_MII_DIG_CTRL1)	2400h
8001	16	VR MII MMD AN Control Register (VR_MII_AN_CTRL)	0000h
8002	16	VR MII MMD AN Interrupt and Status Register (VR_MII_AN_INTR_STS)	000Ah
8003	16	VR MII MMD Test Control Register (VR_MII_TC)	0000h
8005	16	VR MII MMD Debug Control Register (VR_MII_DBG_CTRL)	0000h
8006	16	VR MII MMD EEE Mode Control Register (VR_MII_EEE_MCTRL0)	899Ch
8008	16	VR MII MMD EEE Tx Timer Register (VR_MII_EEE_TXTIMER)	0000h
8009	16	VR MII MMD EEE Rx Timer Register (VR_MII_EEE_RXTIMER)	0000h
800A	16	VVR MII MMD Link Timer Control Register (VR_MII_LINK_TIMER_CTRL)	0000h
800B	16	VR MII MMD EEE Mode Control 1 Register (VR_MII_EEE_MCTRL1)	0000h
8010	16	VR MII MMD Digital Status Register (VR_MII_DIG_STS)	0000h
8011	16	VR MII MMD Invalid Code Group Error Count1 Register (VR_MII_ICG_ERRCNT1)	0000h
8018	16	VR MII MMD Miscellaneous Status Register (VR_MII_MISC_STS)	0000h
8020	16	VR MII PHY Rx Lane Status Register (VR_MII_RX_LSTS)	0000h
80E1	16	VR MII MMD Digital Control2 Register (VR_MII_DIG_CTRL2)	0000h
80E2	16	VR MII MMD Digital Error Count Select Register (VR_MII_DIG_ERRCNT_SEL)	0000h

10.3.1.1 SR Control MMD PMA Device Identifier Register 1 (SR_VSMMD_PMA_ID1) - 1Eh, Address 0000h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 0000h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO	0000h	Reserved

10.3.1.2 SR Control MMD PMA Device Identifier Register 2 (SR_VSMMD_PMA_ID2) - 1Eh, Address 0001h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 0001h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO	0000h	Reserved

10.3.1.3 SR Control MMD Device Identifier Register 1(SR_VSMMD_DEV_ID1) - 1Eh, Address 0002h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 0002h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RW	0000h	Organizationally Unique Identifier [3:18] for Vendor-Specific MMD1 (VSDOUI_3_18): Bits 18:3 of the 24-bit Device Organizationally Unique Identifier (OUI) for the vendor-specific MMD1 for identifying the device manufacturer.

10.3.1.4 SR Control MMD Device Identifier Register 2 (SR_VSMMD_DEV_ID2) - 1Eh, Address 0003h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 0003h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:10	RW	00h	Organizationally Unique Identifier[19:24] for Vendor-Specific MMD1 (VSDOUI_19_24): Bits 24:19 of the 24-bit Device Organizationally Unique Identifier (OUI) for the vendor-specific MMD1 for identifying the device manufacturer.
9:4	RW	00h	Model Number for Vendor-Specific MMD1 (VSDMMN_5_0): 6-bit Model number of the vendor-specific MMD1.
3:0	RW	0h	Revision Number for Vendor-Specific MMD1 (VSDRN_3_0): 4-bit Revision number of the vendor-specific MMD1.

10.3.1.5 SR Control MMD PCS Device Identifier Register 1 (SR_VSMMD_PCS_ID1) - 1Eh, Address 0004h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 0004h**

Default: 7996h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RW	7996h	Organizationally Unique Identifier[3:18] for PCS MMD (PCSDOUI_3_18): Bits 18:3 of the 24-bit Device Organizationally Unique Identifier (OUI) for the vendor-specific PCS MMD for identifying the device manufacturer.

10.3.1.6 SR Control MMD PCS Device Identifier Register 2 (SR_VSMMD_PCS_ID2) - 1Eh, Address 0005h

This register is RW by software via the MDIO interface. The 24-bit Device Organizationally Unique Identifier (OUI) is default-set to CDA679h. The Model Number default value is 2Dh and the Revision Number default is 0.SR Control MMD AN Device.

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 0005h**

Default: CED0h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:10	RW	33h	Organizationally Unique Identifier[19:24] for PCS MMD (PCSDOUI_19_24): Bits 24:19 of the 24-bit Device Organizationally Unique Identifier (OUI) for the vendor-specific PCS MMD for identifying the device manufacturer.
9:4	RW	2Dh	Model Number for PCS MMD (PCSDMMN_5_0): 6-bit Model number of the vendor-specific PCS MMD.
3:0	RW	0h	Revision Number for PCS MMD (PCSDRN_3_0): 4-bit Revision number of the vendor-specific PCS MMD.

10.3.1.7 SR Control MMD AN Device Identifier Register 1 (SR_VSMMD_AN_ID1) - 1Eh, Address 0006h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 0006h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RW	0000h	Organizationally Unique Identifier [3:18] for Vendor-Specific MMD1 (VSDOUI_3_18): Bits 18:3 of the 24-bit Device Organizationally Unique Identifier (OUI) for the vendor-specific MMD1 for identifying the device manufacturer.

10.3.1.8 SR Control MMD AN Device Identifier Register 2 (SR_VSMMD_AN_ID2) - 1Eh, Address 0007h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 0007h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO	0000h	Reserved

10.3.1.9 SR Control MMD Status Register (SR_VSMMD_STS) - 1Eh, Address 0008h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 0008h**

Default: 8000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:14	RO/V	10b	Control MMD Device Present (VSDP): This field indicates if the control MMD device is present and responding to this address: 10: Device responding at this address 11, 01, or 00: No device responding at this address
13:0	RO	0000h	Reserved

10.3.1.10 SR Control MMD Control Register (SR_VSMMD_CTRL) - 1Eh, Address 0009hSR Control MMD

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 0009h**

Default: 0004h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:6	RO	0000h	Reserved
5	RW	0b	Power Down Control (PD_CTRL): This bit is used to control the output port 'xpcs_pdown_o'. If this bit is set, xpcs_pdown_o port will NOT be asserted when LPM (Low Power Enable) bit is programmed to 1. If this bit is low, xpcs_down_o port will be asserted when LPM (Low Power Enable) bit is programmed to 1.
4	RW	0b	Fast Simulation Enable (FASTSIM): When set, this bit indicates that the Fast simulation is enabled. When this bit is set to 1, all IEEE Std 802.3 defined long timers that are implemented are reduced to shorter time period in order to reduce the simulation time. The long timers are implemented in Clause 73 and Clause 37 auto-negotiation modules and also EEE Tx and Rx modules.
3	RO	0b	Reserved
2	RW	1b	VS MMD Enable (MII_MMD_EN): When set, this bit indicates that the vendor-specific MMD1 device is accessible. When reset, this bit indicates that the vendor-specific MMD2 (MII MMD) device is not accessible.
1:0	RO	00b	Reserved

10.3.1.11 SR Control MMD Package Identifier Register 1 (SR_VSMMD_PKGID1) - 1Eh, Address 000Eh

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 000Eh**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO	00h	Reserved

10.3.1.12 SR Control MMD Package Identifier Register 2 (SR_VSMMD_PKGID2) - 1Eh, Address 000Fh

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 000Fh**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO	00h	Reserved

10.3.1.13 SR MII MMD Control Register (SR_MII_CTRL) - 1Fh, Address 0000h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 0000h**

Default: 1140h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15	RW	0b	Soft Reset (RST): When the host sets this bit, it triggers the software reset process in which all internal blocks of the PCS are reset, except the Management Interface block. The registers are reset to their default values. When this bit is set, it also resets the PHY. This bit is Self-Cleared by the PCS after 1 MDC clock period of the MDIO interface.
14	RW	0b	Loopback Enable (LBE): This register bit is not used by the design.
13	RW	0b	Speed Selection - LSB (SS13): This bit, along with SS6 (bit 6) of this register, indicates the SGMII speed: SS6 SS13 SGMII Speed 1 0 1000 Mbps 0 1 100 Mbps 0 0 10 Mbps
12	RW	1b	Enable Auto-Negotiation (AN_ENABLE): When set to 1, this bit enables the Clause 37 auto-negotiation process. Default setting is 1.
11	RW	0b	Power-Down Mode (LPM): This bit controls the power-down mode of the PCS. When 0, the PCS operates as normal. When 1, the PCS goes to the Power-Down Mode and clearing this bit resumes PCS normal operation.
10	RO	0b	Reserved
9	RW	0b	Restart Auto-Negotiation (RESTART_AN): When the host writes this bit, the PCS initiates the Auto-Negotiation process. This bit is used to restart the Auto-Negotiation which is already initiated by setting AN_ENABLE (bit 12). The PCS clears this bit after restarting the Auto-Negotiation.
8	RW	1b	Duplex Mode (DUPLEX_MODE): This bit specifies the duplex mode of the PCS. Programming to 0 indicates Half Duplex and 1 (the default value) indicates Full Duplex. For the PHY Link Duplex Mode: If AN_ENABLE (bit 12) is set to 0, this bit determines the PHY Link Duplex Mode. If AN_ENABLE is set to 1, then the PHY Link Duplex Mode is independent of this bit (although the host can write any value) and is determined by the outcome of the Clause 37 Auto-Negotiation process.
7	RO	0b	Reserved
6	RW	1b	Speed Selection – MSB (SS6): This bit, along with SS13 (bit 23) of this register, indicates the SGMII speed. Default value is 1. See SS13 description.
5:0	RO	000000b	Reserved

10.3.1.14 SR MII MMD Status Register (SR_MII_STS) - 1Fh, Address 0001h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 0001h**

Default: 0189h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15	RO	0b	100BASE-T4 Ability (ABL100T4): Not supported. Hardwired to 0.
14	RO	0b	100BASE-X Full-Duplex Ability (FD100ABL): Not supported. Hardwired to 0.
13	RO	0b	100BASE-X Half-Duplex Ability (HD100ABL): Not supported. Hardwired to 0.
12	RO	0b	10 Mbps Full-Duplex Ability (FD10ABL): Not supported. Hardwired to 0.
11	RO	0b	10 Mbps Half-Duplex Ability (HD10ABL): Not supported. Hardwired to 0.
10	RO	0b	100BASE-T2 Full-Duplex Ability (FD100T): Not supported. Hardwired to 0.
9	RO	0b	100BASE-T2 Half-Duplex Ability (HD100T): Not supported. Hardwired to 0.
8	RO/V	1b	Extended Status Information (EXT_STS_ABL): Hardwired to 1 indicating that Extended Status information is present at register address 16'h000F of this MMD device (DEVAD 1Fh).
7	RO	1b	Unidirectional Ability (UN_DIR_ABL): Hardwired to 1 indicating that the PCS is able to transmit GMII irrespective of whether the device has determined the valid link or not.
6	RO	0b	MF Preamble Suppression (MF_PRE_SUP): Hardwired to 0 indicating that The PCS does not accept the MDIO frames with the preamble suppressed.
5	RO	0b	Auto-negotiation Complete (AN_CMPL): When this bit is set to 1, the contents of the AN MMD Advertisement, AN MMD Link partner Ability, and AN MMD Expansion registers are valid. This bit returns 0 if AN_ENABLE is set to 0.
4	RO	0b	Remote Fault (RF): When set to 1, this bit indicates that the PCS detected that the receive link of the link partner is down. This bit is set based on the auto-negotiated (1000BASE-X Auto-Negotiation) information from the link partner. When 0, this bit indicates that the PCS did not detect a Remote Fault.
3	RO	1b	Auto-negotiation Ability (AN_ABL): The PCS always returns this bit as 1 indicating that the PCS is able to perform Auto-Negotiation.
2	RO	0b	Link Status (LINK_STS): When the PCS sets this bit to 1, it indicates that the Rx link is up. If the link goes down, as indicated by 0, this bit is latched by the PCS until the host performs the read operation to this register.
1	RO	0b	Reserved
0	RO	1b	Extended Register Capability (EXT_REG_CAP): The PCS always returns this bit as 1 indicating that the Extended Register Capability exists.

10.3.1.15 SR MII MMD Device Identifier Register 1 (SR_MII_DEV_ID1) - 1Fh, Address 0002h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 0002h**

Default: 7996h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	7996h	Organizationally Unique Identifier[3:18] for PCS MMD (VS_MII_DEV_OUI_3_18): Bits 18:3 of the 24-bit Device Organizationally Unique Identifier (OUI) of the device manufacturer. Writing to bits 15:0 of the vendor-specific PCS MMD Device Identifier Register 1 (SR_VSMMD_PCS_ID1) modifies the content of this register.

10.3.1.16 SR MII MMD Device Identifier Register 2 (SR_MII_DEV_ID2) - 1Fh, Address 0003h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 0003h**

Default: CED0h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:10	RO/V	33h	Organizationally Unique Identifier [19:24] (VS_MMD_DEV_OUI_19_24): Bits 24:19 of the 24-bit Device Organizationally Unique Identifier (OUI) of the device manufacturer. Writing to bits 15:0 of the vendor-specific PCS MMD Device Identifier Register 2 (SR_VSMMD_PCS_ID2) modifies the content of this register.
9:4	RO/V	2Dh	Model Number (VS_MMD_DEV_MMN_5_0): 6-bit Model number of the vendor-specific PCS MMD. Writing to bits 9:4 of the vendor-specific PCS MMD Device Identifier Register 2 (SR_VSMMD_PCS_ID2) modifies the content of this register.
3:0	RO/V	0h	Revision Number (VS_MMD_DEV_RN_3_0): 4-bit Revision number of the vendor-specific PCS MMD. Writing to bits 3:0 of the vendor-specific PCS MMD Device Identifier Register 2 (SR_VSMMD_PCS_ID2) modifies the content of this register.

10.3.1.17 SR MII MMD AN Advertisement Register (SR_MII_AN_ADV) - 1Fh, Address 0004h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 0004h**

Default: 0020h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15	RO/V	0b	Next Page (NP): Not supported. Hardwired to 0.
14	RO	0b	Reserved
13:12	RW	00b	Remote Fault (RF): This field indicates the fault signaling of the local device to be communicated to the link partner. 00: No Error 01: Offline 10: Link Failure 11: Auto-negotiation Error
11:9	RO	000b	Reserved
8:7	RW	00b	Pause Ability (PAUSE): This field indicates the Pause ability of the device: 00: No Pause 01: Asymmetric Pause towards the link partner 10: Symmetric Pause 11: Symmetric Pause and Asymmetric Pause towards the local device. Software can program suitable values based on the capability of the MAC.
6	RW	0b	Half Duplex (HD): When this bit is set, it indicates that the device can operate in the half-duplex mode.
5	RW	1b	Full Duplex (FD): When this bit is set, it indicates that the device can operate in the full-duplex mode.
4:0	R0	00000b	Reserved

10.3.1.18 SR MII MMD AN Link Partner Base Ability Register (SR_MII_LP_BABL) - 1Fh, Address 0005h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 0005h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15	RO/V	0b	Next Page (LP_NP): This bit indicates that the link partner can handle Next Page. Note: To exchange information through Next Page, both devices (local and remote) should have the capability to handle Next Page. The PCS does not support Next Page. Therefore, the Next Page exchange does not happen.
14	RO/V	0b	ACK bit from the Link Partner (LP_ACK): This bit indicates that the link partner has successfully received the page sent by the local device.
13:12	RO/V	00b	Remote Fault (LP_RF): This field indicates the fault signaling of the link partner: 00: No Error 01: Offline 10: Link Failure 11: Auto-negotiation Error
11:9	RO	000b	Reserved
8:7	RO/V	00b	Pause Ability (LP_PAUSE): This field indicates the Pause ability of the link partner: 00: No Pause 01: Asymmetric Pause towards the link partner 10: Symmetric Pause 11: Both Symmetric Pause and Asymmetric Pause towards the local device
6	RO/V	0b	Half Duplex (LP_HD): When this bit is set, it indicates that the link partner is capable of operating in the half-duplex mode.
5	RO/V	0b	Full Duplex (LP_FD): When this bit is set, it indicates that the link partner is capable of operating in the full-duplex mode.
4:0	RO	00000b	Reserved

10.3.1.19 SR MII MMD AN Expansion Register (SR_MII_AN_EXPN) - 1Fh, Address 0006h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 0006h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:3	RO	00h	Reserved
2	RO/V	00h	Local Device NP Able (LD_NP_ABL): The local device (the PCS) always returns this bit as 0 because it does not support Next Page.
1	RO/V	00h	Page Received (PG_RCVD): This bit indicates that the local device (the PCS) received a page from the link partner. 1: The local device received a new page 0: The local device did not receive a new page
0	RO	00h	Reserved

10.3.1.20 SR MII MMD Extended Status Register (SR_MII_EXT_STS) - 1Fh, Address 000Fh

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 000Fh**

Default: C000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15	RO/V	1b	1000BASE-X Full-Duplex Capable (CAP_1G_X_FD): The PCS always returns 1 because it supports this feature.
14	RO/V	1b	1000BASE-X Half-Duplex Capable (CAP_1G_X_HD): The PCS always returns 1 because it supports this feature.
13	RO/V	0b	1000BASE-T Full-Duplex Capable (CAP_1G_T_FD): The PCS always returns 0 because it does not supports this feature.
12	RO/V	0b	1000BASE-T Half-Duplex Capable (CAP_1G_T_HD): The PCS always returns 0 because it does not supports this feature.
11:0	RO	000h	Reserved

10.3.1.21 SR MII MMD Time Sync Capability Register (SR_MII_TIME_SYNC_ABL) - 1Fh, Address 0708h

Type: MDIO Register PRTAD: 16h DEVAD: 1Fh Register Address: 0708h

Default: 0003h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:2	RO	00h	Reserved
1	RO/V	1b	1000BASE-X Half-Duplex Capable (CAP_1G_X_HD): The PCS always returns 1 because it supports this feature.
0	RO/V	1b	1000BASE-T Full-Duplex Capable (CAP_1G_T_FD): The PCS always returns 0 because it does not supports this feature.

10.3.1.22 SR MII MMD Time Sync Tx Max Delay Lower Register (SR_MII_TIME_SYNC_TX_MAX_DLY_LWR) - 1Fh, Address 0709h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 0709h**

Default: 0038h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	38h	Transmit Path Maximum Data Delay, Lower (MII_TX_MAX_DLY_LWR): This field indicates the lower 16-bit of the 32-bit value which indicates the Maximum Data Delay in the Transmit Path of the XPCS in nanoseconds.

10.3.1.23 SR MII MMD Time Sync Tx Max Delay Upper Register (SR_MII_TIME_SYNC_TX_MAX_DLY_UPR) - 1Fh, Address 070Ah

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 070Ah**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	00h	Transmit Path Maximum Data Delay, Upper (MII_TX_MAX_DLY_UPR): This field indicates the upper 16-bit of the 32-bit value which indicates the Maximum Data Delay in the Transmit Path of the XPCS in nanoseconds.

10.3.1.24 SR MII MMD Time Sync Tx Min Delay Lower Register (SR_MII_TIME_SYNC_TX_MIN_DLY_LWR) - 1Fh, Address 070Bh

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 070Bh**

Default: 0038h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	38h	Transmit Path Minimum Data Delay, Lower (MII_TX_MIN_DLY_LWR): This field indicates the lower 16-bit of the 32-bit value which indicates the Minimum Data Delay in the Transmit Path of the XPCS in nanoseconds.

10.3.1.25 SR MII MMD Time Sync Tx Min Delay Upper Register (SR_MII_TIME_SYNC_TX_MIN_DLY_UPR) - 1Fh, Address 070Ch

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 070Ch**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	00h	Transmit Path Minimum Data Delay, Upper (MII_TX_MIN_DLY_UPR): This field indicates the upper 16-bit of the 32-bit value which indicates the Minimum Data Delay in the Transmit Path of the XPCS in nanoseconds.

10.3.1.26 SR MII MMD Time Sync Rx Max Delay Lower Register (SR_MII_TIME_SYNC_RX_MAX_DLY_LWR) - 1Fh, Address 070Dh

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 070Dh**

Default: 00B8h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	B8h	Receive Path Maximum Data Delay, Lower (MII_RX_MAX_DLY_LWR): This field indicates the lower 16-bit of the 32-bit value which indicates the Maximum Data Delay in the Receive Path of the XPCS in nanoseconds.

10.3.1.27 SR MII MMD Time Sync Rx Max Delay Upper Register (SR_MII_TIME_SYNC_RX_MAX_DLY_UPR) - 1Fh, Address 070Eh

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 070Eh**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	00h	Receive Path Maximum Data Delay, Upper (MII_RX_MAX_DLY_UPR): This field indicates the upper 16-bit of the 32-bit value which indicates the Maximum Data Delay in the Receive Path of the XPCS in nanoseconds.

10.3.1.28 SR MII MMD Time Sync Rx Min Delay Lower Register (SR_MII_TIME_SYNC_RX_MIN_DLY_LWR) - 1Fh, Address 070Fh

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 070Fh**

Default: 0088h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	88h	Receive Path Minimum Data Delay, Lower (MII_RX_MIN_DLY_LWR): This field indicates the lower 16-bit of the 32-bit value which indicates the Minimum Data Delay in the Receive Path of the XPCS in nanoseconds.

10.3.1.29 SR MII MMD Time Sync Rx Min Delay Upper Register (SR_MII_TIME_SYNC_RX_MIN_DLY_UPR) - 1Fh, Address 0710h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 0710h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	00h	Receive Path Minimum Data Delay, Upper (MII_RX_MIN_DLY_UPR): This field indicates the upper 16-bit of the 32-bit value which indicates the Minimum Data Delay in the Receive Path of the XPCS in nanoseconds.

10.3.1.30 VR MII MMD Digital Control1 Register (VR_MII_DIG_CTRL1) - 1Fh, Address 8000h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8000h**

Default: 2400h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15	RW	0b	Vendor-Specific Soft Reset (VR_RST): When the host sets this bit, it triggers a vendor-specific software reset process in which all internal blocks of the PCS, except the Management Interface block and CSR block, are reset. When this bit is set, it also resets the PHY. This bit is Self-Cleared by the PCS after 1 MDC clock period for the MDIO interface.
14	RW	0b	Rx to Tx Loopback Enable (R2TLBE): This bit controls the loopback path from the GMII Rx to the GMII Tx at the GMII interface. 0: Loopback path is disabled 1: Loopback path is enabled
13	RW	1b	Enable Vendor-Specific MMD1 (EN_VSMMD1): When this bit is set to 1 (default value), the vendor-specific MMD1 (VSMMD1) is enabled. When this bit is set to zero, VSMMD1 is disabled.
12	RO/V	0b	Enable Clause 37 AN in Backplane Configuration (CL37_BP): Does not apply.
11	RO	0b	Reserved

Bits	Access Type	Default	Field Name and Description
10	RW	1b	Clock Stop Enable (CS_EN): This bit should be programmed based on the capability of the MAC during Rx LPI mode. Programming this bit to 1 allows the PHY to stop the clock during LPI mode. Programming to 0, the clock cannot be stopped during LPI mode.
9	RW	0b	Automatic Speed Mode Change after CL37 AN (MAC_AUTO_SW): When this field is set to 1, the PCS automatically switches to the negotiated SGMII after the completion of CL37 AN. This mode is valid only when the PCS is configured as MAC-side SGMII and should be set only when Auto-Negotiation is enabled (AN_ENABLE bit is set to 1). If this bit is set to 0, the PCS will operate at the speed/duplex mode as per the values programmed to SR MII MMD Control Register. After the completion of CL37 AN, the application has to read the negotiated Speed/Duplex Mode from VR MII MMD AN Interrupt and Status Register and then program SR MII MMD Control Register appropriately. Note: This bit should be set only when the PCS is configured as SGMII MAC, i.e., TX_CONFIG=0.
8	RW	0b	Datapath Initialization Control (INIT): This bit can be set to flush/initialize the various FIFOs implemented inside the PCS. This is Self-Clear bit. After writing 1 to this bit, software should poll this bit continuously. Only after reading this bit as 0 should software proceed to any other operation. When this bit is programmed to 1, RXFIFO_OVF/RXFIFO_UNF bits of the VR MII MMD Digital Status Register might get set incorrectly. Hence, read these register bits (RXFIFO_OVF and RXFIFO_UNF) so that they get cleared. Thereafter, RXFIOF_UNF and RXFIFO_UNF bits would be reliable.
7	RO/V	0b	Mask Running Disparity Error (MSK_RD_ERR): When this bit is set, running disparity errors are ignored by XPCS receiver in evaluating the validity of received code-groups.
6	RW	0b	Pre-emption Packet Enable (PRE_EMP): When this bit is set, it allows the XPCS to properly receive/transmit IEEE Std 802.3br pre-emption packets in SGMII 10M/100M Modes.
5	RO	0b	Reserved
4	RW	0b	Tx Lane 0 Disable (DTXLANED_0): When this bit is set, the PCS disables the Tx Lane 0 of the PHY. When reset, the PCS enables the Tx Lane 0 of the PHY.
3	RW	0b	Over-Ride Control for CL37 Link Timer (CL37_TMR_OVR_RIDE): This bit can be set to over-ride the default value of Clause 37 link timer used by the PCS for auto-negotiation. If this bit is set, the value programmed to the VR MII MMD Link Timer Control Register will be used to compute the duration of Link Timer. This bit should be set only after programming the appropriate value to the VR MII MMD Link Timer Control Register.

Bits	Access Type	Default	Field Name and Description
2	RW	0b	Enable 2.5G GMII Mode (EN_2_5G_MODE): Setting this bit 1 enables the 2.5G GMII Mode of operation. This bit drives the hardware pertaining to 2.5 Gbps SGMII operation.
1	RO	0b	Reserved
0	RW	0b	SGMII PHY Mode Control (PHY_MODE_CTRL): This bit controls the CL37_AN when operating in SGMII (Port 0) PHY mode. When this bit is set to 1, the PCS advertises the values of input ports xpcs_sgmii_link_sts_i, xpcs_sgmii_link_speed_i and xpcs_sgmii_full_duplex_i during SGMII (Port 0) Auto-Negotiation. When this bit is set to 0, SGMII (Port0) Auto-Negotiation will advertise the values programmed to all of these: SGMII_LINK_STS (bit 4) of the VR MII MMD AN Control Register SS13 (bit 13) and SS6 (bit 6) of the SR MII MMD Control Register FD (bit 5) of the SR MII MMD AN Advertisement Register Note: This bit should be set only when the PCS is configured as SGMII PHY, i.e., TX_CONFIG (bit 3 of the VR_MII_AN_CTRL register) = 1.

10.3.1.31 VR MII MMD AN Control Register (VR_MII_AN_CTRL) - 1Fh, Address 8001h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8001h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:9	RO	00h	Reserved
8	RO/V	0b	MII Control (MII_CTRL): This bit controls the width of the MAC interface when operating at SGMII speed modes of 10 Mbps or 100 Mbps. 0: 4-bit MII 1: 8-bit MII
7:5	RO	000b	Reserved
4	RW	0b	SGMII Link Status (SGMII_LINK_STS): This bit is used in Bit 15 of the Config_Reg during IEEE 802.3 Clause 37 Auto-Negotiation when the TX_CONFIG bit of this register is set to 1 in the SGMII/QSGMII/USXGMII mode and when the PHY_MODE_CTRL bit of VR MII MMD Digital Control 1 Register is 0. 0: Link Down 1: Link Up

Bits	Access Type	Default	Field Name and Description
3	RW	0b	Transmit Configuration (TX_CONFIG): This bit controls the Config_Reg value to be used during the IEEE 802.3 Clause 37 Auto-Negotiation in the SGMII/QSGMII/USXGMII mode. 1: Configures the PCS as the PHY side SGMII/QSGMII/USXGMII 0: Configures the PCS as the MAC side SGMII/QSGMII/USXGMII
2:1	RW	00b	PCS Mode (PCS_MODE): This field controls the auto-negotiation (and operating) mode. 00: 1000BASE-X mode (Clause 37 Auto-Negotiation is as per 1000BASEX). 10: SGMII mode (Clause 37 Auto-Negotiation is as per SGMII). 11: QSGMII mode (Clause 37 Auto-Negotiation conforms to QSGMII). Note: The default value is 00. Must be programmed to 10 for SGMII-mode Auto-Negotiation.
0	RW	0b	Clause 37 AN Complete Interrupt Enable (MII_AN_INTR_EN): When set to 1, this bit enables the generation of the IEEE 802.3 Clause 37 Auto-Negotiation Complete interrupt output. When set to 0, it disables the generation of Clause 37 Auto-Negotiation Complete interrupt.

10.3.1.32 VR MII MMD AN Interrupt and Status Register (VR_MII_AN_INTR_STS) - 1Fh, Address 8002h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8002h**

Default: 000Ah Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:5	RO	000h	Reserved
4:1	RO/V	5h	Clause 37 AN SGMII Status/QSGMII Port 0 Status (CL37_ANSGM_STS): This field is valid only when the PCS_MODE[1:0] is set to the SGMII/QSGMII mode and the auto-negotiation is complete. It indicates the status received from remote link after the SGMII/QSGMII (Port 0) Auto-Negotiation is complete. CL37_ANSGM_STS[0] 0: Half Duplex 1: Full Duplex (default value) CL37_ANSGM_STS[2:1] 00: 10 Mbps speed link 01: 100 Mbps speed link 10: 1000 Mbps speed link (default value) CL37_ANSGM_STS[3] 0: Link is Down (default value) 1: Link is Up
0	RW	0b	Clause 37 AN Complete Interrupt (CL37_ANCMPLT_INTR): The PCS sets this bit when IEEE 802.3 Clause 37 Auto-Negotiation is complete. The host must clear this bit by writing 0 to it.

10.3.1.33 VR MII MMD Test Control Register (VR_MII_TC) - 1Fh, Address 8003h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8003h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:3	RO	0000h	Reserved
2	RW	0b	Test Pattern Enable Lanes (TPE): This bit indicates that a test pattern can be enabled in the Tx path after the current normal frame transmission is complete. 0: Test pattern disabled 1: Test pattern enabled The specific test pattern that is generated is based on bits 1:0 of this register.
1:0	RW	2'b00	Test Pattern Select (TP): This field indicates the pattern type that is enabled with Bit 2 of this register. The following are the supported test patterns: 00: High Frequency Test Pattern (default value) 01: Low Frequency Test Pattern 10: Mixed Frequency Test Pattern 11: Reserved The definitions of these test patterns are specified in Annex 48A of IEEE 802.3.

10.3.1.34 VR MII MMD Debug Control Register (VR_MII_DBG_CTRL) - 1Fh, Address 8005h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8005h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:9	RO	7'h0	Reserved
8	RW	1'h0	Transmit Preamble Control (TX_PMBL_CTL): This bit can be set to 1 to prevent possible preamble truncation in the PCS transmitter when operating in 1000BASE-X Mode or 2.5G Mode over GMII. As per IEEE spec, it is permissible for a compliant 1000BASE-X PCS transmit process to truncate the first byte of preamble in order to align the start of the packet on the EVEN boundary. If this bit is set to 1, the XPCS does not delete any preamble bytes (received from GMII Tx interface) and passes on the same number of preamble bytes to its output. The XPCS out this operation by adjusting the IPG. This mode is a deviation from Clause 36 of IEEE Std 802.3, but it can prove useful when operating at 2.5G Mode (over clocked SGMII Mode) and the far-end device is compliant to IEEE Std 802.3bz/cb.
7	RO	1'h0	Reserved
6	RO	1'h0	Reserved

Bits	Access Type	Default	Field Name and Description
5	RW	1'h0	Suppress EEE Loss of Signal Detection (SUPRESS_EEE_LOS_DET): When this field is set to 1, Loss of Signal indicated by the PHY is ignored by the PCS while evaluating the Receive link when operating in EEE mode. Receive link will be purely evaluated based the on data received by the PCS from the PHY. When this field is set to 0, Loss of signal indicated by the PHY will be considered by the PCS while evaluating the Receive link status in EEE mode.
4	RW	1'h0	Suppress Loss of Signal Detection (SUPRESS_LOS_DET): When this field is set to 1, Loss of Signal indicated by the PHY is ignored by the PCS while evaluating the Receive link. Receive link will be purely evaluated based the Rx data received on the port of the PCS. When this field is set to 0, Loss of signal indicated by the PHY will be considered by the PCS while evaluating the Receive link status.
3:1	RO	3'h0	Reserved
0	RW	1'h0	Restart Synchronization (RESTAR_SYNC_0): When set to 1, this bit restarts the Rx Synchronization State machine on Lane 0. The host must clear this bit to 0 before setting it to 1 next time.

10.3.1.35 VR MII MMD EEE Mode Control Register (VR_MII_EEE_MCTRL0)- 1Fh, Address 8006h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8006h**

Default: 899Ch Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:12	RW	4'h8	Clock Stop (CLKSTOP): This field holds the count value after which the Rx clock to the MAC can be stopped. The default value is 8. The host should program this value depending on the capability of the MAC.
11:8	RW	4'h9	100 ns Clock Tic Multiplying Factor (MULT_FACT_100NS): This bit is the multiplying factor to the clk_eee_i clock time period to make it closer to 100 ns. For example, if the clk_eee_i clock time period (clk_eee_i_time_period) is 10 ns, the value of this field is 9, that is, 1 less than 10. This value should be programmed such that the clk_eee_i_time_period * (MULT_FACT_100NS + 1) should be within 80 ns to 120 ns. The default value of this register is 9, assuming that the default clk_eee_i time period to be 10 ns.
7	RW	1'h1	Rx Control Enable (RX_EN_CTRL): This bit controls the generation of the xpcs_rx_en_o{lane} signal. When this bit is set to 1, the xpcs_rx_en_o{lane} signal is deasserted when the EEE receive controller reaches the Quiet state. When this bit set to 0, the xpcs_rx_en_o{lane} signal is not deasserted when the EEE transmit controller reaches the Quiet state.
6	RW	1'h0	Effective 100ns Tic Value (SIGN_BIT): The host should use this bit to fine-tune the EEE timing requirement. The host should set this bit to 0 when the clk_eee_i_time_period * (MULT_FACT_100NS + 1) value is more than 100 ns. The host should set this bit to 1 when the clk_eee_i clock period * MULT_FACT_100NS + 1) value is less than or equal to 100ns.
5	RO	1'h0	Reserved

Bits	Access Type	Default	Field Name and Description
4	RW	1'h1	Tx Control Enable (TX_EN_CTRL): This bit controls the generation of the signals xpcs_tx_en_o {lane}. When this bit is set to 1, the xgxs_tx{lane}_en_o or xpcs_tx_en_o{lane} signal is de-asserted when the EEE transmit controller reaches the Quiet state. When this bit set to 0, the xgxs_tx{lane}_en_o or xpcs_tx_en_o{lane} signal is not deasserted when the EEE transmit controller reaches the Quiet state.
3	RW	1'h1	Rx Quiet Enable (RX_QUIET_EN): This bit controls the generation of the xpcs_lpitx_quiet_o output. When this bit is set to 1, the xpcs_lpitx_quiet_o output is set to 1 when the EEE receive controller reaches the Quiet state. When this bit set to 0, the xpcs_lpitx_quiet_o output is not set to 1.
2	RW	1'h1	Tx Quiet Enable (TX_QUIET_EN): This bit controls the generation of the xpcs_lpitx_quiet_o output. When this bit is set to 1, the xpcs_lpitx_quiet_o output is set to 1 when the EEE transmit controller reaches the Quiet state. When this bit set to 0, the xpcs_lpitx_quiet_o output is not set to 1.
1	RW	1'h0	LPI Rx Enable (LRX_EN): When set to 1, this bit enables the Energy Efficient Ethernet support in the PCS receive path. When set to 0, it disables the support for Energy Efficient Ethernet in the PCS receive path.
0	RW	1'h0	LPI Tx Enable (LTX_EN): When set to 1, this bit enables the Energy Efficient Ethernet support in the PCS Transmit path. When set to 0, it disables the support for Energy Efficient Ethernet in the PCS Transmit path.

10.3.1.36 VR MII MMD EEE Tx Timer Register (VR_MII_EEE_TXTIMER) - 1Fh, Address 8008h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8008h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:6	RO	10'h000	Reserved
5:0	RW	6'h00	TSL Resolution (TSL_RES): This field stores the resolution value for the Local Sleep Time (TSL) timer. When the generated 100ns tic timer is not exactly 100ns, this field is programmed with the required value. The programmed value is equivalent to the number of more (SIGN_BIT is low) or less (SIGN_BIT is high) counts than the ideal count to meet the range of the TSL timer. The PCS maintains the default value of the TSL timer as 199, assuming clk_eee_i_time_period * (MULT_FACT_100NS + 1) is equal to 100ns to produce 19900ns (19.9 us) as per the TSL requirement in the IEEE standard. If clk_eee_i_time_period * (MULT_FACT_100NS + 1) is 90, the default TSL timer produces 17910ns (17.91 us) which is lesser than the standard 19.9 us. To make it 19.9 us, you should program this register such that (199 +/- TSL_RES) * ((MULT_FACT_100NS + 1) * clk_eee_i_time_period) is greater than 19.9 us and less than 20.1 us (max limit), that is, (199 + TSL_RES)*90 = 19.9 us. TWL_RES = 23 meets the requirement which produces 19.98 us. The SIGN_BIT should be programmed as 1.

10.3.1.37 VR MII MMD EEE Rx Timer Register (VR_MII_EEE_RXTIMER) - 1Fh, Address 8009h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8009h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:14	RO	2'h0	Reserved
13:8	RW	6'h00	TWR Resolution (TWR_RES): This field stores the resolution value for the TWR timer. When the generated 100ns tic timer is not exactly 100ns, this field is programmed with the required value. The programmed value is equivalent to the number of more (SIGN_BIT is low) or less (SIGN_BIT is high) counts than the ideal count to meet the range of the TWR timer. The default value is 11 us for the PCS in this design. This value is as per the requirements specified in the standard assuming that clk_eee_i_time_period * (MULT_FACT_100NS + 1) produces 100ns tick.
7:0	RW	8'h00	100 us Resolution (RES_100U): This field stores the resolution value for the 100 us timer. If the generated 100ns tic timer is not exactly 100ns, this field is programmed with the required value. The programmed value is equivalent to the number of more (SIGN_BIT is low) or less (SIGN_BIT is high) counts than the ideal count to meet the range of the 100 us timer. This field is used to control the generation of 100 us time tick using the clk_eee_i clock and MULT_FACT_100NS field. By default, the 100 us timer is generated assuming clk_eee_i_time_period * (MULT_FACT_100NS + 1) is equal to 100ns. Therefore, the PCS maintains the default value of the 100 us timer as 1000 to achieve 100000ns (100 us). You should use this field if clk_eee_i_time_period * (MULT_FACT_100NS + 1) is not equal to 100ns. To program this field, use the following equation: (1000 +/- RES_100US)* ((MULT_FACT_100NS + 1) * clk_eee_i_time_period) = 100 us. The SIGN_BIT should be programmed as 1 for (+) and 0 for (-).

10.3.1.38 VR MII MMD Link Timer Control Register (VR_MII_LINK_TIMER_CTRL) - 1Fh, Address 800Ah

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 800Ah**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RW	16'h0000	Programmable Link Timer Value for Clause 37 Auto-Negotiation (CL37_LINK_TIME): This field can be programmed to desired value if application wishes to over-ride the standard specified values for Link Timer used during CL37 Auto negotiation. The PCS has a 24-bit timer that runs at the frequency of clk_xgxs_rx0_i clock. The value programmed to this field will be used as the upper 16-bit of the value to be loaded to this timer. The lower 8-bits are hardcoded as 8'h7D After programming this register, application should perform either of the following two steps, so that the new values takes effect: Set CL37_TMR_OVR_RIDE bit (bit 3) of the VR MII MMD Digital Control 1 Register to 1. FAST_SIM bit of SR Control MMD Control Register should be cleared (if already set) and then set back to 1.

10.3.1.39 VR MII MMD EEE Mode Control 1 Register (VR_MII_EEE_MCTRL1) - 1Fh, Address 800Bh

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 800Bh**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:1	RO	15'h0000	Reserved
0	RW	1'h0	Transparent Tx LPI Mode Enable (TRN_LPI): When set to 1 (along with LTX_EN=1), transparent LPI mode gets activated in the XPCS Transmit path. In this mode the transmit LPI state-machine doesn't move to the TX_QUIET state. On detecting Lower-Power Idle on the GMII Tx interface, the XPCS goes to the TX_SLEEP state and remains in this state until the MAC stops sending LPI. In this mode, the XPCS merely sends the encoded LPI pattern to the serdes. This mode does not involve gating-off of any of the clocks to the XPCS. In addition, the serdes transmitter is not disabled. The MAC should ensure that it does not gate-off the GMII Tx clock to the XPCS during this mode of operation.

10.3.1.40 VR MII MMD Digital Status Register (VR_MII_DIG_STS) - 1Fh, Address 8010h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8010h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:13	RO/V	3'h0	LPI Transmit State (LTX_STATE): This field indicates the current state of the LPI Transmit state Machine: 000: LTX_ACTIVE 001: LTX_SLEEP 010: LTX_QUIET 011: LTX_REF_WAKE 100: LTX_ALERT (does not apply to the PCS design) 101: LTX_SCR_BYP (does not apply to the PCS design)
12:10	RO/V	3'h0	LPI Receive State (LRX_STATE): This field indicates the current state of the LPI Receive State Machine: 000: LRX_ACTIVE (default) 001: LRX_SLEEP 010: LRX_QUIET 011: LRX_WAKE 100: LRX_WTF 101: LRX_LINK_FAIL 110: LRX_LPI_K
9:7	RO	3'h0	Reserved
6	RO/V	1'h0	Rx FIFO Overflow (RXFIFO_OVF): This bit indicates the clock rate compensation FIFO overflow. 0 indicates normal operation and 1 indicates FIFO overflow.
5	RO/V	1'h0	Rx FIFO Underflow (RXFIFO_UNDF): This bit indicates the clock rate compensation FIFO underflow. 0 indicates normal operation and 1 indicates FIFO underflow.
4:0	RO	5'h0	Reserved

10.3.1.41 VR MII MMD Invalid Code Group Error Count1 Register (VR_MII_ICG_ERRCNT1) - 1Fh, Address 8011h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8011h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:8	RO	8'h00	Reserved
7:0	RO/V	8'h00	Invalid Code Group Count Lane 0 (EC0): This field gives the invalid code group count in Lane 0 when bit 4 of VR MII MMD Digital Error Count Select Register is set to 1.

10.3.1.42 VR MII MMD Miscellaneous Status Register (VR_MII_MISC_STS) - 1Fh, Address 8018h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8018h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:4	RO	12'h000	Reserved
7:0	RO/V	4'h0	Bit Shift (BIT_SFT): This field indicates the number of bit-shifts carried-out by the comma-detect logic so as to align the incoming 10-bit XGXS Rx data. The default value of this field can be any value, depending on the status of comma-detect logic.

10.3.1.43 VR MII PHY Rx Lane Status Register (VR_MII_RX_LSTS) - 1Fh, Address 8020h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8020h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:13	RO/V	3'h0	DPLL Lock Status for Lanes [3:1] (RX_VALID_3_1): This field indicates that the DPLL in the PHY is locked on the serial data in the corresponding lane. xx1: Lane 1 DPLL bit locked x1x: Lane 2 DPLL bit locked 1xx: Lane 3 DPLL bit locked (x indicates don't care)
12	RO/V	1'h0	DPLL Lock Status for Lane 0 (RX_VALID_0): This field indicates that the DPLL in the PHY is locked on the serial data in Lane 0. The value 1'b1 indicates that Lane 0 DPLL bit is locked.
11:5	RO	2'h0	Reserved
4	RO/V	1'h0	Rx Signal Detect for Lane 0 (SIG_DET_0): This bit indicates that the Rx detected the signal on Lane 0. This bit is the complement value of the signals input from the PHY on Lane 0. The value 1'b1 indicates that Lane 0 signal is detected.
3:0	RO	4'h0	Reserved

10.3.1.44 VR MII MMD Digital Control2 Register (VR_MII_DIG_CTRL2) - 1Fh, Address 80E1h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 80E1h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:5	RO	11'h000	Reserved
4	RW	1'h0	Tx Polarity Invert on Lane 0 (TX_POL_INV_0): When set to 1, this bit reverses the data polarity on the Tx differential lines of Lane 0.
3:1	RO	3'h0	Reserved
0	RW	1'h0	Rx Polarity Invert on Lane 0 (ABL100T4): When set, the bits within this field indicate that the data received on Rx serial line is inverted on Lane 0. This reverses the polarity on the data received from the PHY core. The value 1 indicates that Rx data on Lane 0 is inverted.

10.3.1.45 VR MII MMD Digital Error Count Select Register (VR_MII_DIG_ERRCNT_SEL) - 1Fh, Address 80E2h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 80E2h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:5	RO	11'h000	Reserved
4	RW	1'h0	Invalid Code Group Error Counter Enable (INV_EC_EN): When this bit is set, the counting of invalid code group errors is enabled. 0: The counting of errors is disabled 1: The counting of errors is enabled For information about the fields containing the number of errors counted, see VR MII MMD Invalid Code Group Error Count1 Register.
3:1	RO	3'h0	Reserved
0	RW	1'h0	Clear on Read (COR): When this bit is set and the host reads any error counter, that counter is cleared after the read cycle. 0: Normal operation 1: Clear any error counter that is read

10.3.2 MDIO – Adhoc PHY Sublayer Registers – PHY Address 15h

The Adhoc Registers are accessible as an IEEE Std 802.3 Clause 22 capable PHY MDIO Manageable Device (MMD). Its 5-bit PHY Address (PHYAD) is 15h. Its 32 16-bit data registers are accessible using the 5-bit PHY Register Address (REGAD).

The Adhoc Registers consist of a PHY Global Configuration Register (GCR), one captured 64-bit Always Running Timer (ART) Time Stamp, one six-byte, unique MAC Address provided by the Intel product customer via the system Flash Device, and various status registers and configuration registers related to the PCH internal PHY sublayer circuitry and debug circuity.

Table 10-7. Summary of Adhoc MDIO Registers, PHYAD = 15h

Register Address (Hex)	Data Size (Bits)	Register Name (Register Symbol)	Default Value [15:0]
00h	16	Global Configuration Register (GCR)	0826h
01h	16	PMC ART Time Capture Register 0 (PMC_ART0)	0000h
02h	16	PMC ART Time Capture Register 1 (PMC_ART1)	0000h
03h	16	PMC ART Time Capture Register 2 (PMC_ART2)	0000h
04h	16	PMC ART Time Capture Register 3 (PMC_ART3)	0000h
05h	16	General Purpose Status Register 0 (GPSR0)	0000h
06h	16	General Purpose Status Register 1 (GPSR1)	0000h
07h	16	General Purpose Status Register 2 (GPSR2)	0000h
08h	16	General Purpose Status Register 3 (GPSR3)	0000h
09h	16	General Purpose Status Register 4 (GPSR4)	0000h
0Ah	16	General Purpose Status Register 5 (GPSR5)	0000h
0Bh	16	General Purpose Configuration Register 0 (GPCR0)	1020h
0Ch	16	General Purpose Configuration Register 1 (GPCR1)	0001h
0Dh	16	General Purpose Configuration Register 2 (GPCR2)	0050h
0Eh	16	General Purpose Configuration Register 3 (GPCR3)	0000h
0Fh	16	General Purpose Configuration Register 4 (GPCR4)	0000h
10h	16	General Purpose Configuration Register 5 (GPCR5)	0000h
11h	16	General Purpose Configuration Register 6 (GPCR6)	0000h
12h	16	General Purpose Configuration Register 7 (GPCR7)	0000h
13h	16	MAC Address Strap Value 0 (MACADDR0)	0000h
14h	16	MAC Address Strap Value 1 (MACADDR1)	0000h
15h	16	MAC Address Strap Value 2 (MACADDR2)	0000h
16h	16	MGBE Hammock Harbor Status (MGBE_HH_STATUS)	0000h
17h	16	MGBE RGMII DLL Status (MGBE_STATUS1)	0000h
18h	16	MGBE STATUS Register2 (MGBE_STATUS2)	0000h
19h	16	MGBE STATUS Register3 (MGBE_STATUS3)	0000h
1Ah	16	MGBE RGMII DLL Configuration Register 1 (MGBE_CONFIG1)	0000h
1Bh	16	MGBE RGMII DLL Configuration Register 2 (MGBE_CONFIG2)	0000h
1Ch	16	MGBE CONFIG Register3 (MGBE_CONFIG3)	0000h

Table 10-7. Summary of Adhoc MDIO Registers, PHYAD = 15h

Register Address (Hex)	Data Size (Bits)	Register Name (Register Symbol)	Default Value [15:0]
1Dh	16	MGBE CONFIG Register4 (MGBE_CONFIG4)	0000h
1Eh	16	MGBE CONFIG Register5 (MGBE_CONFIG5)	0000h
1Fh	16	MGBE CONFIG Register6 (MGBE_CONFIG6)	0000h

10.3.2.1 Global Configuration Register (GCR) - Address 00h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 00h**

Default: 0826h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:12	RW	4'h0	Reserved
11:8	RW	4'h8	Always Running Timer Capture Skew (ART_SKEW): The skew is provided as a number of clock cycles. Default value is 8 cycles for the 19.2-MHz ART Clock.
7	RW	1'b0	Reserved
6	RW	1'b0	PHY to MAC Interrupt Polarity (PHY2MAC_INTR_POL): When programmed to 1, the polarity of the interrupt signal that comes from an external PHY is inverted.
5	RW	1'b1	MAC Function Level Reset Enable (MAC_FLR_ENABLE): When programmed to 1, the Function Level Reset (FLR) mechanism is enabled. When programmed to 0, the FLR mechanism is disabled.
4	RW	1'b0	PHY Interface Mode Override (PHYIF_STRAPOVR): Overrides the PHY interface mode established by Soft Straps or system Fuses: 0: Override is disabled 1: Override is enabled
3	RW	1'b0	PHY Interface Mode (PHYIF_MODE): When the PHYIF_STRAPOVR bit of this register is 1, these bits determine the PHY Interface Mode as follows: 0: RGMII Mode 1: SGMII mode
2:1	RW	2'b11	Link Speed Mode (LINK_MODE): This field configures the Link-Speed Mode when the AUTONEG_DISABLE bit of this register is 1: 11: 2.5 Gbps (this is applicable only in SGMII Mode) 10: 1 Gbps 01: 100 Mbps 00: 10 Mbps
0	RW	1'b0	Auto-Negotiation Disable (AUTONEG_DISABLE): When this bit is 1, the Link Speed is determined by the LINK_MODE bits of this register instead of the PCS Auto-Negotiation value.

10.3.2.2 PMC ART Time Capture Register 0 (PMC_ART0) - Address 01h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 01h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	16'h0000	PMC ART Value 0 (PMC_ART0_FLD): Bits 15:0 of the captured 64-bit Always Running Timer (ART) from the PCH Power Management Controller.

10.3.2.3 PMC ART Time Capture Register 1 (PMC_ART1) - Address 02h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 02h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	16'h0000	PMC ART Value 1 (PMC_ART1_FLD): Bits 31:16 of the captured 64-bit Always Running Timer (ART) from the PCH Power Management Controller.

10.3.2.4 PMC ART Time Capture Register 2 (PMC_ART2) - Address 03h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 03h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	16'h0000	PMC ART Value 2 (PMC_ART2_FLD): Bits 47:32 of the captured 64-bit Always Running Timer (ART) from the PCH Power Management Controller.

10.3.2.5 PMC ART Time Capture Register 3 (PMC_ART3) - Address 04h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 04h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	16'h0000	PMC ART Value 3 (PMC_ART3_FLD): Bits 63:48 of the captured 64-bit Always Running Timer (ART) from the PCH Power Management Controller.

10.3.2.6 General Purpose Status Register 0 (GPSR0) - Address 05h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 05h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15	RO	1'b0	Reserved
14	RO/V	1'b0	RXSTANDBY_STATUS_FLD (RXSTANDBY_STATUS_FLD): Indicates the value of the fia_tsn_rxstandbystatus signal.
13	RO	1'b0	Reserved
12	RO/V	1'b0	RXELECIDLE_SUS_FLD (RXELECIDLE_SUS_FLD): Indicates the value of the fia_tsn_rxelecidle_sus signal.
11	RO/V	1'b0	PCLKIN_CHG_OK_FLD (PCLKIN_CHG_OK_FLD): Indicates the value of the fia_tsn_pclkin_chg_ok signal.
10:7	RO	3'b000	Reserved
6:4	RO/V	3'b000	POWERDOWN_SUS_FLD (POWERDOWN_SUS_FLD): Indicates the value of the tsn_fia_powerdown_sus_reg[2:0] signals.
3	RO	1'b0	Reserved
2	RO/V	1'b0	PHY_POWER_STATE_FLD (PHY_POWER_STATE_FLD): When this bit is 1, PHY is out of reset state
1	RO	1'b0	Reserved
0	RO/V	1'b0	PLL_CLK_VLD_FLD (PLL_CLK_VLD_FLD): When this bit is 1, it indicates that the PLL Clock to be used by the GBE-TSN is valid. This can either be the MODPHY SATA PLL Clock or the MIPI PLL Clock depending on the FIA lane on which the GBE-TSN is implemented.

10.3.2.7 General Purpose Status Register 1 (GPSR1) - Address 06h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 06h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO	16'h0000	Reserved

10.3.2.8 General Purpose Status Register 2 (GPSR2) - Address 07h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 07h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO	16'h0000	Reserved

10.3.2.9 General Purpose Status Register 3 (GPSR3) - Address 08h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 08h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO	16'h0000	Reserved

10.3.2.10 General Purpose Status Register 4 (GPSR4) - Address 09h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 09h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:8	RO/V	8'h00	FIA_STATUS_SEL2_FLD MGBE_MDIO (FIA_STATUS_SEL2_FLD): Various signals are multiplexed into status bits based on the bits GPCR4[13:8].
7:0	RO/V	8'h00	FIA_STATUS_SEL1_FLD MGBE_MDIO (FIA_STATUS_SEL1_FLD): Various signals are multiplexed into status bits based on the bits GPCR4[5:0].

10.3.2.11 General Purpose Status Register 5 (GPSR5) - Address 0Ah

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 0Ah**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO	16'h0000	Reserved

10.3.2.12 General Purpose Configuration Register 0 (GPCR0) - Address 0Bh

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 0Bh**

Default: 1020h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15	RO	1'b0	Reserved
14:12	RW	3'b001	MODPHY_PCLK_RATE_FLD MGBE_MDIO (MODPHY_PCLK_RATE_FLD): Destination is MODPHY signals i_pclkrate[2:0]. This determines the rate of PCLK being sent to the PHY. Used by PHY to determine PCLK:DATA Rate for TX/RX Data valid signaling. When MODPHY is in SATA Mode: 000: 37.5 MHz 001: 75 MHz (default) 010: 150 MHz 011: 300 MHz 100: 600 MHz
11	RW	1'b0	PCLKIN_CHG_ACK_FLD MGBE_MDIO (PCLKIN_CHG_ACK_FLD): Destination is MODPHY signal fia_pclkin_chg_ack.
10	RO	1'b0	Reserved
9:8	RW	2'b00	MODPHY_RATE_FLD MGBE_MDIO (MODPHY_RATE_FLD): Destination is MODPHY signals i_rate[1:0]. For SerDes Mode, the choices are: 00: PCI Express Gen 1 01: PCI Express Gen 2 10: PCI Express Gen 3 11: KX Mode, half rate for GbE (default)
7	RO	1'b0	Reserved

Bits	Access Type	Default	Field Name and Description
6:4	RW	3'b010	MODPHY_POWERDOWN_SIGNL_FLD MGBE_MDIO (MODPHY_POWERDOWN_SIGNL_FLD): Destination is MODPHY signals i_powerdown_sus[2:0]. These signals control the power management state of the MODPHY. The MODPHY Power States: 000: P0 - PHY TX is transmitting data. MAC is providing data bytes to be sent every clock cycle. PHY RX may or may not be receiving data. 001: P1 - PHY TX is not transmitting data and is in electrical idle. PHY behavior is undefined if tx_elecidle is deasserted in this state. PHY RX may or may not be receiving data. 010: P2 - PHY does a receiver detection operation. PHY behavior is undefined if tx_elecidle is deasserted in this state. 011: P3 – (default) PHY is in low power state and is in electrical idle. TX is High-Z state. 100: P4 - PHY is in low power state and is in electrical idle. TX pads sit in common mode. 101: P5 - PHY is in low power state and is in electrical idle. TX pad is in strong pull down. 110: P6 - PHY is in low power state and is in electrical idle. TX pads are in common mode with clock hub bias on. 111: Reserved.
3	RO	1'b0	Reserved
2	RW	1'b0	MODPHY_RST_DATAPATH_INT_FLD MGBE_MDIO (MODPHY_RST_DATAPATH_INT_FLD): Destination is MODPHY signal i_reset_l. Active-low reset signal for both the PIPE and SerDes interface. This signal is equivalent to a lane disable signal.
1	RO	1'b0	Reserved
0	RW	1'b0	PLL_CLK_REQUEST_FLD MGBE_MDIO (PLL_CLK_REQUEST_FLD): Depending on the PLL configuration, MIPI PLL or SATA PLL, this bit provides a signal much like mgbe_mii_refclkreq.

10.3.2.13 General Purpose Configuration Register 1 (GPCR1) - Address 0Ch

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 0Ch**

Default: 0001h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:13	RO	7'h00	Reserved
12	RW	1'b0	MODPHY_TX_DATA_SEL_FLD MGBE_MDIO (TX_DATA_SEL_FLD): Used as mux select for selecting tsn_fia_txdata[9:0], directly or bit reversed.
11	RW	1'b0	MODPHY_STATUSREG1_BIT_SEL_FLD MGBE_MDIO (STATUSREG1_BIT_SEL_FLD): Used as mux select for selecting bits of status register 1, directly or synchronized.
10:9	RO	2'b00	Reserved

Bits	Access Type	Default	Field Name and Description
8	RW	1'b0	MODPHY_TX_DET_RX_LPBK_FLD MGBE_MDIO (MODPHY_TX_DET_RX_LPBK_FLD): Destination is MODPHY signal i_txdetrxlpbk_sus. Used to tell the PHY to begin a RX detect operation or loopback to signal LFPS during MODPHY power state P0 for USB polling state. Function of this pin depends on the power state and the i_txelecidle signal.
7	RO	1'b0	Reserved
6:4	RW	3'b000	MODPHY_TX_MRGN_FLD MGBE_MDIO (MODPHY_TX_MRGN_FLD): Destination is MODPHY signals i_txmargin[2:0]. Selects the transmitter voltage levels. 000: TxMargin value 0 = ~1Vdiffp2p (Normal operating range).
3	RW	1'b0	MODPHY_TX_SWING_FLD MGBE_MDIO (TX_SWING_FLD): Drives an output signal fia_tx_swing.
2	RO	1'b0	Reserved
1:0	RW	2'b01	MODPHY_TX_DE_EMP_FLD MGBE_MDIO (MODPHY_TX_DE_EMP_FLD): General Purpose Configuration Register2[15:0]. 00: the de-emphasis is -6dB 01: the de-emphasis -3.5 dB 10: the de-emphasis 0dB 11: the de-emphasis -9.5dB

10.3.2.14 General Purpose Configuration Register 2 (GPCR2) - Address 0Dh

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 0Dh**

Default: 0050h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:9	RO	7'h00	Reserved
8	RW	1'b0	MODPHY_HALT_PHY_RDY_FLD MGBE_MDIO (HALT_PHY_RDY_FLD): additional output signal to halt xpcs_phy_rdy, in addition to powerdown state machine.
7	RO	1'b0	Reserved
6	RW	1'b1	MODPHY_RX_INTFLTREN_FLD MGBE_MDIO (RX_INTFLTREN_FLD): Drives an output signal tsn_fia_rxintfltren_l.
5	RO	1'b0	Reserved
4	RW	1'b1	MODPHY_RXTERMEN_H_AON_FLD MGBE_MDIO (MODPHY_RXTERMEN_H_AON_FLD): Destination is MODPHY signal i_rxtermen_h_aon. This signal controls the presence of the RX termination resistors. 1: Terminations are present 0: Terminations are removed from the circuit
3	RO	1'b0	Reserved

Bits	Access Type	Default	Field Name and Description
2	RW	1'b0	MODPHY_RX_SQUELCH_EN_FLD MGBE_MDIO (MODPHY_RX_SQUELCH_EN_FLD): Destination is MODPHY signal i_rxsquelchen. Used in PCIE P2/USB3 P3/ SATA Slumber power states to cycle the squelch and monitor for activity.
1	RO	1'b0	Reserved
0	RW	1'b0	MODPHY_RX_POLARITY_FLD MGBE_MDIO (MODPHY_RX_POLARITY_FLD): Destination is MODPHY signal i_rxpolarity. Configures the PHY to perform polarity inversion on the received data. 0: PHY does no polarity inversion 1: PHY does polarity inversion

10.3.2.15 General Purpose Configuration Register 3 (GPCR3) - Address 0Eh

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 0Eh**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RW	16'h0000	Reserved

10.3.2.16 General Purpose Configuration Register 4 (GPCR4) - Address 0Fh

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 0Fh**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:14	RO	2'b00	Reserved
13:8	RW	6'b000000	MODPHY_STATUS_SIGNL_SEL2_FLD MGBE_MDIO (MODPHY_STATUS_SIGNL_SEL2_FLD): Based on these bits various FIA signals are multiplexed into the GPSR4[15:8].
7:6	RO	2'b00	Reserved
5:0	RW	6'b000000	MODPHY_STATUS_SIGNL_SEL1_FLD MGBE_MDIO (MODPHY_STATUS_SIGNL_SEL1_FLD): Based on these bits various FIA signals are multiplexed into the GPSR4[7:0].

10.3.2.17 General Purpose Configuration Register 5 (GPCR5) - Address 10h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 10h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RW	16'h0000	Reserved

10.3.2.18 General Purpose Configuration Register 6 (GPCR6) - Address 11h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 11h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:6	RW	10'h000	MODPHY_FIA_OUTPUT_SEL_FLD MGBE_MDIO (MODPHY_FIA_OUTPUT_SEL_FLD): Used to replace various FIA output signals based on GPCR6[5:0] and GPCR7[5:0] bits.
5:0	RW	6'h00	MODPHY_CONFIG_SIGNL_SEL1_FLD MGBE_MDIO (MODPHY_CONFIG_SIGNL_SEL1_FLD): Selects one of 49 sets of internal signal values to be sent to the FIA and Used as MUX select for selecting values for various output FIA signals.

10.3.2.19 General Purpose Configuration Register 7 (GPCR7) - Address 12h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 12h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:6	RW	10'h000	MODPHY_TX_DATA_FLD MGBE_MDIO (TX_DATA_FLD): Used for replacing FIA Tx data, and some other FIA signals too, based on GPCR7[5:0] configuration.
5:0	RW	6'h00	MODPHY_CONFIG_SIGNL_SEL2_FLD MGBE_MDIO (MODPHY_CONFIG_SIGNL_SEL2_FLD): Used as MUX select for selecting values for various output FIA signals.

10.3.2.20 MAC Address Strap Value 0 (MACADDR0) - Address 13h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 13h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	16'h0000	MAC_ADDR_STRAP0_FLD MGBE_MDIO (MAC_ADDR_STRAP0_FLD): MAC address strap values [15:0] This is a write-only-once register, and the value is loaded on iosf2axi_fuse_valid low to high transition.

10.3.2.21 MAC Address Strap Value 1 (MACADDR1) - Address 14h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 14h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	16'h0000	MAC_ADDR_STRAP0_FLD MGBE_MDIO (MAC_ADDR_STRAP0_FLD): MAC address strap values [31:16] This is a write-only-once register, and the value is loaded on iosf2axi_fuse_valid low to high transition.

10.3.2.22 MAC Address Strap Value 2 (MACADDR2) - Address 15h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 15h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	16'h0000	MAC_ADDR_STRAP0_FLD MGBE_MDIO (MAC_ADDR_STRAP0_FLD): MAC address strap values [47:32] This is a write-only-once register, and the value is loaded on iosf2axi_fuse_valid low to high transition.

10.3.2.23 MGBE Hammock Harbor Status (MGBE_HH_STATUS) - Address 16h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 16h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:4	RO	12'h000	Reserved
3	RW	1'b0	MMGBE_SBD_SFTY_UE (MGBE_SBD_SFTY_UE): MAC Safety Uncorrectable error status: This bit is set on ac_sbd_ue_intr and cleared by software.
2	RW	1'b0	MGBE_SBD_SFTY_CE (MGBE_SBD_SFTY_CE): MAC Safety Correctable error status: This bit is set on mac_sbd_ce_intr and cleared by software.
1	RW	1'b0	MGBE_TSW_ERR (MGBE_TSW_ERROR): Timestamp error status: Iosf2axi_hh_tsw_status output from bridge latched on avail.
0	RW	1'b0	MGBE_SNAPSHOT_DONE (MGBE_SNAPSHOT_DONE): Snapshot done bit: Set when MGBE received LocalSync for tsw sync timestamp from iosf2axibr (opcode = 51). Cleared when new request gpo1 is initiated.

10.3.2.24 MGBE RGMII DLL Status (MGBE_STATUS1) - Address 17h

This Read-Only Status Register is available to subsystems that are configured to provide the RGMII rather than the PCS module as the external interface. It provides information concerning the Master/Slave DLL module used for RGMII.

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 17h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15	RO/V	1'b0	Master DLL Lock (MDLL_LOCK): Indicates that the Master DDL for RGMII is locked.
14:8	RO	7'h00	Reserved
7:4	RO/V	4'h0	Master DLL Coarse Tuning Value (MDLL_COARSE_TUNE): Indicates the value used for the Master DLL Coarse Tuning for RGMII.
3:0	RO/V	4'h0	Master DLL Fine Tuning Value (MDLL_FINE_TUNE): Indicates the value used for the Master DLL Fine Tuning for RGMII.

10.3.2.25 MGBE STATUS Register2 (MGBE_STATUS2) - Address 18h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 18h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO	16'h0000	Reserved

10.3.2.26 MGBE STATUS Register3 (MGBE_STATUS3) - Address 19h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 19h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO	16'h0000	Reserved

10.3.2.27 MGBE RGMII DLL Configuration Register 1 (MGBE_CONFIG1) - Address 1Ah

This Read-Write Configuration Register is used to configure the Master/Slave DLL module used for RGMII.

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 1Ah**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15	RW	1'b0	Override Master DLL Tuning Values (SW_OVR): 1 -> SW override is enabled. When set, the coarse and fine values to the slave DLLs will be jammed by configA register values. The master DLL coarse and fine values will be bypassed.
14	RW	1'b0	Software Reset (SW_RESETB): Active-low software reset. Resets the master DLL when asserted low.
13	RW	1'b0	MGBE_DLLRX_BYPASS (MGBE_DLLRX_BYPASS): DLL Bypass option for RGMII RX Clock.
12	RW	1'b0	MGBE_DLLTX_BYPASS (MGBE_DLLTX_BYPASS): DLL Bypass option for RGMII TX Clock.
11	RO	1'b0	Reserved
10:8	RW	3'b000	Observe Master DLL Values (MDLL_DFT): DFT inputs for observing various master DLL values.
7:4	RW	4'h0	Override Slave DLL Coarse Tuning Delay (SDLL_COARSE_OVER): Slave DLL coarse tuning delay override value used when the SW_OVR bit of this register is one.
3:0	RW	4'h0	Override Slave DLL Fine Tuning Delay (SDLL_FINE_OVER): Slave DLL fine tuning delay override value used when the SW_OVR bit of this register is one.

10.3.2.28 MGBE RGMII DLL Configuration Register 2 (MGBE_CONFIG2) - Address 1Bh

This Read-Write Configuration Register is used to configure the Master/Slave DLL module used for RGMII.

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 1Bh**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:14	RO	2'b00	Reserved
13:8	RW	6'h00	RX Slave DLL Tap Value (RX_SLAVE_TAP_VALUE): The taps are binary coded. Each tap gives 250-ps resolution. Valid values are: 6'b00_0000 -> 0 ns 6'b00_0001 -> 250 ps through… 6'b10_1000 -> 10 ns All other values are reserved.
7:6	RO	2'b00	Reserved
5:0	RW	6'h00	TX Slave DLL Tap Value (TX_SLAVE_TAP_VALUE): The taps are binary coded. Each tap gives 250 ps resolution. For example: 6'b00_0000 -> 0 ns 6'b00_0001 -> 250 ps through… 6'b10_1000 -> 10 ns All other values are reserved.

10.3.2.29 MGBE CONFIG Register3 (MGBE_CONFIG3) - Address 1Ch

This Read-Write Configuration Register is for VC1 mapping.

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 1Ch**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RW	16'h0000	VC1 Mapping Register (MGBE_CONFIG3_FLD): VC1 mapping register for 8 Tx and 8 Rx DMA channels.

10.3.2.30 MGBE CONFIG Register4 (MGBE_CONFIG4) - Address 1Dh

This Read-Write Configuration Register is reserved by Intel for possible future use.

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 1Dh**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RW	16'h0000	Reserved

10.3.2.31 MGBE CONFIG Register5 (MGBE_CONFIG5) - Address 1Eh

This Read-Write Configuration Register is reserved by Intel for possible future use.

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 1Eh**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RW	16'h0000	Reserved

10.3.2.32 MGBE CONFIG Register6 (MGBE_CONFIG6) - Address 1Fh

This Read-Write Configuration Register is reserved by Intel for possible future use.

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 1Fh**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RW	16'h0000	Reserved

10.3.3 MDIO – External PHY Sublayer Registers

The MDIO Controller provides the MDIO interface to PHY components that are external to the PCH component. Both Clause 22 capable and Clause 45 capable PHY components are supported. See IEEE Std 802.3-2015 for the MDIO interface and electrical specifications.

11 PCI Express (PCIe*)

11.1 PCIe* Configuration Registers Summary

This chapter documents the registers of the PCIe* device. The device contains multiple PCIe* controller:

- PCIe* Root Port #0 - Bus: 0, Device: 28, Function: 0
- PCIe* Root Port #1 - Bus: 0, Device: 28, Function: 1
- PCIe* Root Port #2 - Bus: 0, Device: 28, Function: 2
- PCIe* Root Port #3 - Bus: 0, Device: 28, Function: 3
- PCIe* Root Port #4 - Bus: 0, Device: 28, Function: 4
- PCIe* Root Port #5 - Bus: 0, Device: 28, Function: 5
- PCIe* Root Port #6 - Bus: 0, Device: 28, Function: 6

DID Values:

- PCIe* Root Port #0:- D28: F0 - 4B38h
- PCIe* Root Port #1:- D28: F1 - 4B39h
- PCIe* Root Port #2:- D28: F2 - 4B3Ah
- PCIe* Root Port #3:- D28: F3 - 4B3Bh
- PCIe* Root Port #4:- D28: F4 - 4B3Ch
- PCIe* Root Port #5:- D28: F5 - 4B3Dh
- PCIe* Root Port #6:- D28: F6 - 4B3Eh

Table 11-1. Summary of Bus: 0, Device: 28, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	ID	4B388086h
4h	4	Device Command And Primary Status (CMD_PSTS)	00100000h
8h	4	Revision ID And Class Code (RID_CC)	060400F0h
Ch	4	Cache Line Size, Primary Latency Timer And Header Type (CLS_PLT_HTYPE)	00810000h
18h	4	Bus Numbers And Secondary Latency Timer (BNUM_SLT)	00000000h
1Ch	4	I/O Base And Limit And Secondary Status (IOBL_SSTS)	00000000h
20h	4	Memory Base And Limit (MBL)	00000000h
24h	4	Prefetchable Memory Base And Limit (PMBL)	00010001h
28h	4	Prefetchable Memory Base Upper 32 Bits (PMBU32)	00000000h
2Ch	4	Prefetchable Memory Limit Upper 32 Bits (PMLU32)	00000000h
34h	4	Capabilities List Pointer (CAPP)	00000040h
3Ch	4	Interrupt Information And Bridge Control (INTR_BCTRL)	00000000h
40h	4	Capabilities List And PCI Express Capabilities (CLIST_XCAP)	00428010h
44h	4	Device Capabilities (DCAP)	00008001h
48h	4	Device Control And Device Status (DCTL_DSTS)	00100000h
4Ch	4	Link Capabilities (LCAP)	00710C00h
50h	4	Link Control And Link Status (LCTL_LSTS)	00010000h
54h	4	Slot Capabilities (SLCAP)	00040060h
58h	4	Slot Control And Slot Status (SLCTL_SLSTS)	00000000h
5Ch	4	Root Control (RCTL)	00000000h
60h	4	Root Status (RSTS)	00000000h
64h	4	Device Capabilities 2 (DCAP2)	00080837h
68h	4	Device Control 2 And Device Status 2 (DCTL2_DSTS2)	00000000h
6Ch	4	Link Capabilities 2 (LCAP2)	00000000h
70h	4	Link Control 2 And Link Status 2 (LCTL2_LSTS2)	00000001h
80h	4	Message Signaled Interrupt Identifiers And Message Signaled Interrupt Message Control (MID_MC)	00009005h
84h	4	Message Signaled Interrupt Message Address (MA)	00000000h
88h	4	Message Signaled Interrupt Message Data (MD)	00000000h
90h	4	Subsystem Vendor Capability (SVCAP)	0000A00Dh
94h	4	Subsystem Vendor IDs (SVID)	00000000h
A0h	4	Power Management Capability And PCI Power Management Capabilities (PMCAP_PMC)	C8030001h
A4h	4	PCI Power Management Control And Status (PMCS)	00000008h
100h	4	Advanced Error Extended Reporting Capability Header (AECH)	00000000h
104h	4	Uncorrectable Error Status (UES)	00000000h
108h	4	Uncorrectable Error Mask (UEM)	00000000h
10Ch	4	Uncorrectable Error Severity (UEV)	00060011h
110h	4	Correctable Error Status (CES)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
114h	4	Correctable Error Mask (CEM)	00002000h
118h	4	Advanced Error Capabilities And Control (AECC)	00000000h
11Ch	4	Header Log DW1 (HL_DW1)	00000000h
120h	4	Header Log DW2 (HL_DW2)	00000000h
124h	4	Header Log DW3 (HL_DW3)	00000000h
128h	4	Header Log DW4 (HL_DW4)	00000000h
12Ch	4	Root Error Command (REC)	00000000h
130h	4	Root Error Status (RES)	00000000h
134h	4	Error Source Identification (ESID)	00000000h
150h	4	PTM Extended Capability Header (PTMECH)	00000000h
154h	4	PTM Capability Register (PTMCAPR)	00000400h
158h	4	PTM Control Register (PTMCTLR)	00000000h
200h	4	L1 Sub-States Extended Capability Header (L1SECH)	00000000h
204h	4	L1 Sub-States Capabilities (L1SCAP)	0028281Fh
208h	4	L1 Sub-States Control 1 (L1SCTL1)	00000000h
20Ch	4	L1 Sub-States Control 2 (L1SCTL2)	00000028h
220h	4	ACS Extended Capability Header (ACSECH)	00000000h
224h	4	ACS Capability Register And ACS Control Register (ACSCAPR_ACSCTLR)	0000001Fh
A00h	4	DPC Extended Capability Header (DPCECH)	00000000h
A04h	4	DPC Capability Register And DPC Control Register (DPCCAPR_DPCCTLR)	000014E0h
A08h	4	DPC Status Register And DPC Error Source ID Register (DPCSR_DPCESIDR)	00001F00h
A0Ch	4	RP PIO Status Register (RPPIOSR)	00000000h
A10h	4	RP PIO Mask Register (RPPIOMR)	00070707h
A14h	4	RP PIO Severity Register (RPPIOVR)	00000000h
A18h	4	RP PIO SysError Register (RPPIOSER)	00000000h
A1Ch	4	RP PIO Exception Register (RPPIOER)	00000000h
A20h	4	RP PIO Header Log Register DW1 (RPPIOHLR_DW1)	00000000h
A24h	4	RP PIO Header Log Register DW2 (RPPIOHLR_DW2)	00000000h
A28h	4	RP PIO Header Log Register DW3 (RPPIOHLR_DW3)	00000000h
A2Ch	4	RP PIO Header Log Register DW4 (RPPIOHLR_DW4)	00000000h
A30h	4	Secondary PCI Express Extended Capability Header (SPEECH)	00000000h
A34h	4	Link Control 3 (LCTL3)	00000000h
A38h	4	Lane Error Status (LES)	00000000h
A3Ch	4	Lane 0 And Lane 1 Equalization Control (L01EC)	7F7F7F7Fh
A40h	4	Lane 2 And Lane 3 Equalization Control (L23EC)	7F7F7F7Fh

11.1.1 ID - Offset 0h

This is Identifiers register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 0h	4B388086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4B38h RO/V	**Device Identification (DID):** See the Device ID table in the SoC documentation Note: DID[lb]15:7[rb] are received through ID Broadcast and DID[lb]6:0[rb] are received through Fuse Pull.
15:0	8086h RO	**Vendor Identification (VID):** Indicates Intel

11.1.2 Device Command And Primary Status (CMD_PSTS) - Offset 4h

This is Device Command and Primary Status register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**DPE - Detected Parity Error (DPE):** Set when the root port receives a command or data from the backbone with a parity error. This is set even if PCMD.PERE is not set.
30	0h RW/1C/V	**Signaled System Error (SSE):** Set when the root port signals a system error to the internal SERR# logic.
29	0h RW/1C/V	**Received Master Abort (RMA):** Set when the root port receives a completion with unsupported request status from the backbone.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the root port receives a completion with completer abort from the backbone.
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set whenever the root port forwards a target abort received from the downstream device onto the backbone.
26:25	0h RO	**Primary DEVSEL# Timing Status (PDTS):** Reserved
24	0h RW/1C/V	**Master Data Parity Error Detected (DPD):** Set when the root port receives a completion with a data parity error on the backbone and PCMD.PERE is set.
23	0h RO	**Primary Fast Back to Back Capable (PFBC):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
22	0h RO	**Reserved**
21	0h RO	**Primary 66 MHz Capable (PC66):** Reserved
20	1h RO	**Capabilities List (CLIST):** Indicates the presence of a capabilities list.
19	0h RO/V	**Interrupt Status (IS):** Indicates status of hot plug and power management interrupts on the root port that result in INTx# message generation. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of CMD.ID.
18:11	0h RO	**Reserved**
10	0h RW/V2	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts on enabled hot plug and power management events. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt for hot plug or power management and MSI is not enabled. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RO and returns a value of 0 when read, else it is RW with the functionality described above.
9	0h RO	**Fast Back to Back Enable (FBE):** Reserved
8	0h RW	**SERR# Enable (SEE):** When set, enables the root port to generate an SERR# message when PSTS.SSE is set.
7	0h RO	**Wait Cycle Control (WCC):** Reserved
6	0h RW	**Parity Error Response Enable (PERE):** Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	0h RO	**VGA Palette Snoop (VGA_PSE):** Reserved
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** Reserved
3	0h RO	**Special Cycle Enable (SCE):** Reserved
2	0h RW	**Bus Master Enable (BME):** When set, allows the root port to forward Memory and I/O Read/Write cycles onto the backbone from a PCI-Express device. When this bit is 0b, Memory and I/O request received at a Root Port must be handled as Unsupported Requests (UR). This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O requests is not controlled by this bit.
1	0h RW	**Memory Space Enable (MSE):** When set, memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI-Express device. When cleared, these memory cycles are master aborted on the backbone.
0	0h RW	**I/O Space Enable (IOSE):** When set, I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI-Express device. When cleared, these cycles are master aborted on the backbone..

11.1.3 Revision ID And Class Code (RID_CC) - Offset 8h

This is Revision ID and Class Code register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 8h	060400F0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	06h RO	**Base Class Code (BCC):** Indicates the device is a bridge device.
23:16	04h RO/V	**Sub-Class Code (SCC):** The default indicates the device is a PCI-to-PCI bridge. If the MPC.Bridge Type register is set to a '1' for a Host Bridge, this register reads 00h.
15:8	00h RO/V	**Programming Interface (PI):** PCI-to-PCI bridge.
7:0	F0h RO/V	**Revision ID (RID):** Indicates the revision of the bridge. The upper nibble, RID[lb]7:4[rb] of this register is hard wired to 4'hF. The lower nibble, RID[lb]3:0[rb] of this register tracks the Revision ID of the SoC

11.1.4 Cache Line Size, Primary Latency Timer And Header Type (CLS_PLT_HTYPE) - Offset Ch

This is Cache Line Size, Primary Latency Timer and Header Type register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + Ch	00810000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	1h RO	**Multi-function Device (MFD):** This bit is '1' to indicate a multi-function device.
22:16	01h RO/V	**Header Type (HTYPE):** The default mode identifies the header layout of the configuration space, which is a PCI-to-PCI bridge. If the MPC.Bridge Type register is set to a '1' for a Host Bridge, this register reads 00h.
15:11	00h RO	**Latency Count (CT):** Reserved
10:8	0h RO	**Reserved**
7:0	00h RW	**Line Size (LS):** This is read/write but contains no functionality, per PCI-Express spec

11.1.5 Bus Numbers And Secondary Latency Timer (BNUM_SLT) - Offset 18h

This is Bus Numbers and Secondary Latency Timer register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW/V2	**Secondary Latency Timer (SLT):** For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is a RW register; else this register is RO and returns 0. This register does not affect the behavior of any HW logic.
23:16	00h RW	**Subordinate Bus Number (SBBN):** Indicates the highest PCI bus number below the bridge.
15:8	00h RW	**Secondary Bus Number (SCBN):** Indicates the bus number the port.
7:0	00h RW	**Primary Bus Number (PBN):** Indicates the bus number of the backbone.

11.1.6 I/O Base And Limit And Secondary Status (IOBL_SSTS) - Offset 1Ch

This is I/O Base and Limit and Secondary Status register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the port receives a poisoned TLP.
30	0h RW/1C/V	**Received System Error (RSE):** Set when the port receives an ERR_FATAL or ERR_NONFATAL message from the device.
29	0h RW/1C/V	**Received Master Abort (RMA):** Set when the port receives a completion with *"Unsupported Request"* status to the device.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the port receives a completion with *"Completion Abort"* status to the device.
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set when the port generates a completion with *"Completion Abort"* status to the device.
26:25	0h RO/V	**Secondary DEVSEL# Timing Status (SDTS):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW/1C/V	**Data Parity Error Detected (DPD):** Set when the BCTRL.PERE, and either of the following two conditions occurs: Port receives completion marked poisoned. Port poisons a write request to the secondary side.
23	0h RO/V	**Secondary Fast Back to Back Capable (SFBC):** Reserved
22	0h RO	**Reserved**
21	0h RO	**Secondary 66 MHz Capable (SC66):** Reserved
20:16	0h RO	**Reserved**
15:12	0h RW	**I/O Address Limit (IOLA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	0h RO	**I/O Limit Address Capability (IOLC):** Indicates that the bridge does not support 32-bit I/O addressing.
7:4	0h RW	**I/O Base Address (IOBA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	0h RO	**I/O Base Address Capability (IOBC):** Indicates that the bridge does not support 32-bit I/O addressing.

11.1.7 Memory Base And Limit (MBL) - Offset 20h

Accesses that are within the ranges specified in this register will be sent to the attached device if CMD.MSE is set. Accesses from the attached device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is MB [gt]= AD[lb]31:20[rb] [lt]= ML.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW	**Memory Limit (ML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	0h RO	**Reserved**
15:4	000h RW	**Memory Base (MB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	0h RO	**Reserved**

11.1.8 Prefetchable Memory Base And Limit (PMBL) - Offset 24h

Accesses that are within the ranges specified in this register will be sent to the device if CMD.MSE is set. Accesses from the device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is PMBU32:PMB [gt]= AD[lb]63:32[rb]:AD[lb]31:20[rb] [lt]= PMLU32:PML.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 24h	00010001h

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW	**Prefetchable Memory Limit (PML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	1h RO	**64-bit Indicator (I64L):** Indicates support for 64-bit addressing.
15:4	000h RW	**Prefetchable Memory Base (PMB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	1h RO	**64-bit Indicator (I64B):** Indicates support for 64-bit addressing.

11.1.9 Prefetchable Memory Base Upper 32 Bits (PMBU32) - Offset 28h

Size: 32 bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 28h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Prefetchable Memory Base Upper Portion (PMBU):** Upper 32-bits of the prefetchable address base.

11.1.10 Prefetchable Memory Limit Upper 32 Bits (PMLU32) - Offset 2Ch

Size: 32 bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Prefetchable Memory Limit Upper Portion (PMLU):** Upper 32-bits of the prefetchable address limit.

11.1.11 Capabilities List Pointer (CAPP) - Offset 34h

This is Capabilities List Pointer register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 34h	00000040h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	40h RW/O	**Capabilities Pointer (PTR):** Indicates that the pointer for the first entry in the capabilities list. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. Capability Linked List (Default Settings) Offset Capability Next Pointer 40h PCI Express 80h 80h Message Signaled Interrupt (MSI)90h 90h Subsystem Vendor A0h PCI Power Management 00h Extended PCIe Capability Linked List Offset Capability Next Pointer 100h Advanced Error Reporting 000h

11.1.12 Interrupt Information And Bridge Control (INTR_BCTRL) - Offset 3Ch

This is Interrupt Information and Bridge Control register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RW/V2	**Discard Timer SERR# Enable (DTSE):** Reserved
26	0h RO	**Discard Timer Status (DTS):** Reserved
25	0h RW/V2	**Secondary Discard Timer (SDT):** Reserved
24	0h RW/V2	**Primary Discard Timer (PDT):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**Fast Back to Back Enable (FBE):** Reserved
22	0h RW	**Secondary Bus Reset (SBR):** Triggers a Hot Reset on the PCI-Express port.
21	0h RW/V2	**Master Abort Mode (MAM):** Reserved
20	0h RW	**VGA 16-Bit Decode (V16):** When set, indicates that the I/O aliases of the VGA range (see BCTRL:VE definition below), are not enabled. 0: Execute 10-bit address decode on VGA I/O accesses. 1: Execute 16-bit address decode on VGA I/O accesses.
19	0h RW	**VGA Enable (VE):** When set, the following ranges will be claimed off the backbone by the root port: Memory ranges A0000h-BFFFFh I/O ranges 3B0h 3BBh and 3C0h 3DFh, and all aliases of bits 15:10 in any combination of 1's
18	0h RW	**ISA Enable (IE):** This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64KB of PCI I/O space. If this bit is set, the root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1KB block (offsets 100h to 3FFh).
17	0h RW	**SERR# Enable (SE):** When set, ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone. When cleared, they are not.
16	0h RW	**Parity Error Response Enable (PERE):** When set, poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD.
15:8	00h RO/V	**Interrupt Pin (IPIN):** Indicates the interrupt pin driven by the root port. At reset, this register takes on the following values, which reflect the reset state of the STRPFUSECFG.PxIP field: Port Bits[lb]15:12[rb] Bits[lb]11:08[rb] 1 0h STRPFUSECFG.P1IP 2 0h STRPFUSECFG.P2IP 3 0h STRPFUSECFG.P3IP 4 0h STRPFUSECFG.P4IP 5 0h STRPFUSECFG.P5IP 6 0h STRPFUSECFG.P6IP 7 0h STRPFUSECFG.P7IP 8 0h STRPFUSECFG.P8IP: : x ohSTRPFUSECFG.PxIP The value that is programmed into STRPFUSECFG.PxIP is always reflected in this register. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 00h when read, else this register returns the value from the table above. Note: Depending on the platform, the number of Root Ports supported may vary. In this case, the encodings defined in this register will be scaled accordingly.
7:0	00h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

11.1.13 Capabilities List And PCI Express Capabilities (CLIST_XCAP) - Offset 40h

This is Capabilities List and PCI Express Capabilities register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 40h	00428010h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:25	00h RO	**Interrupt Message Number (IMN):** The Root Port does not have multiple MSI interrupt numbers.
24	0h RW/O	**Slot Implemented (SI):** Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset.
23:20	4h RO	**Device / Port Type (DT):** Indicates this is a PCI-Express root port
19:16	2h RO	**Capability Version (CV):** Version 2.0 indicates devices compliant to the PCI Express 2.0 and 3.0 specification which incorporates the Register Expansion ECN.
15:8	80h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability. The default value of this register is 80h which points to the MSI Capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	10h RO	**Capability ID (CID):** Indicates this is a PCI Express capability

11.1.14 Device Capabilities (DCAP) - Offset 44h

This is Device Capabilities register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 44h	00008001h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RO	**Function Level Reset Capable (FLRC):** Not supported in Root Ports
27:26	0h RO	**Captured Slot Power Limit Scale (CSPS):** Not supported
25:18	00h RO	**Captured Slot Power Limit Value (CSPV):** Not supported
17:16	0h RO	**Reserved**
15	1h RO	**Role Based Error Reporting (RBER):** Indicates that this device implements the functionality defined in the Error Reporting ECN as required by the PCI Express 1.1 spec.
14:12	0h RO	**Reserved**
11:9	0h RO	**Endpoint L1 Acceptable Latency (E1AL):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
8:6	0h RO	**Endpoint L0 Acceptable Latency (E0AL):** Reserved
5	0h RO	**Extended Tag Field Supported (ETFS):** The Root Port never needs to initiate a transaction as a Requester with the Extended Tag bits being set. This bit does not affect the root port's ability to forward requests as a bridge as the root port always supports forwarding requests with extended tags.
4:3	0h RO	**Phantom Functions Supported (PFS):** No phantom functions supported
2:0	1h RW/O	**Max Payload Size Supported (MPS):** BIOS should write to this field during system initialization. Max Payload Size of up to 256B is supported. Programming this field to any values other than 128B or 256B max payload size will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. A separate register is defined for the IOSF interface. Register Attribute: Static

11.1.15 Device Control And Device Status (DCTL_DSTS) - Offset 48h

This is Device Control and Device Status register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 48h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RO	**Transactions Pending (TDP):** This bit has no meaning for the root port since it never initiates a non-posted request with its own Requester ID.
20	1h RO	**AUX Power Detected (APD):** The root port contains AUX power for wakeup
19	0h RW/1C/V	**Unsupported Request Detected (URD):** Indicates an unsupported request was detected.
18	0h RW/1C/V	**Fatal Error Detected (FED):** Indicates a fatal error was detected. Set when a fatal error occurred on from a data link protocol error, buffer overflow, or malformed tlp
17	0h RW/1C/V	**Non-Fatal Error Detected (NFED):** Indicates a non-fatal error was detected. Set when a received a non-fatal error occurred from a poisoned tlp, unexpected completions, unsupported requests, completer abort, or completer timeout
16	0h RW/1C/V	**Correctable Error Detected (CED):** Indicates a correctable error was detected. Set when received an internal correctable error from receiver errors / framing errors, tlp crc error, dllp crc error, replay num rollover, replay timeout.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14:12	0h RO	**Max Read Request Size (MRRS):** Hardwired to 0. This field applies only to the PCIe link interface. A separate register is defined for the IOSF interface.
11	0h RO	**Enable No Snoop (ENS):** Not supported. The root port will never issue non-snoop requests.
10	0h RW/P	**Aux Power PM Enable (APME):** Must be RW for OS testing. The OS will set this bit to '1' if the device connected has detected aux power. It has no effect on the root port otherwise.
9	0h RO	**Phantom Functions Enable (PFE):** Not supported
8	0h RO	**Extended Tag Field Enable (ETFE):** Not supported
7:5	0h RW	**Max Payload Size (MPS):** The root port only supports up to 256B max payload. Programming this field to any values greater than DCAP.MPS will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. A separate register is defined for the IOSF interface.Note: Software should ensure that the system is quiescent and no TLP is in progress prior to changing this field. BIOS should program this field prior to enabling BME. Register Attribute: Static.
4	0h RO	**Enable Relaxed Ordering (ERO):** Not supported
3	0h RW	**Unsupported Request Reporting Enable (URE):** When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when an unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register.
2	0h RW	**Fatal Error Reporting Enable (FEE):** Enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	0h RW	**Non-Fatal Error Reporting Enable (NFE):** When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	0h RW	**Correctable Error Reporting Enable (CEE):** When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

11.1.16 Link Capabilities (LCAP) - Offset 4Ch

This is Link Capabilities register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 4Ch	00710C00h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO/V	**Port Number (PN):** Indicates the port number for the root port. This value is different for each implemented port: Port # Value of PN field 1 01h 2 02h 3 03h 4 04h: : x 0Xh Note: Depending on the platform, the number of Root Ports supported may vary. In this case, the encodings defined in this register will be scaled accordingly.
23	0h RO	**Reserved**
22	1h RW/O	**ASPM Optionality Compliance (ASPMOC):** ASPM Optionality Compliance (ASPMOC): This bit must be set to 1b for PCIe 3.0 compliant port. Components implemented against certain earlier versions of this specification will have this bit set to 0b. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests.
21	1h RO	**Link Bandwidth Notification Capability (LBNC):** This port supports Link Bandwidth Notification status and interrupt mechanisms.
20	1h RO	**Link Active Reporting Capable (LARC):** This port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine.
19	0h RO	**Surprise Down Error Reporting Capable (SDERC):** Set to '0' to indicate the Root Port does not support Surprise Down Error Reporting
18	0h RO	**Clock Power Management (CPM):** '0' Indicates that root ports do not support the CLKREQ# mechanism.
17:15	2h RW/O	**L1 Exit Latency (EL1):** Indicates an exit latency of 2us to 4us. 000b Less than 1 us 001b 1 us to less than 2 us 010b 2 us to less than 4 us 011b 4 us to less than 8 us 100b 8 us to less than 16 us 101b 16 us to less than 32 us 110b 32 us to 64 us 111b More than 64 us Note: If PXP PLL shutdown is enabled, BIOS should program this latency to comprehend PLL lock latency.
14:12	0h RO/V	**L0s Exit Latency (EL0):** Indicates an exit latency based upon common-clock configuration: LCTL.CCC Value 0 MPC.UCEL 1 MPC.CCEL
11:10	3h RW/O	**Active State Link PM Support (APMS):** Indicates the level of active state power management on this link Bits Definition 00 No ASPM Supported 01 L0s Supported 10 L1 Supported 11 L0s and L1 supported Note: If STRPFUSECFG.ASPMDIS is 1, the default of this field is *"01"*. Otherwise, the default of this field is *"11"*. If STRPFUSECFG.ASPMDIS is 1, BIOS writing *"11"* to this field will have the same effect as writing *"01"*. *"01"* will be reflected on this register when read the register will turn to Read-Only once written.

<table>
<tr><th>Bit Range</th><th>Default & Access</th><th>Field Name (ID): Description</th></tr>
<tr><td>9:4</td><td>00h
RO/V</td><td>Maximum Link Width (MLW):
For the root ports, several values can be taken, based upon the soft strap port configuration for PCIe Controller 0:
<table>
<tr><th rowspan="2">Port Number (PN)</th><th colspan="4">Soft Strap Port Configuration</th></tr>
<tr><th>4x1</th><th>1x2, 2x1</th><th>2x2</th><th>1x4</th></tr>
<tr><td>1</td><td>01h</td><td>02h</td><td>02h</td><td>04h</td></tr>
<tr><td>2</td><td>01h</td><td>01h</td><td>01h</td><td>01h</td></tr>
<tr><td>3</td><td>01h</td><td>01h</td><td>02h</td><td>01h</td></tr>
<tr><td>4</td><td>01h</td><td>01h</td><td>01h</td><td>01h</td></tr>
<tr><td colspan="5">Note: For PCIe Controller 1:3, MLW will have a value of 02h irrespective of the soft strap port configuration.</td></tr>
</table></td></tr>
<tr><td>3:0</td><td>0h
RO/V</td><td>Max Link Speeds (MLS):
This field indicates the maximum Link speed of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed. Defined encodings are: “0001b”: Supported Link Speeds Vector field bit 0. “0010b”: Supported Link Speeds Vector field bit 1. “0011b”: Supported Link Speeds Vector field bit 2. “0100b”: Supported Link Speeds Vector field bit 3. “0101b”: Supported Link Speeds Vector field bit 4. “0110b”: Supported Link Speeds Vector field bit 5. “0111b”: Supported Link Speeds Vector field bit 6. All other encodings are reserved. When operating as PCI Express: This field reports a value of 0001b if GEN1 data rate is supported but both GEN 2 and GEN3 data rate support are disabled through PCI Express Speed Limit Fuse or MPC.PCIESD register. This field reports a value of 0010b if both GEN1 and GEN2 data rate are supported but GEN3 data rate support is disabled through PCI Express Speed Limit Fuse or MPC.PCIESD register. Otherwise, this field reports a value of 0011b. Register Attribute: Static.</td></tr>
</table>

11.1.17 Link Control And Link Status (LCTL_LSTS) - Offset 50h

This is Link Control and Link Status register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 50h	00010000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Link Autonomous Bandwidth Status (LABS):** This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The default value of this bit is 0b.
30	0h RW/1C/V	**Link Bandwidth Management Status (LBMS):** This bit is Set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: - A Link retraining has completed following a write of 1b to the Retrain Link bit Note: This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. - Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. The default value of this bit is 0b.
29	0h RO/V	**Link Active (LA):** Set to 1b when the Data Link Control and Management State Machine is in the DL_Active state, 0b otherwise.
28	0h RO/V	**Slot Clock Configuration (SCC):** In normal mode, root port uses the same reference clock as on the platform and does not generate its own clock. Note: When operating in PCI Express mode, the default of this register bit is dependent on the *"PCIe Non-Common Clock With SSC Mode Enable Strap"*. If the strap enables non-common clock with SSC support, this bit shall default to '0'. Otherwise, this bit shall default to '1'.
27	0h RO/V	**Link Training (LT):** The root port sets this bit whenever link training is occurring, or that 1b was written to the Retrain Link bit but Link training has not yet begun. It clears the bit upon completion of link training.
26	0h RO	**Reserved**
25:20	00h RO/V	**Negotiated Link Width (NLW):** For the root ports, this register could take on several values: Port # Value of PN field RPC 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h. The value of this register is undefined if the link has not successfully trained.
19:16	1h RO/V	**Current Link Speed (CLS):** 0001b Link is 2.5Gb/s Link 0010b 5.0 GT/s Link. This field indicates the negotiated Link speed of the given link. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. The value of this field is undefined if the link is not up. Register Attribute: Static
15:12	0h RO	**Reserved**
11	0h RW	**Link Autonomous Bandwidth Interrupt Enable (LABIE):** Link Autonomous Bandwidth Interrupt Enable - When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**Link Bandwidth Management Interrupt Enable (LBMIE):** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. Functions that do not implement the Link Bandwidth Notification Capability must hardwire this bit to 0b. Default value of this bit is 0b.
9	0h RW	**Hardware Autonomous Width Disable (HAWD):** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Default value of this bit is 0b. Note: When operating as PCI Express, this bit defines the value of the Link Up configure Capability in TS2 Ordered Sets.
8	0h RO	**Enable Clock Power Management (ECPM):** Reserved
7	0h RW	**Extended Synch (ES):** When set, forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0. Note: This functionality is not applicable for Mobile Express.
6	0h RW	**Common Clock Configuration (CCC):** When set, indicates that the Root Port and device are operating with a distributed common reference clock.
5	0h WO	**Retrain Link (RL):** When set, the root port will train its downstream link. This bit always returns '0' when read. Software uses LSTS.LT and LSTS.LTE to check the status of training. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress.
4	0h RW	**Link Disable (LD):** When set, the root port will disable the link by directing the LTSSM to the Disabled state.
3	0h RW/O	**Read Completion Boundary Control (RCBC):** Indicates the read completion boundary is 64 bytes.
2	0h RO	**Reserved**
1:0	0h RW	**Active State Link PM Control (ASPM):** Indicates whether the root port should enter L0s or L1 or both. Bits Definition 00 Disabled 01 L0s Entry Enabled 10 L1 Entry Enabled 11 L0s and L1 Entry Enabled The value of this register is used unless the Root Port ASPM Control Override Enable register is set, in which case the Root Port ASPM Control Override value is used. Note: If STRPFUSECFG.ASPMDIS is '1', hardware will always see *"00"* as an output from this register. BIOS reading this register should always return the correct value.

11.1.18 Slot Capabilities (SLCAP) - Offset 54h

This is Slot Capabilities register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 54h	00040060h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW/O	**Physical Slot Number (PSN__31_24):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
23:19	00h RW/O	**Physical Slot Number (PSN__23_19):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
18	1h RO	**No Command Completed Support (NCCS):** Set to '1' as this port does not implement a Hot Plug controller and can handle back-2-back writes to all fields of the slot control register without delay between successive writes.
17	0h RO	**Electromechanical Interlock Present (EMIP):** Set to 0 to indicate that no electro-mechanical interlock is implemented.
16:15	0h RW/O	**Slot Power Limit Scale (SLS):** Specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset.
14:8	00h RW/O	**Slot Power Limit Value (SLV__14_8):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
7	0h RW/O	**Slot Power Limit Value (SLV__7_7):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
6	1h RW/O	**Hot Plug Capable (HPC):** When set, Indicates that hot plug is supported.
5	1h RW/O	**Hot Plug Surprise (HPS):** When set, indicates the device may be removed from the slot without prior notification.
4	0h RO	**Power Indicator Present (PIP):** Indicates that a power indicator LED is not present for this slot.
3	0h RO	**Attention Indicator Present (AIP):** Indicates that an attention indicator LED is not present for this slot.
2	0h RO	**MRL Sensor Present (MSP):** Indicates that an MRL sensor is not present
1	0h RO	**Power Controller Present (PCP):** Indicates that a power controller is not implemented for this slot
0	0h RO	**Attention Button Present (ABP):** Indicates that an attention button is not implemented for this slot.

11.1.19 Slot Control And Slot Status (SLCTL_SLSTS) - Offset 58h

This is Slot Control and Slot Status register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW/1C/V	**Data Link Layer State Changed (DLLSC):** This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device.
23	0h RO	**Electromechanical Interlock Status (EMIS):** Reserved
22	0h RO/V	**Presence Detect State (PDS):** If XCAP.SI is set (indicating that this root port spawns a slot), then this bit indicates whether a device is connected ('1') or empty ('0'). If XCAP.SI is cleared, this bit is a '1'.
21	0h RO	**MRL Sensor State (MS):** Reserved
20	0h RO	**Command Completed (CC):** This register is RO as this port does not implement a Hot Plug Controller..
19	0h RW/1C/V	**Presence Detect Changed (PDC):** This bit is set by the root port when the PDS bit changes state.
18	0h RO	**MRL Sensor Changed (MSC):** Reserved
17	0h RO	**Power Fault Detected (PFD):** Reserved
16	0h RO	**Attention Button Pressed (ABP):** This register is RO as this port does not implement an attention button
15:14	0h RO	**Reserved**
13	0h RW	**Auto Slot Power Limit Disable (ASPLD):** When set, this bit disables automatic sending of Set_Slot_Power_Limit message when the link transitions from non-DL_Up status to DL_Up status. Register Attribute: Dynamic.
12	0h RW	**Data Link Layer State Changed Enable (DLLSCE):** When set, this field enables generation of a hot plug interrupt when the Data Link Layer Link Active field is changed
11	0h RO	**Electromechanical Interlock Control (EMIC):** Reserved
10	0h RO	**Power Controller Control (PCC):** This bit has no meaning for module based hot plug.
9:8	0h RO	**Power Indicator Control (PIC):** This register is RO as this port does not implement a Hot Plug Controller..
7:6	0h RO	**Attention Indicator Control (AIC):** This register is RO as this port does not implement a Hot Plug Controller..
5	0h RW	**Hot Plug Interrupt Enable (HPE):** When set, enables generation of a hot plug interrupt on enabled hot plug events.
4	0h RO	**Command Completed Interrupt Enable (CCE):** This register is RO as this port does not implement a Hot Plug Controller..

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Presence Detect Changed Enable (PDE):** When set, enables the generation of a hot plug interrupt or wake message when the presence detects logic changes state.
2	0h RO	**MRL Sensor Changed Enable (MSE):** This register is RO as this port does not implement a Hot Plug Controller.
1	0h RO	**Power Fault Detected Enable (PFE):** This register is RO as this port does not implement a Hot Plug Controller.
0	0h RO	**Attention Button Pressed Enable (ABE):** This register is RO as this port does not implement a Hot Plug Controller.

11.1.20 Root Control (RCTL) - Offset 5Ch

This is Root Control register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 5Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**PME Interrupt Enable (PIE):** When set, enables interrupt generation when RSTS.PS is in a set state (either due to a '0' to '1' transition, or due to this bit being set with RSTS.PS already set).
2	0h RW	**System Error on Fatal Error Enable (SFE):** When set, an SERR# will be generated if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port. This register is not dependent on CMD.SEE being set.
1	0h RW	**System Error on Non-Fatal Error Enable (SNE):** When set, an SERR# will be generated if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port. This register is not dependent on CMD.SEE being set.
0	0h RW	**System Error on Correctable Error Enable (SCE):** When set, an SERR# will be generated if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port. This register is not dependent on CMD.SEE being set.

11.1.21 Root Status (RSTS) - Offset 60h

This is Root Status register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RO/V	**PME Pending (PP):** Indicates another PME is pending when the PME status bit is set. When the original PME is cleared by software, it will be set again, the requestor ID will be updated, and this bit will be cleared. Root ports have a one deep PME pending queue.
16	0h RW/1C/V	**PME Status (PS):** Indicates that PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared.
15:0	0000h RO/V	**PME Requestor ID (RID):** Indicates the PCI requestor ID of the last PME requestor. Valid only when PS is set. Root ports are capable of storing the requester ID for two PM_PME messages, with one active (this register) and a one deep pending queue. Subsequent PM_PME messages will be dropped.

11.1.22 Device Capabilities 2 (DCAP2) - Offset 64h

This is Device Capabilities 2 register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 64h	00080837h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:18	2h RW/O	**Optimized Buffer Flush/Fill Supported (OBFFS):** 00b - OBFF is not supported. 01b - OBFF is supported using Message signaling only. 10b - OBFF is supported using WAKE# signaling only. 11b - OBFF is supported using WAKE# and Message signaling. BIOS should program this field to 00b or 10b during system initialization to advertise the level of hardware OBFF support to software. BIOS should never program this field to 01b or 11b since OBFF messaging is not supported. Note: OBFF is not supported. BIOS should program this field to *"00b"*.
17:12	0h RO	**Reserved**
11	1h RW/O	**LTR Mechanism Supported (LTRMS):** A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. BIOS must write to this register with either a '1' or a '0' to enable/disable the root port from declaring support for the LTR capability.
10:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5	1h RO	**ARI Forwarding Supported (AFS):** ARI Forwarding Supported (AFS): Applicable only to Switch Downstream Ports and Root Ports; must be 0b for other Function types. This bit must be set to 1b if a Switch Downstream Port or Root Port supports this optional capability. Note: This bit is not made RWO to simplify implementation, since there is a requirement that the ARI Forwarding Enable bit must be hardwired to 0b if ARI Forwarding Supported bit is 0b. It is low risk to keep this risk 1b. Register Attribute: Static.
4	1h RO	**Completion Timeout Disable Supported (CTDS):** A value of 1b indicates support for the Completion Timeout Disable mechanism.
3:0	7h RO	**Completion Timeout Ranges Supported (CTRS):** This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50us to 10ms Range B: 10ms to 250ms Range C: 250ms to 4s Range D: 4s to 64s Bits are set according to the table below to show timeout value ranges supported. 0000b Completion Timeout programming not supported. 0001b Range A 0010b Range B 0011b Ranges A [amp] B 0110b Ranges B [amp] C 0111b Ranges A, B [amp] C [lt]-- This is what PCH supports 1110b Ranges B, C [amp] D 1111b Ranges A, B, C [amp] D All other values are reserved.

11.1.23 Device Control 2 And Device Status 2 (DCTL2_DSTS2) - Offset 68h

This is Device Control 2 and Device Status 2 register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14:13	0h RW	**Optimized Buffer Flush/Fill Enable (OBFFEN):** 00b Disable OBFF mechanism. 01b Enable OBFF mechanism using Message signaling (Variation A). 10b Enable OBFF mechanism using Message signaling (Variation B). 11b Enable OBFF using WAKE# signaling. Note: Only encoding 00b and 11b are supported. The encoding of 01b or 10b would be aliased to 00b. If DCAP2.OBFFS is clear, programming this field to any non-zero values will have no effect.
12:11	0h RO	**Reserved**
10	0h RW	**LTR Mechanism Enable (LTREN):** When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. If DCAP2.LTRMS is clear, programming this field to any non-zero values will have no effect.
9:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**ARI Forwarding Enable (AFE):** ARI Forwarding Enable (AFE): When set, the Downstream Port disables its traditional Device Number field being 0b enforcement when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port. Register Attribute: Dynamic.
4	0h RW	**Completion Timeout Disable (CTD):** When set to 1b, this bit disables the Completion Timeout mechanism. This field is required for all devices that support the Completion Timeout Disable Capability. Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued.
3:0	0h RW	**Completion Timeout Value (CTV):** In Devices that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. A Device that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50us to 50ms. Devices that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Values Supported field. The root port targeted configurable ranges are listed below, along with the range allowed by the PCI Express 2.0 specification. Defined encodings: 0000b Default range: 40-50ms (spec range 50us to 50ms) Values available if Range A (50us to 10 ms) programmability range is supported: 0001b 90-100us (spec range is 50 us to 100 us) 0010b 9-10ms (spec range is 1ms to 10 ms) Values available if Range B (10ms to 250ms) programmability range is supported: 0101b 40-50ms (spec range is 16ms to 55ms) 0110b 160-170ms (spec range is 65ms to 210ms) Values available if Range C (250ms to 4s) programmability range is supported: 1001b 400-500ms (spec range is 260ms to 900ms) 1010b 1.6-1.7s (spec range is 1s to 3.5s) Values not defined above are Reserved. Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either on when this value was changed or on when each request was issued.

11.1.24 Link Capabilities 2 (LCAP2) - Offset 6Ch

This is Link Capabilities 2 register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 6Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RO	**Lower SKP OS Reception Supported Speeds Vector (LSOSRSS):** Lower SKP OS Reception Supported Speeds Vector (LSOSRSS): If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports receiving SKP OS at the rate defined for SRNS while running in SRIS. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector.
15:9	00h RO	**Lower SKP OS Generation Supported Speeds Vector (LSOSGSSV):** Lower SKP OS Generation Supported Speeds Vector (LSOSGSSV): If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports software control of the SKP Ordered Set transmission scheduling rate. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector.
8	0h RO	**Crosslink Supported (CS):** Crosslink Supported (CS): No support for Crosslink. Register Attribute: Static.
7:1	00h RO/V	**Supported Link Speeds Vector (SLSV):** Supported Link Speeds Vector (SLSV): This field indicates the supported Link speed of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported; otherwise, the Link speed is not supported. Bit definitions within this field for PCI Express are: Bit 0: 2.5 GT/s. Bit 1: 5.0 GT/s. Bit 2: 8.0 GT/s. Bits 6:3: Reserved. This register reports a value of 0000001b if GEN1 data rate is supported but both GEN2 and GEN3 data rate support are disabled through PCI Express Speed Limit Fuse or MPC.PCIESD register. This register reports a value of 0000011b if both GEN1 and GEN2 data rate are supported but GEN3 data rate support is disabled through PCI Express Speed Limit Fuse or MPC.PCIESD register. Otherwise, this field reports 0000111b. Register Attribute: Static.
0	0h RO	**Reserved**

11.1.25 Link Control 2 And Link Status 2 (LCTL2_LSTS2) - Offset 70h

This is Link Control 2 and Link Status 2 register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 70h	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW/1C/V/P	**Link Equalization Request (LER):** Link Equalization Request (LER): This bit is set by hardware to request the Link equalization process to be performed on the Link. Register Attribute: Dynamic.
20	0h RO/V/P	**Equalization Phase 3 Successful (EQP3S):** Equalization Phase 3 Successful (EQP3S): When set to 1, this bit indicates that Phase 3 of the Transmitter Equalization procedure has successfully completed.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO/V/P	**Equalization Phase 2 Successful (EQP2S):** Equalization Phase 2 Successful (EQP2S): When set to 1, this bit indicates that Phase 2 of the Transmitter Equalization procedure has successfully completed.
18	0h RO/V/P	**Equalization Phase 1 Successful (EQP1S):** Equalization Phase 1 Successful (EQP1S): When set to 1, this bit indicates that Phase 1 of the Transmitter Equalization procedure has successfully completed.
17	0h RO/V/P	**Equalization Complete (EQC):** Equalization Complete (EC): When set to 1, this bit indicates that the Transmitter Equalization procedure has completed
16	0h RO/V	**Current De-emphasis Level (CDL):** When the Link is operating at 5.0 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 1b -3.5 dB 0b -6 dB The value in this bit is undefined when the Link is not operating at 5.0 GT/s speed.
15:12	0h RW/P	**Compliance Preset/De-emphasis (CD):** For 8.0 GT/s Data Rate: This field sets the Transmitter Preset in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Results are undefined if a reserved preset encoding is used when entering Polling.Compliance in this way. For 5.0 GT/s Data Rate: This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 0001b -3.5 dB 0000b -6 dB When the Link is not operating at 2.5 GT/s speed, the setting of this bit has no effect. The default value of this field is 0000b. This bit is intended for debug, compliance testing purposes. System firmware and software are allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value.
11	0h RW/P	**Compliance SOS (CSOS):** When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. The default value of this bit is 0b. This bit is applicable when the Link is operating at 2.5 GT/s or 5.0 GT/s data rates only. Register Attribute: Static.
10	0h RW/P	**Enter Modified Compliance (EMC):** When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Default value of this bit is 0b. This register is intended for debug, compliance testing purposes only. System firmware and software are allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.
9:7	0h RW/P	**Transmit Margin (TM):** This field controls the value of the non-deemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling. Encodings: 000b Normal operating range 001b 800-1200 mV for full swing and 400-700 mV for half-swing 010b - (n-1) Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n: 200-400 mV for full-swing and 100-200 mV for half-swing n - 111b reserved For a Multi-Function device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Default value of this field is 000b. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 000b. This register is intended for debug, compliance testing purposes only. System firmware and software are allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.
6	0h RW/P	**Selectable De-emphasis (SD):** When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b -3.5 dB 0b -6 dB When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**Hardware Autonomous Speed Disable (HASD):** Reserved
4	0h RW/P	**Enter Compliance (EC):** Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. This bit is intended for debug, compliance testing purposes only. System firmware and software are allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value. Register Attribute: Static.
3:0	1h RW/V/P	**Target Link Speed (TLS):** Target Link Speed (TLS): This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. If a value is written to this field that does not correspond to a supported speed, as indicated by the Supported Link Speeds Vector, the result is undefined. The default value of this field is GEN1. Note: This register field could be used by REUT software to limit the link speed to 2.5 GT/s or 5 GT/s data rate. Register Attribute: Dynamic.

11.1.26 Message Signaled Interrupt Identifiers And Message Signaled Interrupt Message Control (MID_MC) - Offset 80h

This is Message Signaled Interrupt Identifiers and Message Signaled Interrupt Message Control register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 80h	00009005h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**64-Bit Address Capable (C64):** Capable of generating a 32-bit message only.
22:20	0h RW	**Multiple Message Enable (MME):** These bits are RW for software compatibility, but only one message is ever sent by the root port.
19:17	0h RO	**Multiple Message Capable (MMC):** Only one message is required.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. CMD.BME must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated.
15:8	90h RW/O	**Next Pointer (NEXT):** Indicates the location of the next capability in the list. The default value of this register is 90h which points to the Subsystem Vendor capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	05h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

11.1.27 Message Signaled Interrupt Message Address (MA) - Offset 84h

This is Message Signaled Interrupt Message Address register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**ADDR:** Lower 32 bits of the system specified message address, always DW aligned.
1:0	0h RO	**Reserved**

11.1.28 Message Signaled Interrupt Message Data (MD) - Offset 88h

This is Message Signaled Interrupt Message Data register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**DATA:** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[lb]15:0[rb]) during the data phase of the MSI memory write transaction.

11.1.29 Subsystem Vendor Capability (SVCAP) - Offset 90h

This is Subsystem Vendor Capability register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 90h	0000A00Dh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	A0h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability in the list. The default value of this register is A0h which points to the PCI Power Management capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	0Dh RO	**Capability Identifier (CID):** Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

11.1.30 Subsystem Vendor IDs (SVID) - Offset 94h

Size: 32 bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem Identifier (SID):** Indicates the subsystem as identified by the vendor. This field is written once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	0000h RW/O	**Subsystem Vendor Identifier (SVID):** Indicates the manufacturer of the subsystem. This field is written once and is locked down until a bridge reset occurs (not the PCI bus reset).

11.1.31 Power Management Capability And PCI Power Management Capabilities (PMCAP_PMC) - Offset A0h

Size: 32 bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + A0h	C8030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	19h RO	**PME Support (PMES):** Indicates PME# is supported for states D0, D3HOT and D3COLD. The root port does not generate PME#, but reporting that it does is necessary for legacy operating systems to enable PME# in devices connected behind this root port.
26	0h RO	**D2S:** The D2 state is not supported.
25	0h RO	**D1S:** The D1 state is not supported.
24:22	0h RO	**AC:** Reports 375mA maximum suspend well current required when in the D3COLD state.
21	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
20	0h RO	**Reserved**
19	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
18:16	3h RO	**VS:** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NEXT):** Indicates this is the last item in the list.
7:0	01h RO	**Capability Identifier (CID):** Value of 01h indicates this is a PCI power management capability.

11.1.32 PCI Power Management Control And Status (PMCS) - Offset A4h

This is PCI Power Management Control And Status register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + A4h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**DTA:** Reserved
23	0h RO	**Bus Power / Clock Control Enable (BPCE):** Reserved
22	0h RO	**B2/B3 Support (B23S):** Reserved
21:16	0h RO	**Reserved**
15	0h RO	**PME Status (PMES):** Indicates a PME was received on the downstream link.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RO	**Data Scale (DSC):** Reserved
12:9	0h RO	**Data Select (DSEL):** Reserved
8	0h RW/P	**PME Enable (PMEE):** Indicates PME is enabled. The root port takes no action on this bit, but it must be RW for legacy operating systems to enable PME# on devices connected to this root port.
7:4	0h RO	**Reserved**
3	1h RW/O	**No Soft Reset (NSR):** When set to 1 this bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3hot to D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the Power State bits. When clear, devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the Power State bits. Configuration Context is lost when performing the soft reset. Upon transition from D3hot to D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	**Reserved**
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 - D0 state 11 - D3HOT state When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into D3HOT. If software attempts to write a '10' or '01' to these bits, the write will be ignored. **Locked by:** PMCS.PS

11.1.33 Advanced Error Extended Reporting Capability Header (AECH) - Offset 100h

Size: 32 bits The AER capability can optionally be included or excluded from the capabilities list. The full AER is supported.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 100h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** Set to 000h as this is the last capability in the list. Point to the next capability.
19:16	0h RW/O	**Capability Version (CV):** For systems that support AER, BIOS should write a 1h to this register else it should write 0
15:0	0000h RW/O	**Capability ID (CID):** For systems that support AER, BIOS should write a 0001h to this register else it should write 0

11.1.34 Uncorrectable Error Status (UES) - Offset 104h

This register must maintain its state through a platform reset. It loses its state upon loss of core power.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 104h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26	0h RW/1C/V/P	**Poisoned TLP Egress Blocked Status (PTLPEBS):** Indicates that poisoned TLP Egress Blocked error has occurred. ***Note***: This bit can only be set if DPCCAPR.PTLPEBS = 1 and DPCCTLR.PTLPEBE = 1. Register Attribute: Dynamic.
25:22	0h RO	**Reserved**
21	0h RW/1C/V/P	**ACS Violation Status (AVS):** Indicates an ACS Violation is logged
20	0h RW/1C/V/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received.
19	0h RO	**ECRC Error Status (EE):** ECRC is not supported.
18	0h RW/1C/V/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received.
17	0h RW/1C/V/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred.
16	0h RW/1C/V/P	**Unexpected Completion Status (UC):** Indicates an unexpected completion was received.
15	0h RW/1C/V/P	**Completor Abort Status (CA):** Indicates a completer abort was received
14	0h RW/1C/V/P	**Completion Timeout Status (CT):** Indicates a completion timed out. This is signaled if Completion Timeout is enabled and a completion fails to return within the amount of time specified by the Completion Timeout Value
13	0h RO	**Flow Control Protocol Error Status (FCPE):** Not supported.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C/V/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received.
11:6	0h RO	**Reserved**
5	0h RO	**Surprise Down Error Status (SDE):** Surprise Down is not supported.
4	0h RW/1C/V/P	**Data Link Protocol Error Status (DLPE):** Indicates a data link protocol error occurred.
3:1	0h RO	**Reserved**
0	0h RO	**Training Error Status (TE):** Not supported.

11.1.35 Uncorrectable Error Mask (UEM) - Offset 108h

When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 108h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26	0h RW/P	**Poisoned TLP Egress Blocked Mask (PTLPEBM):** Mask for Poisoned TLP Egress Blocked error. Register Attribute: Dynamic.
25:22	0h RO	**Reserved**
21	0h RW/P	**ACS Violation Mask (AVM):** Mask for ACS Violation errors
20	0h RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors.
19	0h RO	**ECRC Error Mask (EE):** ECRC is not supported.
18	0h RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs
17	0h RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows.
16	0h RW/P	**Unexpected Completion Mask (UC):** Mask for unexpected completions.
15	0h RW/P	**Completor Abort Mask (CM):** Mask for completer abort.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/P	**Completion Timeout Mask (CT):** Mask for completion timeouts.
13	0h RO	**Flow Control Protocol Error Mask (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs.
11:6	0h RO	**Reserved**
5	0h RO	**Surprise Down Error Mask (SDE):** Surprise Down is not supported.
4	0h RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors.
3:1	0h RO	**Reserved**
0	0h RO	**Training Error Mask (TE):** Not supported.

11.1.36 Uncorrectable Error Severity (UEV) - Offset 10Ch

This register gives the option to make an uncorrectable error fatal or non-fatal. An error is fatal if the bit is set. An error is non-fatal if the bit is cleared. This register is only reset by a loss of core power.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 10Ch	00060011h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26	0h RW/P	**Poisoned TLP Egress Blocked Severity (PTLPEBS):** Severity for Poisoned TLP Egress Blocked error. Register Attribute: Dynamic.
25:22	0h RO	**Reserved**
21	0h RW/P	**ACS Violation Severity (AVS):** Severity for ACS violation.
20	0h RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception.
19	0h RO	**ECRC Error Severity (EE):** ECRC is not supported.
18	1h RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception.
17	1h RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW/P	**Unexpected Completion Severity (UC):** Severity for unexpected completion reception.
15	0h RW/P	**Completor Abort Severity (CA):** Severity for completer abort.
14	0h RW/P	**Completion Timeout Severity (CT):** Severity for completion timeout.
13	0h RO	**Flow Control Protocol Error Severity (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception.
11:6	0h RO	**Reserved**
5	0h RO	**Surprise Down Error Severity (SDE):** Surprise Down is not supported.
4	1h RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors.
3:1	0h RO	**Reserved**
0	1h RO	**Training Error Severity (TE):** TE not supported. This bit is left as RO='1' for ease of implementation..

11.1.37 Correctable Error Status (CES) - Offset 110h

This register is only reset by a loss of core power

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 110h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW/1C/V/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that an Advisory Non-Fatal Error occurred.
12	0h RW/1C/V/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out.
11:9	0h RO	**Reserved**
8	0h RW/1C/V/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over.
7	0h RW/1C/V/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/1C/V/P	**Bad TLP Status (BT):** Indicates a bad TLP was received.
5:1	0h RO	**Reserved**
0	0h RW/1C/V/P	**Receiver Error Status (RE):** Indicates a receiver error occurred.

11.1.38 Correctable Error Mask (CEM) - Offset 114h

When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 114h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	1h RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12	0h RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout.
11:9	0h RO	**Reserved**
8	0h RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover.
7	0h RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception.
6	0h RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception.
5:1	0h RO	**Reserved**
0	0h RW/P	**Receiver Error Mask (RE):** Mask for receiver errors.

11.1.39 Advanced Error Capabilities And Control (AECC) - Offset 118h

This register is only reset by a loss of core power.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 118h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RO	**Completion Timeout Prefix/Header Log Capable (CTPHLC):** If set, this bit indicates that port records the prefix/header of Request TLPs that experience a Completion Timeout error. Note: BIOS should program this bit before enable the Completion Timeout mechanism. Register Attribute: Static.
11:9	0h RO	**Reserved**
8	0h RO	**ECRC Check Enable (ECE):** ECRC is not supported.
7	0h RO	**ECRC Check Capable (ECC):** ECRC is not supported.
6	0h RO	**ECRC Generation Enable (EGE):** ECRC is not supported.
5	0h RO	**ECRC Generation Capable (EGC):** ECRC is not supported.
4:0	00h RO/V/P	**First Error Pointer (FEP):** Identifies the bit position of the first error reported in the Uncorrectable Error Status Register.

11.1.40 Header Log DW1 (HL_DW1) - Offset 11Ch

Size: 32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 11Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**1st dWord of TLP (DW1):** Byte0 [amp][amp] Byte1 [amp][amp] Byte2 [amp][amp] Byte3

11.1.41 Header Log DW2 (HL_DW2) - Offset 120h

Size: 32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 120h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**2nd dWord of TLP (DW2):** Byte4 [amp][amp] Byte5 [amp][amp] Byte6 [amp][amp] Byte7

11.1.42 Header Log DW3 (HL_DW3) - Offset 124h

Size: 32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 124h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**3rd dWord of TLP (DW3):** Byte8 [amp][amp] Byte9 [amp][amp] Byte10 [amp][amp] Byte11

11.1.43 Header Log DW4 (HL_DW4) - Offset 128h

Size: 32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 128h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**4th dWord of TLP (DW4):** Byte12 [amp][amp] Byte13 [amp][amp] Byte14 [amp][amp] Byte15

11.1.44 Root Error Command (REC) - Offset 12Ch

This register allows errors to generate interrupts.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 12Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW	**Fatal Error Reporting Enable (FERE):** When set, the root port will generate an interrupt when a fatal error is reported by the attached device.
1	0h RW	**Non-fatal Error Reporting Enable (NERE):** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device.
0	0h RW	**Correctable Error Reporting Enable (CERE):** When set, the root port will generate an interrupt when a correctable error is reported by the attached device.

11.1.45 Root Error Status (RES) - Offset 130h

This register can track more than one error and set the *"multiple"* bits if a second or subsequent error occurs and the first has not been serviced. This register is only reset by a loss of core power.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 130h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**Advanced Error Interrupt Message Number (AEMN):** Reserved
26:7	0h RO	**Reserved**
6	0h RW/1C/V/P	**Fatal Error Message Received (FEMR):** Set when one or more Fatal Uncorrectable Error Messages have been received.
5	0h RW/1C/V/P	**Non-Fatal Error Messages Received (NFEMR):** Set when one or more Non-Fatal Uncorrectable error messages have been received
4	0h RW/1C/V/P	**First Uncorrectable Fatal (FUF):** Set when the first Uncorrectable Error message received is for a fatal error.
3	0h RW/1C/V/P	**Multiple ERR_FATAL/NONFATAL Received (MENR):** Set when either a fatal or a non-fatal error is received and the ENR bit is already set.
2	0h RW/1C/V/P	**ERR_FATAL/NONFATAL Received (ENR):** Set when either a fatal or a non-fatal error message is received.
1	0h RW/1C/V/P	**Multiple ERR_COR Received (MCR):** Set when a correctable error message is received and the CR bit is already set.
0	0h RW/1C/V/P	**ERR_COR Received (CR):** Set when a correctable error message is received.

11.1.46 Error Source Identification (ESID) - Offset 134h

Size: 32 bits Identifies the source (Requester ID) of the first correctable and uncorrectable (Non-Fatal/ Fatal) errors reported in the Root Error Status register. This register is only reset by a loss of core power.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 134h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO/V/P	**ERR_FATAL/NONFATAL Source Identification (EFNFSID):** Loaded with the Requester ID indicated in the received ERR_FATAL or ERR_NONFATAL Message with the ERR_FATAL/NONFATAL Received register is not already set.
15:0	0000h RO/V/P	**ERR_COR Source Identification (ECSID):** Loaded with the Requester ID indicated in the received ERR_COR Message with the ERR_COR Received register is not already set.

11.1.47 PTM Extended Capability Header (PTMECH) - Offset 150h

Size: 32 bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 150h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): For systems that support PTM Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0000h RW/O	**Capability ID (CID):** Capability ID (CID): For systems that support PTM Extended Capability, BIOS should write a 001Fh to this register else it should write 0.

11.1.48 PTM Capability Register (PTMCAPR) - Offset 154h

This is PTM Capability register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 154h	00000400h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	04h RW/O	**Local Clock Granularity (LCG):** Local Clock Granularity (LCG): 0000 0000b - Time Source does not implement a local clock. It simply propagates timing information obtained from further Upstream in the PTM Hierarchy when responding to PTM Request messages. 0000 0001b - 1111 1110b: Indicates the period of this Time Sources local clock in ns. 1111 1111b: Indicates the period of this Time Sources local clock is greater than 254 ns. If the PTM Root Select bit is Set, this local clock is used to provide PTM Master Time. Otherwise, the Time Source uses this local clock to locally track PTM Master Time received from further Upstream within a PTM Hierarchy.
7:3	0h RO	**Reserved**
2	0h RW/O	**PTM Root Capable (PTMRC):** PTM Root Capable (PTMRC): Root Ports must set this bit to 1b.
1	0h RW/O	**PTM Responder Capable (PTMRSPC):** PTM Responder Capable (PTMRSPC): Root Ports are permitted to set this bit to 1b to indicate that they implement the PTM Responder role.
0	0h RO	**PTM Requester Capable (PTMREQC):** PTM Requester Capable (PTMREQC): PTM Requester Role is not supported by Root Port.

11.1.49 PTM Control Register (PTMCTLR) - Offset 158h

This is PTM Control register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 158h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RO	**Effective Granularity (EG):** Effective Granularity (EG): Root Port does not support PTM Requester role.
7:2	0h RO	**Reserved**
1	0h RW	**Root Select (RS):** Root Select (RS): When Set, if the PTM Enable bit is also Set, this Time Source is the PTM Root. Within each PTM Hierarchy, it is recommended that system software select only the furthest Upstream Time Source to be the PTM Root.
0	0h RW	**PTM Enable (PTME):** PTM Enable (PTME): When Set, this Function is permitted to participate in the PTM mechanism according to its selected role. Software must not have the PTM Enable bit Set in the PTM Control register on a Function associated with an Upstream Port unless the associated Downstream Port on the Link already has the PTM Enable bit Set in its associated PTM Control register. Register Attribute: Static.

11.1.50 L1 Sub-States Extended Capability Header (L1SECH) - Offset 200h

Size: 32 bits

Note: When operating in Mobile Express mode, this capability should not be enabled.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 200h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 1h
15:0	0000h RW/O	**PCI Express Extended Capability ID (PCIEEC):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 001Eh.

11.1.51 L1 Sub-States Capabilities (L1SCAP) - Offset 204h

This is L1 Sub-States Capabilities register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 204h	0028281Fh

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:19	05h RW/O	**Port Tpower_on Value (PTV):** Along with the Port T_POWER_ON Scale Field in the L1 Substate Capabilities register sets theTime (in us) that this Port requires the port on the opposite side of Link to wait in L1.OFF_EXIT after sampling CLKREQ# asserted before actively driving the interface. Port Tpower_on is calculated by multiplying the value in this field by the value in the Port Tpower_on scale field in the L1 Sub-States Capabilities 2 register. Required for all Ports that support L1.OFF.
18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW/O	**Port Tpower_on Scale (PTPOS):** Specifies the scale used for Tpower_on value field in the L1 Substate Capabilities register. *"00b"*: 2us *"01b"*: 10us *"10b"*: 100us *"11b"*: Reserved Required for all Ports that support L1.OFF.
15:8	28h RW/O	**Port Common Mode Restore Time (PCMRT):** This is the time (in us) required for this Port to re-establish common mode. Required for all ports that support L1.OFF.
7	0h RO	**Reserved**
6	0h RW/1C/V	**L1-Substate Exit Interrupt Status (L1SSEIS):** CLKREQ# Acceleration Interrupt Status - For a Downstream Port that has both the CLKREQ# Acceleration Supported and CLKREQ# Acceleration Interrupt Enable bits Set, when set this bit indicates that the Port has completed the CLKREQ# Acceleration Link Activation process, and that the Link has reached L0. Software must then clear this bit by writing a 1b to this bit. Must be hardwired to 0b for Upstream Ports. Default value is 0b.
5	0h RW/O	**L1-Substate Exit Supported (L1SSES):** CLKREQ# Acceleration Supported - When set this bit indicates that this Port supports CLKREQ# Acceleration
4	1h RW/O	**L1 PM Substate Supported (L1PSS):** When Set this bit indicates that this Port supports L1 PM Substate. For compatibility with possible future extensions, software must not enable L1 PM Substate unless this bit is set. This RWO field must be programmed prior to enabling ASPM. Required for both Upstream and Downstream Ports.
3	1h RW/O	**ASPM L1.1 Substate Supported (AL11S):** When set, this bit indicates that this port supports L1 Substate for ASPM L1.SNOOZ is supported. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
2	1h RW/O	**ASPM L1.2 Supported (AL12S):** When set, this bit indicates that ASPM_L1.OFF is supported. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
1	1h RW/O	**PCI-PM L1.1 Supported (PPL11S):** When set, this bit indicates that L1.SNOOZ sub-state is supported and this bit must be set by all ports implementing L1 Sub-States. A port that supports L1.OFF must support L1.SNOOZ. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
0	1h RW/O	**PCI-PM L1.2 Supported (PPL12S):** When set, this bit indicates that PCI-PM L1.OFF power management feature is supported. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static

11.1.52 L1 Sub-States Control 1 (L1SCTL1) - Offset 208h

This is L1 Sub-States Control 1 register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 208h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**L1.2 LTR Threshold Latency Scale Value (L12LTRTLSV):** This field contains the L1.OFF LTR Threshold Latency Scale Value for this particular PCIe Root Port. The value in this field, together with L12LTRTLV is compared against both the snoop and non-snoop LTR values of the device. 000: L12LTRSTLV times 1 ns 001: L12LTRSTLV times 32 ns 010: L12LTRSTLV times 1024 ns 011: L12LTRSTLV times 32768 ns 100: L12LTRSTLV times 1048576 ns 101: L12LTRSTLV times 33554432 ns Others: Not Permitted. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
28:26	0h RO	**Reserved**
25:16	000h RW	**L1.2 LTR Threshold Latency Value (L12OFFLTRTLV):** This field contains the L1.2 LTR Threshold Latency Value for this particular PCIe Root Port. The value in this field, together with L12LTRTLSV is compared against both the snoop and non-snoop LTR values of the device. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
15:8	00h RW	**Common Mode Restore Time (CMRT):** This is the Tcommon_mode time (in us) the PCIe Root Port needs to continue sending TS1 and refrain from sending TS2 in Recovery state to allow the TX common mode to be established prior to sending TS2. The timer starts from the time when the first TS1 has been sent and the receiver has detected un-squelch. The value in this field defines the time in micro-seconds. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
7:6	0h RO	**Reserved**
5	0h RW	**L1-Substate Exit Control (L1SSEC):** L1 Substate Exit Control - For a Downstream Port, when any one or more of the PCI-PM L1.2 Enable, PCI-PM L1.1 Enable, {ASPM L1.2 Enable, ASPM L1.1 Enable } bit are Set, then when this bit is Set, the Port must initiate the CLKREQ# Acceleration Link Activation process, and once the Link reaches L0, the Port must continue to attempt to maintain the Link in L0 for as long as this bit remains Set. Must be hardwired to 0b for Upstream Ports. Default value is 0b.If this bit is set, and the link is in L1 Substate, the downstream port will initiate L1 Substate exit to L0. This includes asserting the CLKREQ# pin to trigger L1 Substate exit, and sending Training Sequence to bring the LTSSM back to L0 through Recovery state. The CLKREQ# pin will continue to be asserted as long as this bit is set even after the LTSSM has reached L0, until this bit is cleared.
4	0h RW	**L1-Substate Exit Interrupt Enable (L1SSEIE):** CLKREQ# Acceleration Interrupt Enable - When set this bit enables the generation of an interrupt to indicate the completion of the CLKREQ# Acceleration Link Activation process. Required for Downstream Ports when the CLKREQ# Acceleration Supported bit is Set. Must be hardwired to 0b for Upstream Ports. Default value is 0b.
3	0h RW	**ASPM L1.1 Enabled (AL11E):** When set, this bit indicates that ASPM L1.SNOOZ Substate are enabled for ASPM. Required for both upstream and downstream ports. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**ASPM L1.2 Enable (AL12E):** When set, this bit indicates that ASPM L1.OFF substates are enabled for PCI-PM. Required for both upstream and downstream ports. Register Attribute: Dynamic. Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.
1	0h RW	**PCI-PM L1.SNOOZ Enable (PPL11E):** When set, this bit indicates that PCI-PM L1.SNOOZ power management feature is enabled. If L1.OFF is enabled, L1.SNOOZ must also be enabled. This field must be programmed prior to enabling ASPM L1. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.
0	0h RW	**PCI-PM L1.2 Enabled (PPL12E):** When set, this bit indicates that PCI-PM L1.OFF power management feature is enabled. L1.OFF can only be enabled if the platform supports bi-directional CLKREQPLUS#. This field must be programmed prior to enabling ASPM L1. Ports that support L1.OFF shall support Latency Tolerance Reporting. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.

11.1.53 L1 Sub-States Control 2 (L1SCTL2) - Offset 20Ch

This is L1 Sub-States Control 2 register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 20Ch	00000028h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:3	05h RW	**Power On Wait Time (POWT):** Along with the Tpower_on Scale sets the minimum amount of time (in us) that the Port must wait in L1.OFF EXIT after sampling CLKREQPLUS# asserted before actively driving the interface. The timer starts counting when CLKREQPLUS# is sampled asserts in L1.OFF state. Tpower_on value is calculated by multiplying the value in this field by the value in the TPOS field. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
2	0h RO	**Reserved**
1:0	0h RW	**Tpower_on Scale (TPOS):** Specifies the scale used for Tpower_on value. *"00b"*: 2 us *"01b"*: 10 us *"10b"*: 100us *"11b"*: Reserved. Required for all Ports that support L1.OFF. Register Attribute: Static

11.1.54 ACS Extended Capability Header (ACSECH) - Offset 220h

Size: 32 bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 220h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): For systems that support ACS Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0000h RW/O	**Capability ID (CID):** Capability ID (CID): For systems that support ACS Extended Capability, BIOS should write a 000Dh to this register else it should write 0.

11.1.55 ACS Capability Register And ACS Control Register (ACSCAPR_ACSCTLR) - Offset 224h

This is ACS Capability Register and ACS Control register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + 224h	0000001Fh

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22	0h RO	**ACS Direct Translated P2P Enable (TE):** ACS Direct Translated P2P Enable (T): ACS Direct Translated P2P is not supported.
21	0h RO	**ACS P2P Egress Control Enable (EE):** ACS P2P Egress Control Enable (E): ACS P2P Egress Control is not supported.
20	0h RW	**ACS Upstream Forwarding Enable (UE):** When set, the component forwards upstream any Request or Completion TLPs it receives that were redirected upstream by a component lower in the hierarchy. Note that the U bit only applies to upstream TLPs arriving at a Downstream Port, and whose normal routing targets the same Downstream Port. Upstream I/O, Configuration, VDM Message, Message are never affected by ACS Upstream Forwarding Enable. Register Attribute: Static
19	0h RW	**ACS P2P Completion Redirect Enable (CE):** ACS P2P Completion Redirect (C): Determines when the component redirects peer-to-peer Completions upstream; applicable only to Read Completions whose Relaxed Ordering Attribute is clear. Requests are never affected by ACS P2P Completion Redirect. Default value of this field is 0b. Register Attribute: Static.
18	0h RW	**ACS P2P Request Redirect Enable (RE):** ACS P2P Request Redirect Enable (R): Determines when the component redirects peer-to-peer memory Requests targeting another peer port upstream. I/O, Configuration, VDM Messages and Completions are never affected by ACS P2P Request Redirect. Default value of this field is 0b. Register Attribute: Static.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**ACS Translation Blocking Enable (BE):** ACS Translation Blocking Enable (B): When set, the component blocks all upstream Memory Requests whose Address Translation (AT) field is not set to the default value. I/O, Configuration, Completions and Messages are never affected by ACS Translation Blocking. Default value of this field is 0b. Register Attribute: Static.
16	0h RW	**ACS Source Validation Enable (VE):** ACS Source Validation Enable (V): When set, the component validates the Bus Number from the Requester ID of upstream Requests against the secondary / subordinate Bus Numbers. I/O, Configuration and Completions are never affected by ACS Source Validation. Default value of this field is 0b. Register Attribute: Static.
15:7	0h RO	**Reserved**
6	0h RO	**ACS Direct Translated P2P (T):** ACS Direct Translated P2P (T): ACS Direct Translated P2P is not supported.
5	0h RO	**ACS P2P Egress Control (E):** ACS P2P Egress Control (E): ACS P2P Egress Control is not supported
4	1h RW/O	**ACS Upstream Forwarding (U):** Required for Root Ports if the RC supports Redirected Request Validation: required for Switch Downstream Ports: must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Upstream Forwarding Register Attribute: Static
3	1h RW/O	**ACS P2P Completion Redirect (C):** ACS P2P Completion Redirect (C): Required for all Functions that support ACS P2P Request Redirect; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Completion Redirect. Register Attribute: Static.
2	1h RW/O	**ACS P2P Request Redirect (R):** ACS P2P Request Redirect (R): Required for Root Ports that support peer-to-peer traffic with other Root Ports; required for Switch Downstream Ports; required for multi-function device Functions that support peer-to-peer traffic with other Functions; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Request Redirect. Register Attribute: Static.
1	1h RW/O	**ACS Translation Blocking (B):** ACS Translation Blocking (B): Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Translation Blocking. Register Attribute: Static.
0	1h RW/O	**ACS Source Validation (V):** ACS Source Validation (V): Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Source Validation. Register Attribute: Static.

11.1.56 DPC Extended Capability Header (DPCECH) - Offset A00h

Size: 32 bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + A00h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** For systems that support DPC Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0000h RW/O	**Capability ID (CID):** For systems that support DPC Extended Capability, BIOS should write a 001Dh to this register else it should write 0.

11.1.57 DPC Capability Register And DPC Control Register (DPCCAPR_DPCCTLR) - Offset A04h

This is DPC Capability Register and DPC Control register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + A04h	000014E0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**DL_Active ERR_COR Enable (DLAECE):** This bit when set, enables the downstream port to signal ERR_COR when the link transitions to the DL_Active state. Register Attribute: Dynamic.
22	0h RW	**DPC Software Trigger (DPCST):** If DPC Trigger is enabled and the DPC Trigger Status bit is clear, software writing a 1b to this bit will cause DPC to be triggered. If DPC Trigger is not enabled or DPC Trigger Status is set, software writing a 1b to this bit has no effect. ***Note***: It is permitted to write 1b to this bit while simultaneously writing updated values to other fields in this register, notably the DPC Trigger Enable field. For this case, the DPC Software Trigger semantics are based on the updated value of the DPC Trigger Enable field. ****Note***: This bit always return 0b when read. Register Attribute: Dynamic.
21	0h RW	**Poisoned TLP Egress Blocking Enable (PTLPEBE):** This bit, when set, enables the associated Egress Port to block the transmission of poisoned TLP. Register Attribute: Dynamic.
20	0h RW	**DPC ERR_COR Enable (DPCECE):** When set, this bit enables the generation of an interrupt to indicate that DPC has been triggered. Register Attribute: Dynamic.
19	0h RW	**DPC Interrupt Enable (DPCIE):** When set, this bit enables the generation of an interrupt to indicate that DPC has been triggered. Register Attribute: Dynamic.
18	0h RW	**DPC Completion Control (DPCCC):** This bit controls the Completion Status for completions formed during DPC. 0b: Completer Abort (CA) Completion Status. 1b: Unsupported Request (UR) Completion Status. Register Attribute: Dynamic.

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**DPC Trigger Enable (DPCTE):** This field enables DPC and controls the conditions that cause DPC to be triggered.00b: DPC is disabled. 01b: DPC is enabled and is triggered when the Downstream Port detects an unmasked uncorrectable error or when the Downstream Port receives an ERR_FATAL message. 10b: DPC is enabled and is triggered when the Downstream Port detects an unmasked uncorrectable error or when the Downstream Port receives an ERR_NONFATAL or ERR_FATAL message. 11b: Reserved. Register Attribute: Dynamic.
15:13	0h RO	**Reserved**
12	1h RW/O	**DL_Active ERR_COR Signaling Supported (DLAECSS):** This field when set, indicates that the Root Port supports the ability to signal with ERR_COR when the link transitions to the DL_Active state. Root Port that supports RP Extensions for DPC must set this bit. Register Attribute: Static.
11:8	4h RW/O	**RP PIO Log Size (RPPIOLS):** This field indicates how many DWORDs are allocated for the RP PIO log registers, comprised by the RP PIO Header Log, RP PIO ImpSpec Log and RP PIO TLP Prefix Log. If the Root Port supports RP Extensions for DPC, the value of this field must be 4 or greater; otherwise the value of this field must be 0. Register Attribute: Static.
7	1h RW/O	**DPC Software Triggering Supported (DPCSTS):** This field when set, indicates that the Root Port supports the ability for software to trigger DPC. Root Ports that support RP Extensions for DPC must set this bit. Register Attribute: Static.
6	1h RW/O	**Poisoned TLP Egress Blocking Supported (PTLPEBS):** This field when set, indicates that the Root Port supports the ability to block the transmission of a poisoned TLP from its Egress port. Root Ports that support RP Extensions for DPC must set this bit. Register Attribute: Static.
5	1h RW/O	**RP Extensions For DPC (RPEFDPC):** This field when set, indicates that a Root Port supports a defined set of DPC Extensions that are specific to Root Ports. Register Attribute: Static.
4:0	00h RW/O	**DPC Interrupt Message Number (DPCIMN):** This field indicates which MSI/MSI-X vector is used for the interrupt message generated in association with the DPC Capability structure. For MSI, the value in this field indicates the offset between the base Message Data and the interrupt message that is generated. Hardware is required to update this field so that it is correct if the number of MSI Messages assigned to the Function changes when software writes to the Multiple Message Enable field in the MSI Message Control register. For MSI-X, the value in this field indicates which MSI-X Table entry is used to generate the interrupt message. The entry must be one of the first 32 entries even if the Function implements more than 32 entries. For a given MSI-X implementation, the entry must remain constant. If both MSI and MSI-X are implemented, they are permitted to use different vectors, though software is permitted to enable only one mechanism at a time. If MSI-X is enabled, the value in this field must indicate the vector for MSI-X. If MSI is enabled or neither is enabled, the value in this field must indicate the vector for MSI. If software enables both MSI and MSI-X at the same time, the value in this field is undefined. ***Note***: BIOS is expected to update this field with the right value before enabling DPC interrupt. Register Attribute: Static.

11.1.58 DPC Status Register And DPC Error Source ID Register (DPCSR_DPCESIDR) - Offset A08h

This is DPC Status Register and DPC Error Source ID register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + A08h	00001F00h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO/V/P	**DPC Error Source ID (DPCESID):** When the DPC Trigger Reason field indicates that DPC was triggered due to the reception of an ERR_NONFATAL or ERR_FATAL message, this register field contains the Requester ID of the received messages. Otherwise, the value of this register is undefined. Register Attribute: Static.
15:13	0h RO	**Reserved**
12:8	1Fh RO/V/P	**RP PIO First Error Pointer (RPPIOFEP):** The value of this field identifies a bit position in the RP PIO Status register, and this field is considered valid when that bit is set. When this field is valid, and software writes a 1b to the indicated RP PIO Status bit (thus clearing it), this field must revert to its default value. This field is applicable only for Root Ports that support RP Extensions for DPC, and is otherwise reserved. If this field is not reserved, the default value is 11111b. Register Attribute: Dynamic.
7	0h RO	**Reserved**
6:5	0h RO/V/P	**DPC Trigger Extension (DPCTE):** This field serves as an extension to the DPC Trigger Reason field. When that field is valid and has a value of 11b, this field indicates why DPC has been triggered. 00b: DPC was triggered due to RP PIO error. 01b: DPC was triggered due to DPC Software Trigger bit. 10b: Reserved. 11b: Reserved. This field is valid only when the DPC Trigger Status bit is set and the value of the DPC Trigger Reason field is 11b. Otherwise the value of this field is undefined. Register Attribute: Dynamic.
4	0h RO	**DPC RP Busy (DPCRPB):** When the DPC Trigger Status bit is Set and this bit is Set, the Root Port is busy with internal activity that must complete before software is permitted to clear the DPC Trigger Status bit. If software Clears the DPC Trigger Status bit while this bit is set, the behavior is undefined. This field is valid only when the DPC Trigger Status bit is Set; otherwise the value of this field is undefined. This bit is applicable only for Root Ports that support RP Extensions for DPC, and is Reserved otherwise. Register Attribute: Dynamic.
3	0h RW/1C/V/P	**DPC Interrupt Status (DPCIS):** This bit is set if DPC is triggered while the DPC Interrupt Enable bit is set. Register Attribute: Dynamic.
2:1	0h RO/V/P	**DPC Trigger Reason (DPCTR):** This field indicates why DPC has been triggered. 00b: DPC was triggered due to an unmasked uncorrectable error. 01b: DPC was triggered due to receiving an ERR_NONFATAL. 10b: DPC was triggered due to receiving an ERR_FATAL. 11b: DPC was triggered due to a reason that is indicated by the DPC Trigger Reason Extension field. ***Note***: This field is only valid when DPC Trigger Status bit is set; otherwise the value of this field is undefined. Register Attribute: Dynamic.
0	0h RW/1C/V/P	**DPC Trigger Status (DPCTS):** When set, indicates that DPC has been triggered. DPC is event triggered. While this bit is set, hardware must direct the LTSSM to the Disabled state. This bit must be cleared before the LTSSM can be released from Disabled state. Once the requirements for how long software must leave the downstream port in DPC is met, software is permitted to clear this bit regardless of the state of other status bits associated with the triggering event.

11.1.59 RP PIO Status Register (RPPIOSR) - Offset A0Ch

This is RP PIO Status register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + A0Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW/1C/V/P	**Memory Completion Timeout Status (MCTS):** Non-posted memory request completion times out. Register Attribute: Dynamic.
17	0h RW/1C/V/P	**Memory Completer Abort Completion Status (MCACS):** Non-posted memory request received CA completion. Register Attribute: Dynamic.
16	0h RW/1C/V/P	**Memory Unsupported Request Completion Status (MURCS):** Non-posted Memory request received UR completion. Register Attribute: Dynamic.
15:11	0h RO	**Reserved**
10	0h RW/1C/V/P	**I/O Completion Timeout Status (IOCTS):** I/O request completion times out. Register Attribute: Dynamic.
9	0h RW/1C/V/P	**I/O Completer Abort Completion Status (IOCACS):** I/O request received CA completion. Register Attribute: Dynamic.
8	0h RW/1C/V/P	**I/O Unsupported Request Completion Status (IOURCS):** I/O request received UR completion. Register Attribute: Dynamic.
7:3	0h RO	**Reserved**
2	0h RW/1C/V/P	**Configuration Completion Timeout Status (CCTS):** Configuration request completion times out. Register Attribute: Dynamic.
1	0h RW/1C/V/P	**Configuration Completer Abort Completion Status (CCACS):** Configuration request received CA completion. Register Attribute: Dynamic.
0	0h RW/1C/V/P	**Configuration Unsupported Request Completion Status (CURCS):** Configuration request received UR completion. Register Attribute: Dynamic.

11.1.60 RP PIO Mask Register (RPPIOMR) - Offset A10h

This is RP PIO Mask register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + A10h	00070707h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	1h RW/P	**Memory Completion Timeout Mask (MCTM):** Mask bit for Memory Completion Timeout Status. Register Attribute: Dynamic.
17	1h RW/P	**Memory Completer Abort Completion Mask (MCACM):** Mask bit for Memory Completer Abort Completion Status. Register Attribute: Dynamic.
16	1h RW/P	**Memory Unsupported Request Completion Mask (MURCM):** Mask bit for Memory Unsupported Request Completion Status. Register Attribute: Dynamic.
15:11	0h RO	**Reserved**
10	1h RW/P	**I/O Completion Timeout Mask (IOCTM):** Mask bit for I/O Completion Timeout Status. Register Attribute: Dynamic.
9	1h RW/P	**I/O Completer Abort Completion Mask (IOCACM):** Mask bit for I/O Completer Abort Completion Status. Register Attribute: Dynamic.
8	1h RW/P	**I/O Unsupported Request Completion Mask (IOURCM):** Mask bit for I/O Unsupported Request Completion Status. Register Attribute: Dynamic.
7:3	0h RO	**Reserved**
2	1h RW/P	**Configuration Completion Timeout Mask (CCTM):** Mask bit for Configuration Completion Timeout Status. Register Attribute: Dynamic.
1	1h RW/P	**Configuration Completer Abort Completion Mask (CCACM):** Mask bit for Configuration Completer Abort Completion Status. Register Attribute: Dynamic.
0	1h RW/P	**Configuration Unsupported Request Completion Mask (CURCM):** Mask bit for Configuration Unsupported Request Completion Status. Register Attribute: Dynamic.

11.1.61 RP PIO Severity Register (RPPIOVR) - Offset A14h

This is RP PIO Severity register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + A14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW/P	**Memory Completion Timeout Severity (MCTSV):** Severity bit for Memory Completion Timeout Status. Register Attribute: Dynamic.
17	0h RW/P	**Memory Completer Abort Completion Severity (MCACSV):** Severity bit for Memory Completer Abort Completion Status. Register Attribute: Dynamic.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW/P	**Memory Unsupported Request Completion Severity (MURCSV):** Severity bit for Memory Unsupported Request Completion Status. Register Attribute: Dynamic.
15:11	0h RO	**Reserved**
10	0h RW/P	**I/O Completion Timeout Severity (IOCTSV):** Severity bit for I/O Completion Timeout Status. Register Attribute: Dynamic.
9	0h RW/P	**I/O Completer Abort Completion Severity (IOCACSV):** Severity bit for I/O Completer Abort Completion Status. Register Attribute: Dynamic.
8	0h RW/P	**I/O Unsupported Request Completion Severity (IOURCSV):** Severity bit for I/O Unsupported Request Completion Status. Register Attribute: Dynamic.
7:3	0h RO	**Reserved**
2	0h RW/P	**Configuration Completion Timeout Severity (CCTSV):** Severity bit for Configuration Completion Timeout Status. Register Attribute: Dynamic.
1	0h RW/P	**Configuration Completer Abort Completion Severity (CCACSV):** Severity bit for Configuration Completer Abort Completion Status. Register Attribute: Dynamic.
0	0h RW/P	**Configuration Unsupported Request Completion Severity (CURCSV):** Severity bit for Configuration Unsupported Request Completion Status. Register Attribute: Dynamic.

11.1.62 RP PIO SysError Register (RPPIOSER) - Offset A18h

This is RP PIO SysError register. Refer to register field for more details

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + A18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW/P	**Memory Completion Timeout SysErr (MCTSE):** SysErr bit for Memory Completion Timeout Status. Register Attribute: Dynamic.
17	0h RW/P	**Memory Completer Abort Completion SysErr (MCACSE):** SysErr bit for Memory Completer Abort Completion Status. Register Attribute: Dynamic.
16	0h RW/P	**Memory Unsupported Request Completion SysErr (MURCSE):** SysErr bit for Memory Unsupported Request Completion Status. Register Attribute: Dynamic.
15:11	0h RO	**Reserved**
10	0h RW/P	**I/O Completion Timeout SysErr (IOCTSE):** SysErr bit for I/O Completion Timeout Status. Register Attribute: Dynamic.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/P	**I/O Completer Abort Completion SysErr (IOCACSE):** SysErr bit for I/O Completer Abort Completion Status. Register Attribute: Dynamic.
8	0h RW/P	**I/O Unsupported Request Completion SysErr (IOURCSE):** SysErr bit for I/O Unsupported Request Completion Status. Register Attribute: Dynamic.
7:3	0h RO	**Reserved**
2	0h RW/P	**Configuration Completion Timeout SysErr (CCTSE):** SysErr bit for Configuration Completion Timeout Status. Register Attribute: Dynamic.
1	0h RW/P	**Configuration Completer Abort Completion SysErr (CCACSE):** SysErr bit for Configuration Completer Abort Status. Register Attribute: Dynamic.
0	0h RW/P	**Configuration Unsupported Request Completion SysErr (CURCSE):** SysErr bit for Configuration Unsupported Request Completion Status. Register Attribute: Dynamic.

11.1.63 RP PIO Exception Register (RPPIOER) - Offset A1Ch

This is RP PIO Exception register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + A1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW/P	**Memory Completion Timeout Exception (MCTE):** Exception bit for Memory Completion Timeout Status. Register Attribute: Dynamic.
17	0h RW/P	**Memory Completer Abort Completion Exception (MCACE):** Exception bit for Memory Completer Abort Completion Status. Register Attribute: Dynamic.
16	0h RW/P	**Memory Unsupported Request Completion Exception (MURCE):** Exception bit for Memory Unsupported Request Completion Status. Register Attribute: Dynamic.
15:11	0h RO	**Reserved**
10	0h RW/P	**I/O Completion Timeout Exception (IOCTE):** Exception bit for I/O Completion Timeout Status. Register Attribute: Dynamic.
9	0h RW/P	**I/O Completer Abort Completion Exception (IOCACE):** Exception bit for I/O Completer Abort Completion Status. Register Attribute: Dynamic.
8	0h RW/P	**I/O Unsupported Request Completion Exception (IOURCE):** Exception bit for I/O Unsupported Request Completion Status. Register Attribute: Dynamic.

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved**
2	0h RW/P	**Configuration Completion Timeout Exception (CCTE):** Exception bit for Configuration Completion Timeout Status. Register Attribute: Dynamic.
1	0h RW/P	**Configuration Completer Abort Completion Exception (CCACE):** Exception bit for Configuration Completer Abort Completion Status. Register Attribute: Dynamic.
0	0h RW/P	**Configuration Unsupported Request Completion Exception (CURCE):** Exception bit for Configuration Unsupported Request Completion Status. Register Attribute: Dynamic.

11.1.64 RP PIO Header Log Register DW1 (RPPIOHLR_DW1) - Offset A20h

Size: 32 bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + A20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**1st dWord of TLP (DW1):** Byte0 [amp][amp] Byte1 [amp][amp] Byte2 [amp][amp] Byte3. Register Attribute: Dynamic.

11.1.65 RP PIO Header Log Register DW2 (RPPIOHLR_DW2) - Offset A24h

Size: 32 bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + A24h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**2nd dWord of TLP (DW2):** Byte4 [amp][amp] Byte5 [amp][amp] Byte6 [amp][amp] Byte7. Register Attribute: Dynamic.

11.1.66 RP PIO Header Log Register DW3 (RPPIOHLR_DW3) - Offset A28h

Size: 32 bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + A28h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**3rd dWord of TLP (DW3):** Byte8 [amp][amp] Byte9 [amp][amp] Byte10 [amp][amp] Byte11. Register Attribute: Dynamic.

11.1.67 RP PIO Header Log Register DW4 (RPPIOHLR_DW4) - Offset A2Ch

Size: 32 bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + A2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**4th dWord of TLP (DW4):** Byte12 [amp][amp] Byte13 [amp][amp] Byte14 [amp][amp] Byte15. Register Attribute: Dynamic.

11.1.68 Secondary PCI Express Extended Capability Header (SPEECH) - Offset A30h

Size: 32 bits

Note: When operating in Mobile Express mode, this capability should not be enabled.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + A30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 1h to this register else it should write 0
15:0	0000h RW/O	**PCI Express Extended Capability ID (PCIEECID):** PCI Express Extended Capability ID (PCIEECID): This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the Secondary PCI Express Extended Capability is 0019h. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 0019h to this register else it should write 0.

11.1.69 Link Control 3 (LCTL3) - Offset A34h

This is Link Control 3 register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + A34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:9	00h RO	**Enable Lower SKP OS Generation Vector (ELSOSGV):** Enable Lower SKP OS Generation Vector (ELSOSGV): When the Link is in L0 and the bit in this field corresponding to the current Link speed is Set, SKP Ordered Sets are scheduled at the rate defined for SRNS, overriding the rate required based on the clock tolerance architecture. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is Set in this field and the corresponding bit in the Lower SKP OS Generation Supported Speeds Vector is not set.
8:2	0h RO	**Reserved**
1	0h RW	**Link Equalization Request Interrupt Enable (LERIE):** Link Equalization Request Interrupt Enable (LERIE): When set, this bit enables the generation of an interrupt to indicate that the Link Equalization Request bit has been set.
0	0h RW	**Perform Equalization (PE):** Perform Equalization (PE): When this bit is 1b and Link Retrain bit is set with the Target Link Speed field set to 8 GT/s, the Downstream Port must perform Link Equalization. This bit is cleared by Root Port upon entry to Link Equalization.

11.1.70 Lane Error Status (LES) - Offset A38h

The Lane number is the default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during training. Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + A38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW/1C/V/P	**Lane 3 Error Status (L3ES):** Lane 3 Error Status (L3ES): Lane 3 detected a Lane-based error.
2	0h RW/1C/V/P	**Lane 2 Error Status (L2ES):** Lane 2 Error Status (L2ES): Lane 2 detected a Lane-based error.
1	0h RW/1C/V/P	**Lane 1 Error Status (L1ES):** Lane 1 Error Status (L1ES): Lane 1 detected a Lane-based error.
0	0h RW/1C/V/P	**Lane 0 Error Status (L0ES):** Lane 0 Error Status (L0ES): Lane 0 detected a Lane-based error.

11.1.71 Lane 0 And Lane 1 Equalization Control (L01EC) - Offset A3Ch

Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training. Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + A3Ch	7F7F7F7Fh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 1 Receiver Preset Hint (UPL1RPH):** Upstream Port Lane 1 Receiver Preset Hint (UPL1RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalizatio
27:24	Fh RW	**Upstream Port Lane 1 Transmitter Preset (UPL1TP):** Upstream Port Lane 1 Transmitter Preset (UPL1TP): Field contains the Transmit Preset value sent or received during Link Equalization.
23	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
22:20	7h RW	**Downstream Port Lane 1 Receiver Preset Hint (DPL1RPH):** Downstream Port Lane 1 Receiver Preset Hint (DPL1RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 1 Transmitter Preset (DPL1TP):** Downstream Port Lane 1 Transmitter Preset (DPL1TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 0 Receiver Preset Hint (UPL0RPH):** Upstream Port Lane 0 Receiver Preset Hint (UPL0RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
11:8	Fh RW	**Upstream Port Lane 0 Transmitter Preset (UPL0TP):** Upstream Port Lane 0 Transmitter Preset (UPL0TP): Field contains the Transmit Preset value sent or received during Link Equalization.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 0 Receiver Preset Hint (DPL0RPH):** Downstream Port Lane 0 Receiver Preset Hint (DPL0RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 0 Transmitter Preset (DPL0TP):** Downstream Port Lane 0 Transmitter Preset (DPL0TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

11.1.72 Lane 2 And Lane 3 Equalization Control (L23EC) - Offset A40h

Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training. Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:28, F:0] + A40h	7F7F7F7Fh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 3 Receiver Preset Hint (UPL3RPH):** Upstream Port Lane 3 Receiver Preset Hint (UPL3RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
27:24	Fh RW	**Upstream Port Lane 3 Transmitter Preset (UPL3TP):** Upstream Port Lane 3 Transmitter Preset (UPL3TP): Field contains the Transmit Preset value sent or received during Link Equalization.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 3 Receiver Preset Hint (DPL3RPH):** Downstream Port Lane 3 Receiver Preset Hint (DPL3RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 3 Transmitter Preset (DPL3TP):** Downstream Port Lane 3 Transmitter Preset (DPL3TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 2 Receiver Preset Hint (UPL2RPH):** Upstream Port Lane 2 Receiver Preset Hint (UPL2RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
11:8	Fh RW	**Upstream Port Lane 2 Transmitter Preset (UPL2TP):** Upstream Port Lane 2 Transmitter Preset (UPL2TP): Field contains the Transmit Preset value sent or received during Link Equalization.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 2 Receiver Preset Hint (DPL2RPH):** Downstream Port Lane 2 Receiver Preset Hint (DPL2RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 2 Transmitter Preset (DPL2TP):** Downstream Port Lane 2 Transmitter Preset (DPL2TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

12 embedded Multi Media Card (eMMC) Controller

12.1 eMMC Configuration Registers Summary

This chapter records the registers in Bus: 0, Device 26, Function 0.

Table 12-1. Summary of Bus: 0, Device: 26, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	REG DEVVENDID (DEVVENDID)	4B478086h
4h	4	REG STATUSCOMMAND (STATUSCOMMAND)	00100000h
8h	4	REG REVCLASSCODE (REVCLASSCODE)	08050100h
Ch	4	REG CLLATHEADERBIST (CLLATHEADERBIST)	00800000h
10h	4	REG BAR (BAR)	00000004h
14h	4	REG BAR_HIGH (BAR_HIGH)	00000000h
18h	4	REG BAR1 (BAR1)	00000004h
1Ch	4	REG BAR1_HIGH (BAR1_HIGH)	00000000h
2Ch	4	REG SUBSYSTEMID (SUBSYSTEMID)	00000000h
30h	4	REG EXPANSION_ROM_BASEADDR (EXPANSION_ROM_BASEADDR)	00000000h
34h	4	REG CAPABILITYPTR (CAPABILITYPTR)	00000080h
3Ch	4	REG INTERRUPTREG (INTERRUPTREG)	00000000h
80h	4	REG POWERCAPID (POWERCAPID)	00039001h
84h	4	REG PMECTRLSTATUS (PMECTRLSTATUS)	00000008h
90h	4	REG PCIDEVIDLE_CAP_RECORD (PCIDEVIDLE_CAP_RECORD)	F0140009h
94h	4	REG DEVID_VEND_SPECIFIC_REG (DEVID_VEND_SPECIFIC_REG)	01400010h
98h	4	REG D0I3_CONTROL_SW_LTR_MMIO_REG (D0I3_CONTROL_SW_LTR_MMIO_REG)	00008041h
9Ch	4	REG DEVICE_IDLE_POINTER_REG (DEVICE_IDLE_POINTER_REG)	000081C1h
A0h	4	REG D0I3_MAX_POW_LAT_PG_CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG)	00290800h
B0h	4	REG GEN_REGRW1 (GEN_REGRW1)	00000000h
B4h	4	REG GEN_REGRW2 (GEN_REGRW2)	00000000h
B8h	4	REG GEN_REGRW3 (GEN_REGRW3)	00000000h
BCh	4	REG GEN_REGRW4 (GEN_REGRW4)	00000000h
C0h	4	REG GEN_INPUT_REG (GEN_INPUT_REG)	00000000h
F8h	4	REG MANID (MANID)	0000000Fh

12.1.1 REG DEVVENDID (DEVVENDID) - Offset 0h

Vendor ID Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 0h	4B478086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4B47h RO	**DEVICEID:** DEVICEID
15:0	8086h RO	**VENDORID:** VENDORID

12.1.2 REG STATUSCOMMAND (STATUSCOMMAND) - Offset 4h

PCI Command Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW/1C	**RMA:** RMA
28	0h RW/1C	**RTA:** RTA
27:21	0h RO	**Reserved**
20	1h RO	**CAPLIST:** CAPLIST
19	0h RO	**INTR_STATUS:** INTR_STATUS
18:11	0h RO	**Reserved**
10	0h RW	**INTR_DISABLE:** INTR_DISABLE
9	0h RO	**Reserved**
8	0h RW	**SERR_ENABLE:** SERR_ENABLE
7:3	0h RO	**Reserved**
2	0h RW	**BME:** BME
1	0h RW	**MSE:** MSE
0	0h RO	**Reserved**

12.1.3 REG REVCLASSCODE (REVCLASSCODE) - Offset 8h

Revision Id Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 8h	08050100h

Bit Range	Default & Access	Field Name (ID): Description
31:8	080501h RO	**CLASS_CODES:** CLASS_CODES
7:0	00h RO	**RID:** RID

12.1.4 REG CLLATHEADERBIST (CLLATHEADERBIST) - Offset Ch

Cache Line Latency Header and BIST Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + Ch	00800000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	1h RO	**MULFNDEV:** MULFNDEV
22:16	00h RO	**HEADERTYPE:** HEADERTYPE
15:8	00h RO	**LATTIMER:** LATTIMER
7:0	00h RW	**CACHELINE_SIZE:** CACHELINE_SIZE

12.1.5 REG BAR (BAR) - Offset 10h

BAR - Base Address Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 10h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**BASEADDR:** BASEADDR
11:4	00h RO	**SIZEINDICATOR:** SIZEINDICATOR
3	0h RO	**PREFETCHABLE:** PREFETCHABLE
2:1	2h RO	**TYPE:** TYPE
0	0h RO	**MESSAGE_SPACE:** MESSAGE_SPACE

12.1.6 REG BAR_HIGH (BAR_HIGH) - Offset 14h

BAR - Base Address Register High

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**BASEADDR_HIGH:** BASEADDR_HIGH

12.1.7 REG BAR1 (BAR1) - Offset 18h

BAR1 - Base Address Register1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 18h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**BASEADDR1:** BASEADDR1
11:4	00h RO	**SIZEINDICATOR1:** SIZEINDICATOR1
3	0h RO	**PREFETCHABLE1:** PREFETCHABLE1
2:1	2h RO	**TYPE1:** TYPE1
0	0h RO	**MESSAGE_SPACE1:** MESSAGE_SPACE1

12.1.8 REG BAR1_HIGH (BAR1_HIGH) - Offset 1Ch

BAR1 - Base Address Register1 High

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**BASEADDR1_HIGH:** BASEADDR1_HIGH

12.1.9 REG SUBSYSTEMID (SUBSYSTEMID) - Offset 2Ch

SUBSYSTEMID - Subsystem Vendor and Subsystem ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**SUBSYSTEMID:** SUBSYSTEMID
15:0	0000h RW/O	**SUBSYSTEMVENDORID:** SUBSYSTEMVENDORID

12.1.10 REG EXPANSION_ROM_BASEADDR (EXPANSION_ROM_BASEADDR) - Offset 30h

Expansion ROM Base Address Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** EXPANSION_ROM_BASE

12.1.11 REG CAPABILITYPTR (CAPABILITYPTR) - Offset 34h

Capabilities Pointer Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**CAPPTR_POWER:** CAPPTR_POWER

12.1.12 REG INTERRUPTREG (INTERRUPTREG) - Offset 3Ch

Interrupt Line Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**MAX_LAT:** MAX_LAT
23:16	00h RO	**MIN_GNT:** MIN_GNT
15:12	0h RO	**Reserved**
11:8	0h RO	**INTPIN:** INTPIN
7:0	00h RW	**INTLINE:** INTLINE

12.1.13 REG POWERCAPID (POWERCAPID) - Offset 80h

Power Management Capability ID Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 80h	00039001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PMESUPPORT:** PMESUPPORT
26:19	0h RO	**Reserved**
18:16	3h RO	**VERSION:** VERSION
15:8	90h RO	**NXTCAP:** NXTCAP
7:0	01h RO	**POWER_CAP:** POWER_CAP

12.1.14 REG PMECTRLSTATUS (PMECTRLSTATUS) - Offset 84h

Power Management Control and Status Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C	**PMESTATUS:** PMESTATUS
14:9	0h RO	**Reserved**
8	0h RW	**PMEENABLE:** PMEENABLE
7:4	0h RO	**Reserved**
3	1h RO	**NO_SOFT_RESET:** NO_SOFT_RESET
2	0h RO	**Reserved**
1:0	0h RW	**POWERSTATE:** POWERSTATE

12.1.15 REG PCIDEVIDLE_CAP_RECORD (PCIDEVIDLE_CAP_RECORD) - Offset 90h

PCI Device Idle Capability Record Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 90h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP:** VEND_CAP
27:24	0h RO	**REVID:** REVID
23:16	14h RO	**CAP_LENGTH:** CAP_LENGTH
15:8	00h RO	**NEXT_CAP:** NEXT_CAP
7:0	09h RO	**CAPID:** CAPID

12.1.16 REG DEVID_VEND_SPECIFIC_REG (DEVID_VEND_SPECIFIC_REG) - Offset 94h

Device ID Vendor Specific Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**VSEC_LENGTH:** VSEC_LENGTH
19:16	0h RO	**VSEC_REV:** VSEC_REV
15:0	0010h RO	**VSECID:** VSECID

12.1.17 REG D0I3_CONTROL_SW_LTR_MMIO_REG (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h

SW LTR Update MMIO Location Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 98h	00008041h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000804h RO	**SW_LAT_DWORD_OFFSET:** SW_LAT_DWORD_OFFSET
3:1	0h RO	**SW_LAT_BAR_NUM:** SW_LAT_BAR_NUM
0	1h RO	**SW_LAT_VALID:** SW_LAT_VALID

12.1.18 REG DEVICE_IDLE_POINTER_REG (DEVICE_IDLE_POINTER_REG) - Offset 9Ch

Device IDLE Pointer Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 9Ch	000081C1h

Bit Range	Default & Access	Field Name (ID): Description
31:4	000081Ch RO	**DWORD_OFFSET:** DWORD_OFFSET
3:1	0h RO	**BAR_NUM:** BAR_NUM
0	1h RO	**VALID:** VALID

12.1.19 REG D0I3_MAX_POW_LAT_PG_CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h

Doi3 Max Power On Latency

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + A0h	00290800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	1h RW	**HAE:** HAE
20	0h RO	**Reserved**
19	1h RW	**SLEEP_EN:** SLEEP_EN

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**PGE:** PGE
17	0h RW	**I3_ENABLE:** I3_ENABLE
16	1h RW	**PMCRE:** PMCRE
15:13	0h RO	**Reserved**
12:10	2h RW/O	**POW_LAT_SCALE:** POW_LAT_SCALE
9:0	000h RW/O	**POW_LAT_VALUE:** POW_LAT_VALUE

12.1.20 REG GEN_REGRW1 (GEN_REGRW1) - Offset B0h

General Purpose PCI RW Register1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW1:** GEN_REG_RW1

12.1.21 REG GEN_REGRW2 (GEN_REGRW2) - Offset B4h

General Purpose PCI RW Register2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW2:** GEN_REG_RW2

12.1.22 REG GEN_REGRW3 (GEN_REGRW3) - Offset B8h

General Purpose PCI RW Register3

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW3:** GEN_REG_RW3

12.1.23 REG GEN_REGRW4 (GEN_REGRW4) - Offset BCh

General Purpose PCI RW Register4

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW4:** GEN_REG_RW4

12.1.24 REG GEN_INPUT_REG (GEN_INPUT_REG) - Offset C0h

General Input Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**GEN_REG_INPUT_RW:** GEN_REG_INPUT_RW

12.1.25 REG MANID (MANID) - Offset F8h

Manufacturers ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + F8h	0000000Fh

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000Fh RO	**MANID:** MANID

12.2 eMMC Memory Mapped Registers Summary

Table 12-2. Summary of eMMC Memory Mapped Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	SDMASYSADDR Reg (SDMASYSADDR)	00000000h
4h	2	BLOCKSIZE Reg (BLOCKSIZE)	0000h
6h	2	BLOCKCOUNT Reg (BLOCKCOUNT)	0000h
8h	4	ARGUMENT1 Reg (ARGUMENT1)	00000000h
Ch	2	TRANSFERMODE Reg (TRANSFERMODE)	0000h
Eh	2	COMMAND Reg (COMMAND)	0000h
10h	4	RESPONSE01 Reg (RESPONSE01)	00000000h
14h	2	RESPONSE2 Reg (RESPONSE2)	0000h
16h	2	RESPONSE3 Reg (RESPONSE3)	0000h
18h	2	RESPONSE4 Reg (RESPONSE4)	0000h
1Ah	2	RESPONSE5 Reg (RESPONSE5)	0000h
1Ch	2	RESPONSE6 Reg (RESPONSE6)	0000h
1Eh	2	RESPONSE7 Reg (RESPONSE7)	0000h
20h	4	DATAPORT Reg (DATAPORT)	00000000h
24h	4	PRESENTSTATE Reg (PRESENTSTATE)	1FF00000h
28h	1	HOSTCONTROL1 Reg (HOSTCONTROL1)	00h
29h	1	POWERCONTROL Reg (POWERCONTROL)	00h
2Ah	1	BLOCKGAPCONTROL Reg (BLOCKGAPCONTROL)	80h
2Bh	1	WAKEUPCONTROL Reg (WAKEUPCONTROL)	00h
2Ch	2	CLOCKCONTROL Reg (CLOCKCONTROL)	0000h
2Eh	1	TIMEOUTCONTROL Reg (TIMEOUTCONTROL)	00h
2Fh	1	SOFTWARERESET Reg (SOFTWARERESET)	00h
30h	2	NORMALINTRSTS Reg (NORMALINTRSTS)	0000h
32h	2	ERRORINSTRSTS Reg (ERRORINSTRSTS)	0000h
34h	2	NORMALINTRSTSENA Reg (NORMALINTRSTSENA)	0000h
36h	2	ERRORINTRSTSENA Reg (ERRORINTRSTSENA)	0000h
38h	2	NORMALINTRSIGENA Reg (NORMALINTRSIGENA)	0000h
3Ah	2	ERRORINTRSIGENA Reg (ERRORINTRSIGENA)	0000h
3Ch	2	AUTOCMDERRSTS Reg (AUTOCMDERRSTS)	0000h
3Eh	2	HOSTCONTROL2 Reg (HOSTCONTROL2)	0000h
40h	8	CAPABILITIES Reg (CAPABILITIES)	800000075 46EC881h
48h	8	MAXCURRENTCAP Reg (MAXCURRENTCAP)	000000000 0000000h
50h	2	FORCEVENTFORAUTOCMDERRORSTATUS Reg (FORCEVENTFORAUTOCMDERRORSTATUS)	0000h
52h	2	FORCEEVENTFORERRINTSTS Reg (FORCEEVENTFORERRINTSTS)	0000h
54h	1	ADMAERRSTS Reg (ADMAERRSTS)	00h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
58h	4	ADMASYSADDR1 Reg (ADMASYSADDR1)	00000000h
5Ch	2	ADMASYSADDR2 Reg (ADMASYSADDR2)	0000h
60h	2	PRESETVALUE0 Reg (PRESETVALUE0)	0004h
62h	2	PRESETVALUE1 Reg (PRESETVALUE1)	0004h
64h	2	PRESETVALUE2 Reg (PRESETVALUE2)	0002h
66h	2	PRESETVALUE3 Reg (PRESETVALUE3)	0004h
68h	2	PRESETVALUE4 Reg (PRESETVALUE4)	0002h
6Ah	2	PRESETVALUE5 Reg (PRESETVALUE5)	0001h
6Ch	2	PRESETVALUE6 Reg (PRESETVALUE6)	0000h
6Eh	2	PRESETVALUE7 Reg (PRESETVALUE7)	0002h
70h	4	BOOTTIMEOUTCNT Reg (BOOTTIMEOUTCNT)	00000000h
FCh	2	SLOTINTRSTS Reg (SLOTINTRSTS)	0000h

12.2.1 SDMASYSADDR Reg (SDMASYSADDR) - Offset 0h

SDMA_SYSADDRESS

Type	Size	Offset	Default
MMIO	32 bit	BAR + 0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SDMA_SYSADDRESS:** SDMA_SYSADDRESS

12.2.2 BLOCKSIZE Reg (BLOCKSIZE) - Offset 4h

Type	Size	Offset	Default
MMIO	16 bit	BAR + 4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14:12	0h RW	**HOST_SDMA_BUF_SIZE:** HOST_SDMA_BUF_SIZE
11:0	000h RW	**XFER_BLOCKSIZE:** XFER_BLOCKSIZE

12.2.3 BLOCKCOUNT Reg (BLOCKCOUNT) - Offset 6h

BLOCK_CNT_16BIT

Type	Size	Offset	Default
MMIO	16 bit	BAR + 6h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**BLOCK_CNT_16BIT:** BLOCK_CNT_16BIT

12.2.4 ARGUMENT1 Reg (ARGUMENT1) - Offset 8h

COMMAND_ARGUMENT1

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**COMMAND_ARGUMENT1:** COMMAND_ARGUMENT1

12.2.5 TRANSFERMODE Reg (TRANSFERMODE) - Offset Ch

Type	Size	Offset	Default
MMIO	16 bit	BAR + Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RW	**XFERMODE_MULTIBLKSEL:** XFERMODE_MULTIBLKSEL
4	0h RW	**XFERMODE_DATAXFERDIR:** XFERMODE_DATAXFERDIR
3:2	0h RW	**XFERMODE_AUTOCMDENA:** XFERMODE_AUTOCMDENA
1	0h RW	**XFERMODE_BLKCNTENA:** XFERMODE_BLKCNTENA
0	0h RW	**XFERMODE_DMAENABLE:** XFERMODE_DMAENABLE

12.2.6 COMMAND Reg (COMMAND) - Offset Eh

Type	Size	Offset	Default
MMIO	16 bit	BAR + Eh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Reserved**
13:8	00h RW	**COMMAND_CMDINDEX:** COMMAND_CMDINDEX
7:6	0h RW	**COMMAND_CMDTYPE:** COMMAND_CMDTYPE
5	0h RW	**COMMAND_DATAPRESENT:** COMMAND_DATAPRESENT
4	0h RW	**COMMAND_INDEXCHKENA:** COMMAND_INDEXCHKENA
3	0h RW	**COMMAND_CRCCHKENA:** COMMAND_CRCCHKENA
2	0h RO	**Reserved**
1:0	0h RW	**COMMAND_RESPONSETYPE:** COMMAND_RESPONSETYPE

12.2.7 RESPONSE01 Reg (RESPONSE01) - Offset 10h

COMMAND_RESPONSE_31_0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**COMMAND_RESPONSE_31_0:** COMMAND_RESPONSE_31_0

12.2.8 RESPONSE2 Reg (RESPONSE2) - Offset 14h

COMMAND_RESPONSE_47_32

Type	Size	Offset	Default
MMIO	16 bit	BAR + 14h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**COMMAND_RESPONSE_47_32:** COMMAND_RESPONSE_47_32

12.2.9 RESPONSE3 Reg (RESPONSE3) - Offset 16h

COMMAND_RESPONSE_63_48

Type	Size	Offset	Default
MMIO	16 bit	BAR + 16h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**COMMAND_RESPONSE_63_48:** COMMAND_RESPONSE_63_48

12.2.10 RESPONSE4 Reg (RESPONSE4) - Offset 18h

COMMAND_RESPONSE_79_64

Type	Size	Offset	Default
MMIO	16 bit	BAR + 18h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**COMMAND_RESPONSE_79_64:** COMMAND_RESPONSE_79_64

12.2.11 RESPONSE5 Reg (RESPONSE5) - Offset 1Ah

COMMAND_RESPONSE_95_80

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1Ah	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**COMMAND_RESPONSE_95_80:** COMMAND_RESPONSE_95_80

12.2.12 RESPONSE6 Reg (RESPONSE6) - Offset 1Ch

COMMAND_RESPONSE_111_96

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**COMMAND_RESPONSE_111_96:** COMMAND_RESPONSE_111_96

12.2.13 RESPONSE7 Reg (RESPONSE7) - Offset 1Eh

COMMAND_RESPONSE_127_112

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1Eh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**COMMAND_RESPONSE_127_112:** COMMAND_RESPONSE_127_112

12.2.14 DATAPORT Reg (DATAPORT) - Offset 20h

SDHCDMACTRL_PIOBUFRDDATA

Type	Size	Offset	Default
MMIO	32 bit	BAR + 20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SDHCDMACTRL_PIOBUFRDDATA:** SDHCDMACTRL_PIOBUFRDDATA

12.2.15 PRESENTSTATE Reg (PRESENTSTATE) - Offset 24h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 24h	1FF00000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:25	Fh RO/V	**SDIF_DAT4IN_DSYNC:** SDIF_DAT4IN_DSYNC
24	1h RO/V	**SDIF_CMDIN_DSYNC:** SDIF_CMDIN_DSYNC
23:20	Fh RO/V	**SDIF_DAT0IN_DSYNC:** SDIF_DAT0IN_DSYNC
19	0h RO/V	**SDIF_WP_DSYNC:** SDIF_WP_DSYNC
18	0h RO/V	**SDIF_CD_N_DSYNC:** SDIF_CD_N_DSYNC
17	0h RO/V	**SDHCCARDDET_STATESTABLE_DSYNC:** SDHCCARDDET_STATESTABLE_DSYNC
16	0h RO/V	**SDHCCARDDET_INSERTED_DSYNC:** SDHCCARDDET_INSERTED_DSYNC
15:12	0h RO	**Reserved**
11	0h RO/V	**SDHCDMACTRL_PIOBUFRDENA:** SDHCDMACTRL_PIOBUFRDENA
10	0h RO/V	**SDHCDMACTRL_PIOBUFWRENA:** SDHCDMACTRL_PIOBUFWRENA
9	0h RO/V	**SDHCDMACTRL_RDXFERACTIVE:** SDHCDMACTRL_RDXFERACTIVE
8	0h RO/V	**SDHCDMACTRL_WRXFERACTIVE:** SDHCDMACTRL_WRXFERACTIVE
7:4	0h RO	**Reserved**
3	0h RO/V	**SDHCSDCTRL_RETUNINGREQ_DSYNC:** SDHCSDCTRL_RETUNINGREQ_DSYNC
2	0h RO/V	**SDHCDMACTRL_DATALINEACTIVE:** SDHCDMACTRL_DATALINEACTIVE
1	0h RO/V	**PRESENTSTATE_INHIBITDAT:** PRESENTSTATE_INHIBITDAT
0	0h RO/V	**PRESENTSTATE_INHIBITCMD:** PRESENTSTATE_INHIBITCMD

12.2.16 HOSTCONTROL1 Reg (HOSTCONTROL1) - Offset 28h

HOSTCTRL1_CDSIGSELECT

Type	Size	Offset	Default
MMIO	8 bit	BAR + 28h	00h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**HOSTCTRL1_CDSIGSELECT:** HOSTCTRL1_CDSIGSELECT
6	0h RW	**HOSTCTRL1_CDTESTLEVEL:** HOSTCTRL1_CDTESTLEVEL
5	0h RW	**HOSTCTRL1_EXTDATAWIDTH:** HOSTCTRL1_EXTDATAWIDTH
4:3	0h RW	**HOSTCTRL1_DMASELECT:** HOSTCTRL1_DMASELECT
2	0h RW	**HOSTCTRL1_HIGHSPEEDENA:** HOSTCTRL1_HIGHSPEEDENA
1	0h RW	**HOSTCTRL1_DATAWIDTH:** HOSTCTRL1_DATAWIDTH
0	0h RW	**HOSTCTRL1_LEDCONTROL:** HOSTCTRL1_LEDCONTROL

12.2.17 POWERCONTROL Reg (POWERCONTROL) - Offset 29h

Type	Size	Offset	Default
MMIO	8 bit	BAR + 29h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Reserved**
4	0h RW	**EMMC_HWRESET:** EMMC_HWRESET
3:1	0h RW	**PWRCTRL_SDBUSVOLTAGE:** PWRCTRL_SDBUSVOLTAGE
0	0h RW	**PWRCTRL_SDBUSPOWER:** PWRCTRL_SDBUSPOWER

12.2.18 BLOCKGAPCONTROL Reg (BLOCKGAPCONTROL) - Offset 2Ah

BOOT_ACK_CHK

Type	Size	Offset	Default
MMIO	8 bit	BAR + 2Ah	80h

Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**BOOT_ACK_CHK:** BOOT_ACK_CHK
6	0h RW	**ALT_BOOT_EN:** ALT_BOOT_EN
5	0h RW	**BOOT_EN:** BOOT_EN
4	0h RW	**SPI_MODE:** SPI_MODE
3	0h RW	**INTR_AT_BLOCK_GAP:** INTR_AT_BLOCK_GAP
2	0h RW	**RD_WAIT_CTRL:** RD_WAIT_CTRL
1	0h RW	**CONTINUE_REQ:** CONTINUE_REQ
0	0h RW	**STOPATBLKGAP_REQ:** STOPATBLKGAP_REQ

12.2.19 WAKEUPCONTROL Reg (WAKEUPCONTROL) - Offset 2Bh

Type	Size	Offset	Default
MMIO	8 bit	BAR + 2Bh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved**
2	0h RW	**WKUPCTRL_CARDREMOVAL:** WKUPCTRL_CARDREMOVAL
1	0h RW	**WKUPCTRL_CARDINSERTION:** WKUPCTRL_CARDINSERTION
0	0h RW	**WKUPCTRL_CARDINTERRUPT:** WKUPCTRL_CARDINTERRUPT

12.2.20 CLOCKCONTROL Reg (CLOCKCONTROL) - Offset 2Ch

CLKCTRL_SDCLKFREQSEL

Type	Size	Offset	Default
MMIO	16 bit	BAR + 2Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RW	**CLKCTRL_SDCLKFREQSEL:** CLKCTRL_SDCLKFREQSEL
7:6	0h RW	**CLKCTRL_SDCLKFREQSEL_UPPERBITS:** CLKCTRL_SDCLKFREQSEL_UPPERBITS
5	0h RW	**CLKCTRL_CLKGENSEL:** CLKCTRL_CLKGENSEL
4:3	0h RO	**Reserved**
2	0h RW	**CLKCTRL_SDCLKENA:** CLKCTRL_SDCLKENA
1	0h RO/V	**SDHCCLKGEN_INTCLKSTABLE_DSYNC:** SDHCCLKGEN_INTCLKSTABLE_DSYNC
0	0h RW	**CLKCTRL_INTCLKENA:** CLKCTRL_INTCLKENA

12.2.21 TIMEOUTCONTROL Reg (TIMEOUTCONTROL) - Offset 2Eh

Type	Size	Offset	Default
MMIO	8 bit	BAR + 2Eh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**Reserved**
3:0	0h RW	**TIMEOUT_CTRVALUE:** TIMEOUT_CTRVALUE

12.2.22 SOFTWARERESET Reg (SOFTWARERESET) - Offset 2Fh

Type	Size	Offset	Default
MMIO	8 bit	BAR + 2Fh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved**
2	0h RW	**SWRESET_FOR_DAT:** SWRESET_FOR_DAT
1	0h RW	**SWRESET_FOR_CMD:** SWRESET_FOR_CMD
0	0h RW	**SWRESET_FOR_ALL:** SWRESET_FOR_ALL

12.2.23 NORMALINTRSTS Reg (NORMALINTRSTS) - Offset 30h

REG_ERRORINTRSTS

Type	Size	Offset	Default
MMIO	16 bit	BAR + 30h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**REG_ERRORINTRSTS:** REG_ERRORINTRSTS
14	0h RW/1C	**NORMALINTRSTS_BOOTCOMPLETE:** NORMALINTRSTS_BOOTCOMPLETE
13	0h RW/1C	**NORMALINTRSTS_RCVBOOTACK:** NORMALINTRSTS_RCVBOOTACK
12	0h RO	**NORMALINTRSTS_RETUNINGEVENT:** NORMALINTRSTS_RETUNINGEVENT
11	0h RO	**NORMALINTRSTS_INTC:** NORMALINTRSTS_INTC
10	0h RO	**NORMALINTRSTS_INTB:** NORMALINTRSTS_INTB
9	0h RO	**NORMALINTRSTS_INTA:** NORMALINTRSTS_INTA
8	0h RO	**NORMALINTRSTS_CARDINTSTS:** NORMALINTRSTS_CARDINTSTS
7	0h RW/1C	**NORMALINTRSTS_CARDREMSTS:** NORMALINTRSTS_CARDREMSTS
6	0h RW/1C	**NORMALINTRSTS_CARDINSSTS:** NORMALINTRSTS_CARDINSSTS
5	0h RW/1C	**NORMALINTRSTS_BUFRDREADY:** NORMALINTRSTS_BUFRDREADY
4	0h RW/1C	**NORMALINTRSTS_BUFWRREADY:** NORMALINTRSTS_BUFWRREADY
3	0h RW/1C	**NORMALINTRSTS_DMAINTERRUPT:** NORMALINTRSTS_DMAINTERRUPT

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**NORMALINTRSTS_BLKGAPEVENT:** NORMALINTRSTS_BLKGAPEVENT
1	0h RW/1C	**NORMALINTRSTS_XFERCOMPLETE:** NORMALINTRSTS_XFERCOMPLETE
0	0h RW/1C	**NORMALINTRSTS_CMDCOMPLETE:** NORMALINTRSTS_CMDCOMPLETE

12.2.24 ERRORINSTRSTS Reg (ERRORINSTRSTS) - Offset 32h

Type	Size	Offset	Default
MMIO	16 bit	BAR + 32h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**Reserved**
12	0h RW/1C	**ERRORINTRSTS_HOSTERROR:** ERRORINTRSTS_HOSTERROR
11:10	0h RO	**Reserved**
9	0h RW/1C	**ERRORINTRSTS_ADMAERROR:** ERRORINTRSTS_ADMAERROR
8	0h RW/1C	**ERRORINTRSTS_AUTOCMDERROR:** ERRORINTRSTS_AUTOCMDERROR
7	0h RW/1C	**ERRORINTRSTS_CURRLIMITERROR:** ERRORINTRSTS_CURRLIMITERROR
6	0h RW/1C	**ERRORINTRSTS_DATAENDBITERROR:** ERRORINTRSTS_DATAENDBITERROR
5	0h RW/1C	**ERRORINTRSTS_DATACRCERROR:** ERRORINTRSTS_DATACRCERROR
4	0h RW/1C	**ERRORINTRSTS_DATATIMEOUTERROR:** ERRORINTRSTS_DATATIMEOUTERROR
3	0h RW/1C	**ERRORINTRSTS_CMDINDEXERROR:** ERRORINTRSTS_CMDINDEXERROR
2	0h RW/1C	**ERRORINTRSTS_CMDENDBITERROR:** ERRORINTRSTS_CMDENDBITERROR
1	0h RW/1C	**ERRORINTRSTS_CMDCRCERROR:** ERRORINTRSTS_CMDCRCERROR
0	0h RW/1C	**ERRORINTRSTS_CMDTIMEOUTERROR:** ERRORINTRSTS_CMDTIMEOUTERROR

12.2.25 NORMALINTRSTSENA Reg (NORMALINTRSTSENA) - Offset 34h

Type	Size	Offset	Default
MMIO	16 bit	BAR + 34h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RW	**BOOTINTR_ENA:** BOOTINTR_ENA
13	0h RW	**BOOTACK_RCVENA:** BOOTACK_RCVENA
12	0h RW	**RETUNE_EVENTSTSENA:** RETUNE_EVENTSTSENA
11	0h RW	**INT_C_STSENA:** INT_C_STSENA
10	0h RW	**INT_B_STSENA:** INT_B_STSENA
9	0h RW	**INT_A_STSENA:** INT_A_STSENA
8	0h RW	**SDHCREGSET_CARDINTSTSENA:** SDHCREGSET_CARDINTSTSENA
7	0h RW	**SDHCREGSET_CARDREMSTSENA:** SDHCREGSET_CARDREMSTSENA
6	0h RW	**SDHCREGSET_CARDINSSTSENA:** SDHCREGSET_CARDINSSTSENA
5	0h RW	**BUFFRD_READTSTSENA:** BUFFRD_READTSTSENA
4	0h RW	**BUFFWR_READTSTSENA:** BUFFWR_READTSTSENA
3	0h RW	**DMAINTRSTSENA:** DMAINTRSTSENA
2	0h RW	**BLOCKGAP_EVENTSTSENA:** BLOCKGAP_EVENTSTSENA
1	0h RW	**XFRCMPLTSTSENA:** XFRCMPLTSTSENA
0	0h RW	**CMDCMPLTSTSENA:** CMDCMPLTSTSENA

12.2.26 ERRORINTRSTSENA Reg (ERRORINTRSTSENA) - Offset 36h

Type	Size	Offset	Default
MMIO	16 bit	BAR + 36h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**Reserved**
12	0h RO	**XFRRESPONCE_ERR:** XFRRESPONCE_ERR
11	0h RO	**Reserved**
10	0h RW	**TUNE_ERRSTSENA:** TUNE_ERRSTSENA
9	0h RW	**ADMA_ERRSTSENA:** ADMA_ERRSTSENA
8	0h RW	**AUTOCMD12_ERRSTSENA:** AUTOCMD12_ERRSTSENA
7	0h RW	**CURRENTLIM_ERRSTSENA:** CURRENTLIM_ERRSTSENA
6	0h RW	**DATAENDBIT_ERRSTSENA:** DATAENDBIT_ERRSTSENA
5	0h RW	**DATACRC_ERRSTSENA:** DATACRC_ERRSTSENA
4	0h RW	**DATATIMEOUT_ERRSTSENA:** DATATIMEOUT_ERRSTSENA
3	0h RW	**CMDINDEX_ERRSTSENA:** CMDINDEX_ERRSTSENA
2	0h RW	**CMDENDBIT_ERRSTSENA:** CMDENDBIT_ERRSTSENA
1	0h RW	**CMDCRC_ERRSTSENA:** CMDCRC_ERRSTSENA
0	0h RW	**CMDTIMEOUT_ERRSTSENA:** CMDTIMEOUT_ERRSTSENA

12.2.27 NORMALINTRSIGENA Reg (NORMALINTRSIGENA) - Offset 38h

FIXED_TO_0

Type	Size	Offset	Default
MMIO	16 bit	BAR + 38h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**FIXED_TO_0:** FIXED_TO_0
14	0h RW	**BOOTINTR_SIGENA:** BOOTINTR_SIGENA
13	0h RW	**BOOTACK_RCVSIGENA:** BOOTACK_RCVSIGENA
12	0h RW	**RETUNE_EVENTSIGENA:** RETUNE_EVENTSIGENA
11	0h RW	**INT_C_SIGENA:** INT_C_SIGENA
10	0h RW	**INT_B_SIGENA:** INT_B_SIGENA
9	0h RW	**INT_A_SIGENA:** INT_A_SIGENA
8	0h RW	**SDHCREGSET_CARDINTSTSENA:** SDHCREGSET_CARDINTSTSENA
7	0h RW	**SDHCREGSET_CARDREMSTSENA:** SDHCREGSET_CARDREMSTSENA
6	0h RW	**SDHCREGSET_CARDINSSTSENA:** SDHCREGSET_CARDINSSTSENA
5	0h RW	**BUFFRD_READTSIGENA:** BUFFRD_READTSIGENA
4	0h RW	**BUFFWR_READTSIGENA:** BUFFWR_READTSIGENA
3	0h RW	**DMAINTRSIGENA:** DMAINTRSIGENA
2	0h RW	**BLOCKGAP_EVENTSIGENA:** BLOCKGAP_EVENTSIGENA
1	0h RW	**XFRCMPLTSIGENA:** XFRCMPLTSIGENA
0	0h RW	**CMDCMPLTSIGENA:** CMDCMPLTSIGENA

12.2.28 ERRORINTRSIGENA Reg (ERRORINTRSIGENA) - Offset 3Ah

Type	Size	Offset	Default
MMIO	16 bit	BAR + 3Ah	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**Reserved**
12	0h RO	**XFRRESPONCE_SIGERR:** XFRRESPONCE_SIGERR
11	0h RO	**Reserved**
10	0h RW	**TUNE_ERRSIGENA:** TUNE_ERRSIGENA
9	0h RW	**ADMA_ERRSIGENA:** ADMA_ERRSIGENA
8	0h RW	**AUTOCMD12_ERRSIGENA:** AUTOCMD12_ERRSIGENA
7	0h RW	**CURRENTLIM_ERRSIGENA:** CURRENTLIM_ERRSIGENA
6	0h RW	**DATAENDBIT_ERRSIGENA:** DATAENDBIT_ERRSIGENA
5	0h RW	**DATACRC_ERRSIGENA:** DATACRC_ERRSIGENA
4	0h RW	**DATATIMEOUT_ERRSIGENA:** DATATIMEOUT_ERRSIGENA
3	0h RW	**CMDINDEX_ERRSIGENA:** CMDINDEX_ERRSIGENA
2	0h RW	**CMDENDBIT_ERRSIGENA:** CMDENDBIT_ERRSIGENA
1	0h RW	**CMDCRC_ERRSIGENA:** CMDCRC_ERRSIGENA
0	0h RW	**CMDTIMEOUT_ERRSIGENA:** CMDTIMEOUT_ERRSIGENA

12.2.29 AUTOCMDERRSTS Reg (AUTOCMDERRSTS) - Offset 3Ch

Type	Size	Offset	Default
MMIO	16 bit	BAR + 3Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7	0h RO	**AUTOCMDERRSTS_NEXTERROR:** AUTOCMDERRSTS_NEXTERROR
6:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**AUTOCMDERRSTS_INDEXERROR:** AUTOCMDERRSTS_INDEXERROR
3	0h RO	**AUTOCMDERRSTS_ENDBITERROR:** AUTOCMDERRSTS_ENDBITERROR
2	0h RO	**AUTOCMDERRSTS_CRCERROR:** AUTOCMDERRSTS_CRCERROR
1	0h RO	**AUTOCMDERRSTS_TIMEOUTERROR:** AUTOCMDERRSTS_TIMEOUTERROR
0	0h RO	**AUTOCMDERRSTS_NOTEXECERROR:** AUTOCMDERRSTS_NOTEXECERROR

12.2.30 HOSTCONTROL2 Reg (HOSTCONTROL2) - Offset 3Eh

HOSTCTRL2_PRESETVALUEENABLE

Type	Size	Offset	Default
MMIO	16 bit	BAR + 3Eh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**HOSTCTRL2_PRESETVALUEENABLE:** Preset Value Enable Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When Preset Value Enable is set to automatic. This bit enables the functions defined in the Preset Value registers. 1 Automatic Selection by Preset Value are Enabled 0 SDCLK and Driver Strength are controlled by Host Driver If this bit is set to 0, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Driver. If this bit is set to 1, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Controller as specified in the Preset Value registers
14	0h RW	**HOSTCTRL2_ASYNCHINTRENABLE:** Asynchronous Interrupt Enable This bit can be set to 1 if a card support asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode (and zero is set to Interrupt Pin Select in the Shared Bus Control register). If this bit is set to 1, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver Card Interrupt to the host when it is asserted by the Card. 0 – Disabled 1 – Enabled
13:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**HOSTCTRL2_DRIVERSTRENGTH:** Driver Strength This is the programmed Drive Strength output and it[2] of the sdhccore_drivestrength value
8	0h RO	**Reserved**
7	0h RW	**HOSTCTRL2_SAMPLINGCLKSELECT:** Sampling Clock Select This bit is set by tuning procedure when Execute Tuning is cleared. Writing 1 to this bit is meaningless and ignored. Setting 1 means that tuning is completed successfully and setting 0 means that tuning is failed. Host Controller uses this bit to select sampling clock to receive CMD and DAT. This bit is cleared by writing 0. Change of this bit is not allowed while the Host Controller is receiving response or a read data block. 0 - Fixed clock is used to sample data 1 - Tuned clock is used to sample data
6	0h RW	**HOSTCTRL2_EXECUTETUNING:** Execute Tuning This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select. Tuning procedure is aborted by writing 0 for more detail about tuning procedure. 0 - Not Tuned or Tuning Completed 1 - Execute Tuning

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**HOSTCTRL2_DRIVERSTRENGTHSEL:** Driver Strength Select Host Controller output driver in 1.8V signaling is selected by this bit. In 3.3V signaling, this field is not effective. This field can be set depends on Driver Type A, C and D support bits in the Capabilities register. This bit depends on setting of Preset Value Enable. If Preset Value Enable = 0, this field is set by Host Driver. If Preset Value Enable = 1, this field is automatically set by a value specified in the one of Preset Value registers. 00b Driver Type B is Selected (Default) 01b Driver Type A is Selected 10b Driver Type C is Selected 11b Driver Type D is Selected
3	0h RW	**HOSTCTRL2_1P8VSIGNALLINGENA:** 1.8V Signaling Enable This bit controls voltage regulator for I/O cell. 3.3V is supplied to the card regardless of signaling voltage. Setting this bit from 0 to 1 starts changing signal voltage from 3.3V to 1.8V. 1.8V regulator output shall be stable within 5ms. Host Controller clears this bit if switching to 1.8V signaling fails. Clearing this bit from 1 to 0 starts changing signal voltage from 1.8V to 3.3V. 3.3V regulator output shall be stable within 5ms. Host Driver can set this bit to 1 when Host Controller supports 1.8V signaling (One of support bits is set to 1: SDR50, SDR104 or DDR50 in the Capabilities register) and the card or device supports UHS-I 1 - 1.8V Signaling 0 - 3.3V Signaling
2:0	0h RW	**HOSTCTRL2_UHSMODESELECT:** UHS Mode Select This field is used to select one of UHS-I modes and effective when 1.8V Signaling Enable is set to 1. If Preset Value Enable in the Host Control 2 register is set to 1, Host Controller sets SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select according to Preset Value registers. In this case, one of preset value registers is selected by this field. Host Driver needs to reset SD Clock Enable before changing this field to avoid generating clock glitch. After setting this field, Host Driver sets SD Clock Enable again. 000b - SDR12 001b - SDR25 010b - SDR50 011b - SDR104 100b - DDR50 101b - HS400 110b - 111 Reserved When SDR50, SDR104 or DDR50 is selected for SDIO card, interrupt detection at the block gap shall not be used. Read Wait timing is changed for these modes. Refer to the SDIO Specification Version 3.00 for more detail

12.2.31 CAPABILITIES Reg (CAPABILITIES) - Offset 40h

CAPREG_HS400_SUPPORT

Type	Size	Offset	Default
MMIO	64 bit	BAR + 40h	80000007546EC881h

Bit Range	Default & Access	Field Name (ID): Description
63	1h RO	**CAPREG_HS400_SUPPORT:** CAPREG_HS400_SUPPORT
62:58	0h RO	**Reserved**
57	0h RO	**CAPREG_SPIBLK_MODE:** CAPREG_SPIBLK_MODE
56	0h RO	**CAPREG_SPISUPPORT:** CAPREG_SPISUPPORT
55:48	00h RO	**CAPREG_CLK_MULT:** CAPREG_CLK_MULT
47:46	0h RO	**CAPREG_RETUNINGMODES:** CAPREG_RETUNINGMODES
45	0h RO	**CAPREG_USE_TNG4_SDR50:** CAPREG_USE_TNG4_SDR50
44	0h RO	**Reserved**
43:40	0h RO	**CAPREG_TIMER_CNT4_RETUNG:** CAPREG_TIMER_CNT4_RETUNG
39	0h RO	**CAPREG_DRVTYPE4_SUPPORT:** CAPREG_DRVTYPE4_SUPPORT
38	0h RO	**CAPREG_DRVTYPED_SUPPORT:** CAPREG_DRVTYPED_SUPPORT
37	0h RO	**CAPREG_DRVTYPEC_SUPPORT:** CAPREG_DRVTYPEC_SUPPORT
36	0h RO	**CAPREG_DRVTYPEA_SUPPORT:** CAPREG_DRVTYPEA_SUPPORT
35	0h RO	**Reserved**
34	1h RO	**CORECFG_DDR50SUPPORT:** CORECFG_DDR50SUPPORT
33	1h RO	**CORECFG_SDR104SUPPORT:** CORECFG_SDR104SUPPORT
32	1h RO	**CORECFG_SDR50SUPPORT:** CORECFG_SDR50SUPPORT
31:30	1h RO	**CORECFG_SLOTTYPE:** CORECFG_SLOTTYPE
29	0h RO	**CORECFG_ASYNCHINTRSUPPORT:** CORECFG_ASYNCHINTRSUPPORT
28	1h RO	**CORECFG_64BITSUPPORTV3:** CORECFG_64BITSUPPORTV3
27	0h RO	**Reserved**
26	1h RO	**CORECFG_1P8VOLTSUPPORT:** CORECFG_1P8VOLTSUPPORT
25	0h RO	**CORECFG_3P0VOLTSUPPORT:** CORECFG_3P0VOLTSUPPORT

Bit Range	Default & Access	Field Name (ID): Description
24	0h RO	**CORECFG_3P3VOLTSUPPORT:** CORECFG_3P3VOLTSUPPORT
23	0h RO	**CORECFG_SUSPRESUME:** CORECFG_SUSPRESUME
22	1h RO	**CORECFG_SDMASUPPORT:** CORECFG_SDMASUPPORT
21	1h RO	**CORECFG_HIGHSPEEDSUPPORT:** CORECFG_HIGHSPEEDSUPPORT
20	0h RO	**Reserved**
19	1h RO	**CORECFG_ADMA2SUPPORT:** CORECFG_ADMA2SUPPORT
18	1h RO	**CORECFG_EXTDMEDIABUS:** CORECFG_EXTDMEDIABUS
17:16	2h RO	**CORECFG_MAXBLKLENGTH:** CORECFG_MAXBLKLENGTH
15:8	C8h RO	**CORECFG_BASECLKFREQ:** CORECFG_BASECLKFREQ
7	1h RO	**CORECFG_TIMEOUTCLKUNIT:** CORECFG_TIMEOUTCLKUNIT
6	0h RO	**Reserved**
5:0	01h RO	**CORECFG_TIMEOUTCLKFREQ:** CORECFG_TIMEOUTCLKFREQ

12.2.32 MAXCURRENTCAP Reg (MAXCURRENTCAP) - Offset 48h

Type	Size	Offset	Default
MMIO	64 bit	BAR + 48h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:24	0h RO	**Reserved**
23:16	00h WO	**CORECFG_MAXCURRENT1P8V:** CORECFG_MAXCURRENT1P8V
15:8	00h WO	**CORECFG_MAXCURRENT3P0V:** CORECFG_MAXCURRENT3P0V
7:0	00h WO	**CORECFG_MAXCURRENT3P3V:** CORECFG_MAXCURRENT3P3V

12.2.33 FORCEVENTFORAUTOCMDERRORSTATUS Reg (FORCEVENTFORAUTOCMDERRORSTATUS) - Offset 50h

Type	Size	Offset	Default
MMIO	16 bit	BAR + 50h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7	0h WO	**FORCECMDNOTISSUEDBYAUTOCMD12ERR:** FORCECMDNOTISSUEDBYAUTOCMD12ERR
6:5	0h RO	**Reserved**
4	0h WO	**FORCEAUTOCMDINDEXERR:** FORCEAUTOCMDINDEXERR
3	0h WO	**FORCEAUTOCMDENDBITERR:** FORCEAUTOCMDENDBITERR
2	0h WO	**FORCEAUTOCMDCRCERR:** FORCEAUTOCMDCRCERR
1	0h WO	**FORCEAUTOCMDTIMEOUTERR:** FORCEAUTOCMDTIMEOUTERR
0	0h WO	**FORCEAUTOCMDNOTEXEC:** FORCEAUTOCMDNOTEXEC

12.2.34 FORCEEVENTFORERRINTSTS Reg (FORCEEVENTFORERRINTSTS) - Offset 52h

Type	Size	Offset	Default
MMIO	16 bit	BAR + 52h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved**
10	0h RO	**FORCETUNINGERR:** FORCETUNINGERR
9	0h WO	**FORCEADMAERR:** FORCEADMAERR
8	0h WO	**FORCEAUTOCMDERR:** FORCEAUTOCMDERR

Bit Range	Default & Access	Field Name (ID): Description
7	0h WO	**FORCECURRLIMERR:** FORCECURRLIMERR
6	0h WO	**FORCEDATENDBITERR:** FORCEDATENDBITERR
5	0h WO	**FORCEDATCRCERR:** FORCEDATCRCERR
4	0h WO	**FORCEDATTIMEOUTERR:** FORCEDATTIMEOUTERR
3	0h WO	**FORCECMDINDEXERR:** FORCECMDINDEXERR
2	0h WO	**FORCECMDENDBITERR:** FORCECMDENDBITERR
1	0h WO	**FORCECMDCRCERR:** FORCECMDCRCERR
0	0h WO	**FORCECMDTIMEOUTERR:** FORCECMDTIMEOUTERR

12.2.35 ADMAERRSTS Reg (ADMAERRSTS) - Offset 54h

Type	Size	Offset	Default
MMIO	8 bit	BAR + 54h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved**
2	0h RO	**ADMAERRSTS_ADMALENMISMATCHERR:** ADMAERRSTS_ADMALENMISMATCHERR
1:0	0h RO	**ADMAERRSTS_ADMAERRORSTATE:** ADMAERRSTS_ADMAERRORSTATE

12.2.36 ADMASYSADDR1 Reg (ADMASYSADDR1) - Offset 58h

ADMA_32BIT_SYSADDRESS

Type	Size	Offset	Default
MMIO	32 bit	BAR + 58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**ADMA_32BIT_SYSADDRESS:** ADMA_32BIT_SYSADDRESS

12.2.37 ADMASYSADDR2 Reg (ADMASYSADDR2) - Offset 5Ch

ADMA_64BIT_SYSADDRESS2

Type	Size	Offset	Default
MMIO	16 bit	BAR + 5Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**ADMA_64BIT_SYSADDRESS2:** ADMA_64BIT_SYSADDRESS2

12.2.38 PRESETVALUE0 Reg (PRESETVALUE0) - Offset 60h

DRIVERSTRENGTHSELECTVALUE

Type	Size	Offset	Default
MMIO	16 bit	BAR + 60h	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**DRIVERSTRENGTHSELECTVALUE:** DRIVERSTRENGTHSELECTVALUE
13:11	0h RO	**Reserved**
10	0h RO	**CLOCKGENERATORSELECTVALUE:** CLOCKGENERATORSELECTVALUE
9:0	004h RO	**SDCLKFREQUENCYSELECTVALUE:** SDCLKFREQUENCYSELECTVALUE

12.2.39 PRESETVALUE1 Reg (PRESETVALUE1) - Offset 62h

DRIVERSTRENGTHSELECTVALUE

Type	Size	Offset	Default
MMIO	16 bit	BAR + 62h	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**DRIVERSTRENGTHSELECTVALUE:** DRIVERSTRENGTHSELECTVALUE

Bit Range	Default & Access	Field Name (ID): Description
13:11	0h RO	**Reserved**
10	0h RO	**CLOCKGENERATORSELECTVALUE:** CLOCKGENERATORSELECTVALUE
9:0	004h RO	**SDCLKFREQUENCYSELECTVALUE:** SDCLKFREQUENCYSELECTVALUE

12.2.40 PRESETVALUE2 Reg (PRESETVALUE2) - Offset 64h

DRIVERSTRENGTHSELECTVALUE

Type	Size	Offset	Default
MMIO	16 bit	BAR + 64h	0002h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**DRIVERSTRENGTHSELECTVALUE:** DRIVERSTRENGTHSELECTVALUE
13:11	0h RO	**Reserved**
10	0h RO	**CLOCKGENERATORSELECTVALUE:** CLOCKGENERATORSELECTVALUE
9:0	002h RO	**SDCLKFREQUENCYSELECTVALUE:** SDCLKFREQUENCYSELECTVALUE

12.2.41 PRESETVALUE3 Reg (PRESETVALUE3) - Offset 66h

DRIVERSTRENGTHSELECTVALUE

Type	Size	Offset	Default
MMIO	16 bit	BAR + 66h	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**DRIVERSTRENGTHSELECTVALUE:** DRIVERSTRENGTHSELECTVALUE
13:11	0h RO	**Reserved**
10	0h RO	**CLOCKGENERATORSELECTVALUE:** CLOCKGENERATORSELECTVALUE
9:0	004h RO	**SDCLKFREQUENCYSELECTVALUE:** SDCLKFREQUENCYSELECTVALUE

12.2.42 PRESETVALUE4 Reg (PRESETVALUE4) - Offset 68h

DRIVERSTRENGTHSELECTVALUE

Type	Size	Offset	Default
MMIO	16 bit	BAR + 68h	0002h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**DRIVERSTRENGTHSELECTVALUE:** DRIVERSTRENGTHSELECTVALUE
13:11	0h RO	**Reserved**
10	0h RO	**CLOCKGENERATORSELECTVALUE:** CLOCKGENERATORSELECTVALUE
9:0	002h RO	**SDCLKFREQUENCYSELECTVALUE:** SDCLKFREQUENCYSELECTVALUE

12.2.43 PRESETVALUE5 Reg (PRESETVALUE5) - Offset 6Ah

DRIVERSTRENGTHSELECTVALUE

Type	Size	Offset	Default
MMIO	16 bit	BAR + 6Ah	0001h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**DRIVERSTRENGTHSELECTVALUE:** DRIVERSTRENGTHSELECTVALUE
13:11	0h RO	**Reserved**
10	0h RO	**CLOCKGENERATORSELECTVALUE:** CLOCKGENERATORSELECTVALUE
9:0	001h RO	**SDCLKFREQUENCYSELECTVALUE:** SDCLKFREQUENCYSELECTVALUE

12.2.44 PRESETVALUE6 Reg (PRESETVALUE6) - Offset 6Ch

DRIVERSTRENGTHSELECTVALUE

Type	Size	Offset	Default
MMIO	16 bit	BAR + 6Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**DRIVERSTRENGTHSELECTVALUE:** DRIVERSTRENGTHSELECTVALUE
13:11	0h RO	**Reserved**
10	0h RO	**CLOCKGENERATORSELECTVALUE:** CLOCKGENERATORSELECTVALUE
9:0	000h RO	**SDCLKFREQUENCYSELECTVALUE:** SDCLKFREQUENCYSELECTVALUE

12.2.45 PRESETVALUE7 Reg (PRESETVALUE7) - Offset 6Eh

DRIVERSTRENGTHSELECTVALUE

Type	Size	Offset	Default
MMIO	16 bit	BAR + 6Eh	0002h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**DRIVERSTRENGTHSELECTVALUE:** DRIVERSTRENGTHSELECTVALUE
13:11	0h RO	**Reserved**
10	0h RO	**CLOCKGENERATORSELECTVALUE:** CLOCKGENERATORSELECTVALUE
9:0	002h RO	**SDCLKFREQUENCYSELECTVALUE:** SDCLKFREQUENCYSELECTVALUE

12.2.46 BOOTTIMEOUTCNT Reg (BOOTTIMEOUTCNT) - Offset 70h

BOOT_TIMEOUTCNT

Type	Size	Offset	Default
MMIO	32 bit	BAR + 70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**BOOT_TIMEOUTCNT:** BOOT_TIMEOUTCNT

12.2.47 SLOTINTRSTS Reg (SLOTINTRSTS) - Offset FCh

Type	Size	Offset	Default
MMIO	16 bit	BAR + FCh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:1	0h RO	**Reserved**
0	0h RO/V	**SDHCHOSTIF_SLOTINTRSTSSLOT0:** SDHCHOSTIF_SLOTINTRSTSSLOT0

13 Secure Digital I/O (SDIO) Controller

13.1 SDIO Configuration Registers Summary

This chapter records the registers in Bus: 0, Device 26, Function 1...

Table 13-1. Summary of Bus: 0, Device: 26, Function: 1 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	REG DEVVENDID (DEVVENDID)	4B488086h
4h	4	REG STATUSCOMMAND (STATUSCOMMAND)	00100000h
8h	4	REG REVCLASSCODE (REVCLASSCODE)	08050100h
Ch	4	REG CLLATHEADERBIST (CLLATHEADERBIST)	00800000h
10h	4	REG BAR (BAR)	00000004h
14h	4	REG BAR_HIGH (BAR_HIGH)	00000000h
18h	4	REG BAR1 (BAR1)	00000004h
1Ch	4	REG BAR1_HIGH (BAR1_HIGH)	00000000h
2Ch	4	REG SUBSYSTEMID (SUBSYSTEMID)	00000000h
30h	4	REG EXPANSION_ROM_BASEADDR (EXPANSION_ROM_BASEADDR)	00000000h
34h	4	REG CAPABILITYPTR (CAPABILITYPTR)	00000080h
3Ch	4	REG INTERRUPTREG (INTERRUPTREG)	00000000h
80h	4	REG POWERCAPID (POWERCAPID)	00039001h
84h	4	REG PMECTRLSTATUS (PMECTRLSTATUS)	00000008h
90h	4	REG PCIDEVIDLE_CAP_RECORD (PCIDEVIDLE_CAP_RECORD)	F0140009h
94h	4	REG DEVID_VEND_SPECIFIC_REG (DEVID_VEND_SPECIFIC_REG)	01400010h
98h	4	REG D0I3_CONTROL_SW_LTR_MMIO_REG (D0I3_CONTROL_SW_LTR_MMIO_REG)	00008041h
9Ch	4	REG DEVICE_IDLE_POINTER_REG (DEVICE_IDLE_POINTER_REG)	000081C1h
A0h	4	REG D0I3_MAX_POW_LAT_PG_CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG)	00290800h
B0h	4	REG GEN_REGRW1 (GEN_REGRW1)	00000000h
B4h	4	REG GEN_REGRW2 (GEN_REGRW2)	00000000h
B8h	4	REG GEN_REGRW3 (GEN_REGRW3)	00000000h
BCh	4	REG GEN_REGRW4 (GEN_REGRW4)	00000000h
C0h	4	REG GEN_INPUT_REG (GEN_INPUT_REG)	00000000h
F8h	4	REG MANID (MANID)	0000000Fh

13.1.1 REG DEVVENDID (DEVVENDID) - Offset 0h

Vendor ID Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + 0h	4B488086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4B48h RO	**DEVICEID:** DEVICEID
15:0	8086h RO	**VENDORID:** VENDORID

13.1.2 REG STATUSCOMMAND (STATUSCOMMAND) - Offset 4h

PCI Command Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW/1C	**RMA:** RMA
28	0h RW/1C	**RTA:** RTA
27:21	0h RO	**Reserved**
20	1h RO	**CAPLIST:** CAPLIST
19	0h RO	**INTR_STATUS:** INTR_STATUS
18:11	0h RO	**Reserved**
10	0h RW	**INTR_DISABLE:** INTR_DISABLE
9	0h RO	**Reserved**
8	0h RW	**SERR_ENABLE:** SERR_ENABLE
7:3	0h RO	**Reserved**
2	0h RW	**BME:** BME
1	0h RW	**MSE:** MSE
0	0h RO	**Reserved**

13.1.3 REG REVCLASSCODE (REVCLASSCODE) - Offset 8h

Revision ID Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + 8h	08050100h

Bit Range	Default & Access	Field Name (ID): Description
31:8	080501h RO	**CLASS_CODES:** CLASS_CODES
7:0	00h RO	**RID:** RID

13.1.4 REG CLLATHEADERBIST (CLLATHEADERBIST) - Offset Ch

Cache Line Latency Header and BIST Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + Ch	00800000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	1h RO	**MULFNDEV:** MULFNDEV
22:16	00h RO	**HEADERTYPE:** HEADERTYPE
15:8	00h RO	**LATTIMER:** LATTIMER
7:0	00h RW	**CACHELINE_SIZE:** CACHELINE_SIZE

13.1.5 REG BAR (BAR) - Offset 10h

BAR - Base Address Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + 10h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**BASEADDR:** BASEADDR
11:4	00h RO	**SIZEINDICATOR:** SIZEINDICATOR
3	0h RO	**PREFETCHABLE:** PREFETCHABLE
2:1	2h RO	**TYPE:** TYPE
0	0h RO	**MESSAGE_SPACE:** MESSAGE_SPACE

13.1.6 REG BAR_HIGH (BAR_HIGH) - Offset 14h

BAR - Base Address Register High

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**BASEADDR_HIGH:** BASEADDR_HIGH

13.1.7 REG BAR1 (BAR1) - Offset 18h

BAR1 - Base Address Register1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + 18h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**BASEADDR1:** BASEADDR1
11:4	00h RO	**SIZEINDICATOR1:** SIZEINDICATOR1
3	0h RO	**PREFETCHABLE1:** PREFETCHABLE1
2:1	2h RO	**TYPE1:** TYPE1
0	0h RO	**MESSAGE_SPACE1:** MESSAGE_SPACE1

13.1.8 REG BAR1_HIGH (BAR1_HIGH) - Offset 1Ch

BAR1 - Base Address Register1 High

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**BASEADDR1_HIGH:** BASEADDR1_HIGH

13.1.9 REG SUBSYSTEMID (SUBSYSTEMID) - Offset 2Ch

SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**SUBSYSTEMID:** SUBSYSTEMID
15:0	0000h RW/O	**SUBSYSTEMVENDORID:** SUBSYSTEMVENDORID

13.1.10 REG EXPANSION_ROM_BASEADDR (EXPANSION_ROM_BASEADDR) - Offset 30h

Expansion ROM Base Address Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** EXPANSION_ROM_BASE

13.1.11 REG CAPABILITYPTR (CAPABILITYPTR) - Offset 34h

Capabilities Pointer Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**CAPPTR_POWER:** CAPPTR_POWER

13.1.12 REG INTERRUPTREG (INTERRUPTREG) - Offset 3Ch

Interrupt Line Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + 3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**MAX_LAT:** MAX_LAT
23:16	00h RO	**MIN_GNT:** MIN_GNT
15:12	0h RO	**Reserved**
11:8	0h RO	**INTPIN:** INTPIN
7:0	00h RW	**INTLINE:** INTLINE

13.1.13 REG POWERCAPID (POWERCAPID) - Offset 80h

Power Management Capability ID Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + 80h	00039001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PMESUPPORT:** PMESUPPORT
26:19	0h RO	**Reserved**
18:16	3h RO	**VERSION:** VERSION
15:8	90h RO	**NXTCAP:** NXTCAP
7:0	01h RO	**POWER_CAP:** POWER_CAP

13.1.14 REG PMECTRLSTATUS (PMECTRLSTATUS) - Offset 84h

Power Management Control and Status Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C	**PMESTATUS:** PMESTATUS
14:9	0h RO	**Reserved**
8	0h RW	**PMEENABLE:** PMEENABLE
7:4	0h RO	**Reserved**
3	1h RO	**NO_SOFT_RESET:** NO_SOFT_RESET
2	0h RO	**Reserved**
1:0	0h RW	**POWERSTATE:** POWERSTATE

13.1.15 REG PCIDEVIDLE_CAP_RECORD (PCIDEVIDLE_CAP_RECORD) - Offset 90h

PCI Device Idle Capability Record Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + 90h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP:** VEND_CAP
27:24	0h RO	**REVID:** REVID
23:16	14h RO	**CAP_LENGTH:** CAP_LENGTH
15:8	00h RO	**NEXT_CAP:** NEXT_CAP
7:0	09h RO	**CAPID:** CAPID

13.1.16 REG DEVID_VEND_SPECIFIC_REG (DEVID_VEND_SPECIFIC_REG) - Offset 94h

Device ID Vendor Specific Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**VSEC_LENGTH:** VSEC_LENGTH
19:16	0h RO	**VSEC_REV:** VSEC_REV
15:0	0010h RO	**VSECID:** VSECID

13.1.17 REG D0I3_CONTROL_SW_LTR_MMIO_REG (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h

SW LTR Update MMIO Location Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + 98h	00008041h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000804h RO	**SW_LAT_DWORD_OFFSET:** SW_LAT_DWORD_OFFSET
3:1	0h RO	**SW_LAT_BAR_NUM:** SW_LAT_BAR_NUM
0	1h RO	**SW_LAT_VALID:** SW_LAT_VALID

13.1.18 REG DEVICE_IDLE_POINTER_REG (DEVICE_IDLE_POINTER_REG) - Offset 9Ch

Device IDLE Pointer Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + 9Ch	000081C1h

Bit Range	Default & Access	Field Name (ID): Description
31:4	000081Ch RO	**DWORD_OFFSET:** DWORD_OFFSET
3:1	0h RO	**BAR_NUM:** BAR_NUM
0	1h RO	**VALID:** VALID

13.1.19 REG D0I3_MAX_POW_LAT_PG_CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h

Doi3 Max Power On Latency

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + A0h	00290800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	1h RW	**HAE:** HAE
20	0h RO	**Reserved**
19	1h RW	**SLEEP_EN:** SLEEP_EN

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**PGE:** PGE
17	0h RW	**I3_ENABLE:** I3_ENABLE
16	1h RW	**PMCRE:** PMCRE
15:13	0h RO	**Reserved**
12:10	2h RW/O	**POW_LAT_SCALE:** POW_LAT_SCALE
9:0	000h RW/O	**POW_LAT_VALUE:** POW_LAT_VALUE

13.1.20 REG GEN_REGRW1 (GEN_REGRW1) - Offset B0h

General Purpose PCI RW Register1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW1:** GEN_REG_RW1

13.1.21 REG GEN_REGRW2 (GEN_REGRW2) - Offset B4h

General Purpose PCI RW Register2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW2:** GEN_REG_RW2

13.1.22 REG GEN_REGRW3 (GEN_REGRW3) - Offset B8h

General Purpose PCI RW Register3

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW3:** GEN_REG_RW3

13.1.23 REG GEN_REGRW4 (GEN_REGRW4) - Offset BCh

General Purpose PCI RW Register4

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW4:** GEN_REG_RW4

13.1.24 REG GEN_INPUT_REG (GEN_INPUT_REG) - Offset C0h

General Input Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**GEN_REG_INPUT_RW:** GEN_REG_INPUT_RW

13.1.25 REG MANID (MANID) - Offset F8h

Manufacturers ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:1] + F8h	0000000Fh

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000Fh RO	**MANID:** MANID

13.2 SDIO Memory Mapped Registers Summary

Table 13-2. Summary of SDIO Memory Mapped Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	REG SDMASYSADDR (SDMASYSADDR)	00000000h
4h	2	REG BLOCKSIZE (BLOCKSIZE)	0000h
6h	2	REG BLOCKCOUNT (BLOCKCOUNT)	0000h
8h	4	REG ARGUMENT1 (ARGUMENT1)	00000000h
Ch	2	REG TRANSFERMODE (TRANSFERMODE)	0000h
Eh	2	REG COMMAND (COMMAND)	0000h
10h	4	REG RESPONSE01 (RESPONSE01)	00000000h
14h	2	REG RESPONSE2 (RESPONSE2)	0000h
16h	2	REG RESPONSE3 (RESPONSE3)	0000h
18h	2	REG RESPONSE4 (RESPONSE4)	0000h
1Ah	2	REG RESPONSE5 (RESPONSE5)	0000h
1Ch	2	REG RESPONSE6 (RESPONSE6)	0000h
1Eh	2	REG RESPONSE7 (RESPONSE7)	0000h
20h	4	REG DATAPORT (DATAPORT)	00000000h
24h	4	REG PRESENTSTATE (PRESENTSTATE)	01F00000h
28h	1	REG HOSTCONTROL1 (HOSTCONTROL1)	00h
29h	1	REG POWERCONTROL (POWERCONTROL)	00h
2Ah	1	REG BLOCKGAPCONTROL (BLOCKGAPCONTROL)	00h
2Bh	1	REG WAKEUPCONTROL (WAKEUPCONTROL)	00h
2Ch	2	REG CLOCKCONTROL (CLOCKCONTROL)	0000h
2Eh	1	REG TIMEOUTCONTROL (TIMEOUTCONTROL)	00h
2Fh	1	REG SOFTWARERESET (SOFTWARERESET)	00h
30h	2	REG NORMALINTRSTS (NORMALINTRSTS)	0000h
32h	2	REG ERRORINTRSTS (ERRORINTRSTS)	0000h
34h	2	REG NORMALINTRSTSENA (NORMALINTRSTSENA)	0000h
36h	2	REG ERRORINTRSTSENA (ERRORINTRSTSENA)	0000h
38h	2	REG NORMALINTRSIGENA (NORMALINTRSIGENA)	0000h
3Ah	2	REG ERRORINTRSIGENA (ERRORINTRSIGENA)	0000h
3Ch	2	REG AUTOCMDERRSTS (AUTOCMDERRSTS)	0000h
3Eh	2	REG HOSTCONTROL2 (HOSTCONTROL2)	0000h
40h	8	REG CAPABILITIES (CAPABILITIES)	180000073 D68C881h
48h	8	REG MAXCURRENTCAP (MAXCURRENTCAP)	000000000 0000000h
50h	2	REG FORCEEVENTFORAUTOCMDERRORSTATUS (FORCEEVENTFORAUTOCMDERRORSTATUS)	0000h
52h	2	REG FORCEEVENTFORERRINTSTS (FORCEEVENTFORERRINTSTS)	0000h
54h	1	REG ADMAERRSTS (ADMAERRSTS)	00h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
58h	4	REG ADMASYSADDR01 (ADMASYSADDR01)	00000000h
5Ch	2	REG ADMASYSADDR2 (ADMASYSADDR2)	0000h
5Eh	2	REG ADMASYSADDR3 (ADMASYSADDR3)	0000h
60h	2	REG PRESETVALUE0 (PRESETVALUE0)	0004h
62h	2	REG PRESETVALUE1 (PRESETVALUE1)	0004h
64h	2	REG PRESETVALUE2 (PRESETVALUE2)	0002h
66h	2	REG PRESETVALUE3 (PRESETVALUE3)	0004h
68h	2	REG PRESETVALUE4 (PRESETVALUE4)	0002h
6Ah	2	REG PRESETVALUE5 (PRESETVALUE5)	0001h
6Ch	2	REG PRESETVALUE6 (PRESETVALUE6)	0000h
6Eh	2	REG PRESETVALUE7 (PRESETVALUE7)	0002h
70h	4	REG BOOTTIMEOUTCNT (BOOTTIMEOUTCNT)	00000000h
74h	2	REG PRESETVALUE8 (PRESETVALUE8)	0000h
78h	4	REG ADMA3_LOW (ADMA3_LOW)	00000000h
FCh	2	REG SLOTINTRSTS (SLOTINTRSTS)	0000h
FEh	2	REG HOSTCONTROLLERVER (HOSTCONTROLLERVER)	1002h

13.2.1 REG SDMASYSADDR (SDMASYSADDR) - Offset 0h

32-bit Block Count (SDMA System Address) Register (High)

Type	Size	Offset	Default
MMIO	32 bit	BAR + 0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SDMA_SYSADDRESS:** sdma_sysaddress

13.2.2 REG BLOCKSIZE (BLOCKSIZE) - Offset 4h

BlockSize

Type	Size	Offset	Default
MMIO	16 bit	BAR + 4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14:12	0h RW	**SDMA_BUFBOUNDARY:** sdma_bufboundary
11:0	000h RW	**XFER_BLOCKSIZE:** xfer_blocksize

13.2.3 REG BLOCKCOUNT (BLOCKCOUNT) - Offset 6h

BlockCount

Type	Size	Offset	Default
MMIO	16 bit	BAR + 6h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**BLOCK_CNT_16BIT:** block_cnt_16bit

13.2.4 REG ARGUMENT1 (ARGUMENT1) - Offset 8h

Argument1

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**COMMAND_ARGUMENT1:** command_argument1

13.2.5 REG TRANSFERMODE (TRANSFERMODE) - Offset Ch

TransferMode

Type	Size	Offset	Default
MMIO	16 bit	BAR + Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	**Reserved**
8	0h RW	**XFERMODE_RESP_INTR_DISABLE:** xfermode_resp_intr_disable
7	0h RW	**XFER_RESP_ERR_CHK_ENB:** xfer_resp_err_chk_enb
6	0h RW	**XFER_RESP_TYPE_R1_R5:** xfer_resp_type_r1_r5
5	0h RW	**XFERMODE_MULTIBLKSEL:** xfermode_multiblksel
4	0h RW	**XFERMODE_DATAXFERDIR:** xfermode_dataxferdir
3:2	0h RW	**XFERMODE_AUTOCMDENA:** xfermode_autocmdena
1	0h RW	**XFERMODE_BLKCNTENA:** xfermode_blkcntena
0	0h RW	**XFERMODE_DMAENABLE:** xfermode_dmaenable

13.2.6 REG COMMAND (COMMAND) - Offset Eh

Command

Type	Size	Offset	Default
MMIO	16 bit	BAR + Eh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Reserved**
13:8	00h RW	**COMMAND_CMDINDEX:** command_cmdindex
7:6	0h RW	**COMMAND_CMDTYPE:** command_cmdtype
5	0h RW	**COMMAND_DATAPRESENT:** command_datapresent
4	0h RW	**COMMAND_INDEXCHKENA:** command_indexchkena
3	0h RW	**COMMAND_CRCCHKENA:** command_crcchkena
2	0h RW	**COMMAND_SUB_FLAG:** command_sub_flag
1:0	0h RW	**COMMAND_RESPONSETYPE:** command_responsetype

13.2.7 REG RESPONSE01 (RESPONSE01) - Offset 10h

Response Register 1

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**COMMAND_RESPONSE_31_0:** command_response_31_0

13.2.8 REG RESPONSE2 (RESPONSE2) - Offset 14h

Response Register 2

Type	Size	Offset	Default
MMIO	16 bit	BAR + 14h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**COMMAND_RESPONSE_47_32:** command_response_47_32

13.2.9 REG RESPONSE3 (RESPONSE3) - Offset 16h

Response Register 3

Type	Size	Offset	Default
MMIO	16 bit	BAR + 16h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**COMMAND_RESPONSE_63_48:** command_response_63_48

13.2.10 REG RESPONSE4 (RESPONSE4) - Offset 18h

Response Register 4

Type	Size	Offset	Default
MMIO	16 bit	BAR + 18h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**COMMAND_RESPONSE_79_64:** command_response_79_64

13.2.11 REG RESPONSE5 (RESPONSE5) - Offset 1Ah

Response Register 5

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1Ah	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**COMMAND_RESPONSE_95_80:** command_response_95_80

13.2.12 REG RESPONSE6 (RESPONSE6) - Offset 1Ch

Response Register 6

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**COMMAND_RESPONSE_111_96:** command_response_111_96

13.2.13 REG RESPONSE7 (RESPONSE7) - Offset 1Eh

Response Register 7

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1Eh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**COMMAND_RESPONSE_127_112:** command_response_127_112

13.2.14 REG DATAPORT (DATAPORT) - Offset 20h

Buffer DataPort

Type	Size	Offset	Default
MMIO	32 bit	BAR + 20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SDHCDMACTRL_PIOBUFRDDATA:** sdhcdmactrl_piobufrddata

13.2.15 REG PRESENTSTATE (PRESENTSTATE) - Offset 24h

PresentState

Type	Size	Offset	Default
MMIO	32 bit	BAR + 24h	01F00000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**UHS2_INTF_DETECT:** uhs2_intf_detect
30	0h RO/V	**UHS2_LANE_SYNCH:** uhs2_lane_synch
29	0h RO/V	**UHS2_INDORMANTSTE:** uhs2_indormantste
28	0h RO/V	**SUB_CMND_STS:** sub_cmnd_sts
27	0h RO/V	**CMND_NOTISSUE_BYERR:** cmnd_notissue_byerr
26	0h RO	**Reserved**
25	0h RO/V	**HOST_REGU_VOL_STB:** host_regu_vol_stb
24	1h RO/V	**SDIF_CMDIN_DSYNC:** sdif_cmdin_dsync
23:20	Fh RO/V	**SDIF_DAT0IN_DSYNC:** sdif_dat0in_dsync
19	0h RO/V	**SDIF_WP_DSYNC:** sdif_wp_dsync
18	0h RO/V	**SDIF_CD_N_DSYNC:** sdif_cd_n_dsync
17	0h RO/V	**SDHCCARDDET_STATESTABLE_DSYNC:** sdhccarddet_statestable_dsync
16	0h RO/V	**SDHCCARDDET_INSERTED_DSYNC:** sdhccarddet_inserted_dsync
15:12	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO/V	**SDHCDMACTRL_PIOBUFRDENA:** sdhcdmactrl_piobufrdena
10	0h RO/V	**SDHCDMACTRL_PIOBUFWRENA:** sdhcdmactrl_piobufwrena
9	0h RO/V	**SDHCDMACTRL_RDXFERACTIVE:** sdhcdmactrl_rdxferactive
8	0h RO/V	**SDHCDMACTRL_WRXFERACTIVE:** sdhcdmactrl_wrxferactive
7:4	0h RO/V	**DAT7_4_LINE_SIGLEVEL:** dat7_4_line_siglevel
3	0h RO/V	**SDHCSDCTRL_RETUNINGREQ_DSYNC:** sdhcsdctrl_retuningreq_dsync
2	0h RO/V	**SDHCDMACTRL_DATALINEACTIVE:** sdhcdmactrl_datalineactive
1	0h RO/V	**PRESENTSTATE_INHIBITDAT:** presentstate_inhibitdat
0	0h RO/V	**PRESENTSTATE_INHIBITCMD:** presentstate_inhibitcmd

13.2.16 REG HOSTCONTROL1 (HOSTCONTROL1) - Offset 28h

HostControl1

Type	Size	Offset	Default
MMIO	8 bit	BAR + 28h	00h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**HOSTCTRL1_CDSIGSELECT:** hostctrl1_cdsigselect
6	0h RW	**HOSTCTRL1_CDTESTLEVEL:** hostctrl1_cdtestlevel
5	0h RW	**HOSTCTRL1_EXTDATAWIDTH:** hostctrl1_extdatawidth
4:3	0h RW	**HOSTCTRL1_DMASELECT:** hostctrl1_dmaselect
2	0h RW	**HOSTCTRL1_HIGHSPEEDENA:** hostctrl1_highspeedena
1	0h RW	**HOSTCTRL1_DATAWIDTH:** hostctrl1_datawidth
0	0h RW	**HOSTCTRL1_LEDCONTROL:** hostctrl1_ledcontrol

13.2.17 REG POWERCONTROL (POWERCONTROL) - Offset 29h

PowerControl

Type	Size	Offset	Default
MMIO	8 bit	BAR + 29h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RW	**SDBUS_VOLTAGE_SEL_VDD2:** sdbus_voltage_sel_vdd2
4	0h RW	**SDBUS_POWER_VDD2:** sdbus_power_vdd2
3:1	0h RW	**SDBUS_VOLTAGE_SEL_VDD1:** sdbus_voltage_sel_vdd1
0	0h RW	**SDBUS_POWER_VDD1:** sdbus_power_vdd1

13.2.18 REG BLOCKGAPCONTROL (BLOCKGAPCONTROL) - Offset 2Ah

BlockGapControl

Type	Size	Offset	Default
MMIO	8 bit	BAR + 2Ah	00h

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**Reserved**
3	0h RW	**INTR_AT_BLOCK_GAP:** intr_at_block_gap
2	0h RW	**RD_WAIT_CTRL:** rd_wait_ctrl
1	0h RW	**CONTINUE_REQ:** continue_req
0	0h RW	**STOPATBLKGAP_REQ:** stopatblkgap_req

13.2.19 REG WAKEUPCONTROL (WAKEUPCONTROL) - Offset 2Bh

Wakeup Control

Type	Size	Offset	Default
MMIO	8 bit	BAR + 2Bh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved**
2	0h RW	**WKUPCTRL_CARDREMOVAL:** wkupctrl_cardremoval
1	0h RW	**WKUPCTRL_CARDINSERTION:** wkupctrl_cardinsertion
0	0h RW	**WKUPCTRL_CARDINTERRUPT:** wkupctrl_cardinterrupt

13.2.20 REG CLOCKCONTROL (CLOCKCONTROL) - Offset 2Ch

Clock Control

Type	Size	Offset	Default
MMIO	16 bit	BAR + 2Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RW	**CLKCTRL_SDCLKFREQSEL:** clkctrl_sdclkfreqsel
7:6	0h RW	**CLKCTRL_SDCLKFREQSEL_UPPERBITS:** clkctrl_sdclkfreqsel_upperbits
5	0h RW	**CLKCTRL_CLKGENSEL:** clkctrl_clkgensel
4	0h RO	**Reserved**
3	0h RW	**PLL_ENBLE:** pll_enble
2	0h RW	**CLKCTRL_SDCLKENA:** clkctrl_sdclkena
1	0h RO/V	**SDHCCLKGEN_INTCLKSTABLE_DSYNC:** sdhcclkgen_intclkstable_dsync
0	0h RW	**CLKCTRL_INTCLKENA:** clkctrl_intclkena

13.2.21 REG TIMEOUTCONTROL (TIMEOUTCONTROL) - Offset 2Eh

Timeout Control

Type	Size	Offset	Default
MMIO	8 bit	BAR + 2Eh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**Reserved**
3:0	0h RW	**DATA_TIMEOUT_CNTR_VAL:** data_timeout_cntr_val

13.2.22 REG SOFTWARERESET (SOFTWARERESET) - Offset 2Fh

Software Reset

Type	Size	Offset	Default
MMIO	8 bit	BAR + 2Fh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved**
2	0h RW	**SWRESET_FOR_DAT:** swreset_for_dat
1	0h RW	**SWRESET_FOR_CMD:** swreset_for_cmd
0	0h RW	**SWRESET_FOR_ALL:** swreset_for_all

13.2.23 REG NORMALINTRSTS (NORMALINTRSTS) - Offset 30h

Normal Interrupt Status

Type	Size	Offset	Default
MMIO	16 bit	BAR + 30h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**REG_ERRORINTRSTS:** reg_errorintrsts
14	0h RO	**Reserved**
13	0h RO	**FX_EVENT:** FX_event
12	0h RO	**NORMALINTRSTS_RETUNINGEVENT:** normalintrsts_retuningevent
11	0h RO	**NORMALINTRSTS_INTC:** normalintrsts_intc

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO	**NORMALINTRSTS_INTB:** normalintrsts_intb
9	0h RO	**NORMALINTRSTS_INTA:** normalintrsts_inta
8	0h RO	**NORMALINTRSTS_CARDINTSTS:** normalintrsts_cardintsts
7	0h RW/1C	**NORMALINTRSTS_CARDREMSTS:** normalintrsts_cardremsts
6	0h RW/1C	**NORMALINTRSTS_CARDINSSTS:** normalintrsts_cardinssts
5	0h RW/1C	**NORMALINTRSTS_BUFRDREADY:** normalintrsts_bufrdready
4	0h RW/1C	**NORMALINTRSTS_BUFWRREADY:** normalintrsts_bufwrready
3	0h RW/1C	**NORMALINTRSTS_DMAINTERRUPT:** normalintrsts_dmainterrupt
2	0h RW/1C	**NORMALINTRSTS_BLKGAPEVENT:** normalintrsts_blkgapevent
1	0h RW/1C	**NORMALINTRSTS_XFERCOMPLETE:** normalintrsts_xfercomplete
0	0h RW/1C	**NORMALINTRSTS_CMDCOMPLETE:** normalintrsts_cmdcomplete

13.2.24 REG ERRORINTRSTS (ERRORINTRSTS) - Offset 32h

Error Interrupt Status

Type	Size	Offset	Default
MMIO	16 bit	BAR + 32h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RW/1C	**VENDORSPECIFICERRORSTATUS:** VendorSpecificErrorStatus
12	0h RW/1C	**TARGET_RESPONSE_ERROR:** target_response_error
11	0h RW/1C	**RESPONSE_ERR_SD_MODE:** response_err_sd_mode
10	0h RW/1C	**TUNING_ERR_UHSI:** tuning_err_uhsI
9	0h RW/1C	**ADMA_ERROR:** adma_error
8	0h RW/1C	**AUTO_CMD_ERR_SD_MODE:** auto_cmd_err_sd_mode

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/1C	**CURRENT_LIMIT_ERR:** current_limit_err
6	0h RW/1C	**DATA_END_BIT_ERR:** data_end_bit_err
5	0h RW/1C	**DATA_CRC_ERR_SD_MODE:** data_crc_err_sd_mode
4	0h RW/1C	**DATA_TIMEOUT_ERR_SD_MODE:** data_timeout_err_sd_mode
3	0h RW/1C	**CMD_INDEX_ERR_SD_MODE:** cmd_index_err_sd_mode
2	0h RW/1C	**CMD_END_BIT_ERR_SD_MODE:** cmd_end_bit_err_sd_mode
1	0h RW/1C	**CMD_CRC_ERR_SD_MODE:** cmd_crc_err_sd_mode
0	0h RW/1C	**CMD_TIMEOUT_ERR_SD_MODE:** cmd_timeout_err_sd_mode

13.2.25 REG NORMALINTRSTSENA (NORMALINTRSTSENA) - Offset 34h

Normal Interrupt Status Enable

Type	Size	Offset	Default
MMIO	16 bit	BAR + 34h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**NORM_FIXED_TO_0:** norm_fixed_to_0
14	0h RO	**Reserved**
13	0h RW	**FX_EVENT_STS_ENB:** FX_event_sts_enb
12	0h RW	**RE_TUNING_EVNT_STS_ENB:** re_tuning_evnt_sts_enb
11	0h RW	**INT_C_STS_ENB:** int_c_sts_enb
10	0h RW	**INT_B_STS_ENB:** int_b_sts_enb
9	0h RW	**INT_A_STS_ENB:** int_a_sts_enb
8	0h RW	**SDHCREGSET_CARDINTSTSENA:** sdhcregset_cardintstsena
7	0h RW	**SDHCREGSET_CARDREMSTSENA:** sdhcregset_cardremstsena

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**SDHCREGSET_CARDINSSTSENA:** sdhcregset_cardinsstsena
5	0h RW	**BUFFER_RD_READY_STS_EN:** buffer_rd_ready_sts_en
4	0h RW	**BUFFER_WR_READY_STS_EN:** buffer_wr_ready_sts_en
3	0h RW	**DMA_INTR_STS_ENB:** dma_intr_sts_enb
2	0h RW	**BLOCK_GAP_EVENT_STS_ENB:** block_gap_event_sts_enb
1	0h RW	**TRANSFER_COMPLETE_STS_ENB:** transfer_complete_sts_enb
0	0h RW	**CMD_COMPLETE_STS_ENB:** cmd_complete_sts_enb

13.2.26 REG ERRORINTRSTSENA (ERRORINTRSTSENA) - Offset 36h

Error Interrupt Status Enable

Type	Size	Offset	Default
MMIO	16 bit	BAR + 36h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW	**VENDORSPECIFICERRORSTATUSENB:** VendorSpecificErrorStatusEnb
11	0h RW	**RESPONSE_ERR_STS_ENB:** response_err_sts_enb
10	0h RW	**TUNING_ERR_STS_ENB:** tuning_err_sts_enb
9	0h RW	**ADMA_ERR_STS_ENB:** adma_err_sts_enb
8	0h RW	**AUTO_CMD_ERR_STS_ENB:** auto_cmd_err_sts_enb
7	0h RW	**CURRENT_LIMIT_ERR_STS_ENB:** current_limit_err_sts_enb
6	0h RW	**DATA_END_BIT_ERR_STS_ENB:** data_end_bit_err_sts_enb
5	0h RW	**DATA_CRC_ERR_SD_MODE:** data_crc_err_sd_mode
4	0h RW	**DATA_TIMEOUT_ERR_SD_MODE:** data_timeout_err_sd_mode
3	0h RW	**CMD_INDEX_ERR_SD_MODE:** cmd_index_err_sd_mode

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**CMD_END_BIT_ERR_SD_MODE:** cmd_end_bit_err_sd_mode
1	0h RW	**CMD_CRC_ERR_SD_MODE:** cmd_crc_err_sd_mode
0	0h RW	**CMD_TIMEOUT_ERR_SD_MODE:** cmd_timeout_err_sd_mode

13.2.27 REG NORMALINTRSIGENA (NORMALINTRSIGENA) - Offset 38h

Normal Interrupt Signal Enable

Type	Size	Offset	Default
MMIO	16 bit	BAR + 38h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**FIXED_TO_0:** fixed_to_0
14	0h RO	**Reserved**
13	0h RW	**FX_EVENT_SIGENB:** FX_event_sigenb
12	0h RW	**RETUNG_EVNT_INTRSIG_ENB:** retung_evnt_intrsig_enb
11	0h RW	**INT_C_SIG_ENB:** int_c_sig_enb
10	0h RW	**INT_B_SIG_ENB:** int_b_sig_enb
9	0h RW	**INT_A_SIG_ENB:** int_a_sig_enb
8	0h RW	**CARD_INTR_SIG_ENB:** card_intr_sig_enb
7	0h RW	**CARD_REMOVE_SIG_ENB:** card_remove_sig_enb
6	0h RW	**CARD_INSERT_SIG_ENB:** card_insert_sig_enb
5	0h RW	**BUFFER_RD_READY_SIG_ENB:** buffer_rd_ready_sig_enb
4	0h RW	**BUFFER_WR_READY_SIG_ENB:** buffer_wr_ready_sig_enb
3	0h RW	**DMA_INTR_SIG_ENB:** dma_intr_sig_enb

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**BLOCK_GAP_EVENT_SIG_ENB:** block_gap_event_sig_enb
1	0h RW	**TRANSFER_COMPLETE_SIG_ENB:** transfer_complete_sig_enb
0	0h RW	**CMD_COMPLETE_SIG_ENB:** cmd_complete_sig_enb

13.2.28 REG ERRORINTRSIGENA (ERRORINTRSIGENA) - Offset 3Ah

Error Interrupt Signal Enable

Type	Size	Offset	Default
MMIO	16 bit	BAR + 3Ah	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW	**VENDORSPECIFICERRORSIGENB:** VendorSpecificErrorSigEnb
11	0h RW	**RESPONSE_ERR_SIG_ENB:** response_err_sig_enb
10	0h RW	**TUNING_ERR_SIG_ENB:** tuning_err_sig_enb
9	0h RW	**ADMA_ERR_SIG_ENB:** adma_err_sig_enb
8	0h RW	**AUTO_CMD_ERR_SIG_ENB:** auto_cmd_err_sig_enb
7	0h RW	**CURRENT_LIMIT_ERR_SIG_ENB:** current_limit_err_sig_enb
6	0h RW	**DATA_END_BIT_ERR_SIG_ENB:** data_end_bit_err_sig_enb
5	0h RW	**DATA_CRC_ERR_SIG_SD_MODE:** data_crc_err_sig_sd_mode
4	0h RW	**DATA_TIMEOUT_ERR_SIG_SD_MODE:** data_timeout_err_sig_sd_mode
3	0h RW	**CMD_INDEX_ERR_SIG_SD_MODE:** cmd_index_err_sig_sd_mode
2	0h RW	**CMD_END_BIT_ERR_SIG_SD_MODE:** cmd_end_bit_err_sig_sd_mode
1	0h RW	**CMD_CRC_ERR_SIG_SD_MODE:** cmd_crc_err_sig_sd_mode
0	0h RW	**CMD_TIMEOUT_ERR_SIG_SD_MODE:** cmd_timeout_err_sig_sd_mode

13.2.29 REG AUTOCMDERRSTS (AUTOCMDERRSTS) - Offset 3Ch

Auto CMD12 Error Status

Type	Size	Offset	Default
MMIO	16 bit	BAR + 3Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7	0h RO	**AUTOCMDERRSTS_NEXTERROR:** autocmderrsts_nexterror
6	0h RO	**Reserved**
5	0h RO	**AUTO_CMD_RESP_ERROR:** auto_cmd_resp_error
4	0h RO	**AUTOCMDERRSTS_INDEXERROR:** autocmderrsts_indexerror
3	0h RO	**AUTOCMDERRSTS_ENDBITERROR:** autocmderrsts_endbiterror
2	0h RO	**AUTOCMDERRSTS_CRCERROR:** autocmderrsts_crcerror
1	0h RO	**AUTOCMDERRSTS_TIMEOUTERROR:** autocmderrsts_timeouterror
0	0h RO	**AUTOCMDERRSTS_NOTEXECERROR:** autocmderrsts_notexecerror

13.2.30 REG HOSTCONTROL2 (HOSTCONTROL2) - Offset 3Eh

Host Control2

Type	Size	Offset	Default
MMIO	16 bit	BAR + 3Eh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**HOSTCTRL2_PRESETVALUEENABLE:** hostctrl2_presetvalueenable
14	0h RW	**HOSTCTRL2_ASYNCHINTRENABLE:** hostctrl2_asynchintrenable
13	0h RW	**HOSTCTRL2_ADDRESS_64BIT:** hostctrl2_address_64bit
12	0h RW	**HOSTCTRL2_HOST_VER4_ENB:** hostctrl2_host_ver4_enb

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**HOSTCTRL2_CMD23_ENB:** hostctrl2_cmd23_enb
10	0h RW	**HOSTCTRL2_ADMA2LENGTH_MODE:** hostctrl2_adma2length_mode
9	0h RO	**Reserved**
8	0h RW	**HOSTCTRL2_UHS2_INTRF_ENB:** hostctrl2_uhs2_intrf_enb
7	0h RW	**HOSTCTRL2_SAMPLINGCLKSELECT:** hostctrl2_samplingclkselect
6	0h RW	**HOSTCTRL2_EXECUTETUNING:** hostctrl2_executetuning
5:4	0h RW	**HOSTCTRL2_DRIVERSTRENGTHSEL:** hostctrl2_driverstrengthsel
3	0h RW	**HOSTCTRL2_1P8VSIGNALLINGENA:** hostctrl2_1p8vsignallingena
2:0	0h RW	**HOSTCTRL2_UHSMODESELECT:** hostctrl2_uhsmodeselect

13.2.31 REG CAPABILITIES (CAPABILITIES) - Offset 40h

Host Controller Capabilities

Type	Size	Offset	Default
MMIO	64 bit	BAR + 40h	180000073D68C881h

Bit Range	Default & Access	Field Name (ID): Description
63:61	0h RO	**Reserved**
60	1h RO	**VDD2_1P8_SUPPORT:** vdd2_1p8_support
59	1h RO	**ADMA3_SUPPORT:** adma3_support
58:56	0h RO	**Reserved**
55:48	00h RO	**CLK_MULT:** clk_mult
47:46	0h RO	**RE_TUNING_MODES:** re_tuning_modes
45	0h RO	**USE_TUNG_SDR50:** use_tung_sdr50
44	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
43:40	0h RO	**TIMER_CNT_RETUNG:** timer_cnt_retung
39	0h RO	**Reserved**
38	0h RO	**DRV_TYPED_SUPPORT:** drv_typeD_support
37	0h RO	**DRVTYPEC_SUPPORT:** drvtypeC_support
36	0h RO	**DRVTYPEA_SUPPORT:** drvtypeA_support
35	0h RO	**UHS2_SUPPORT:** uhs2_support
34	1h RO	**DDR50_SUPPORT:** ddr50_support
33	1h RO	**SDR104SUPPORT:** sdr104support
32	1h RO	**SDR50_SUPPORT:** sdr50_support
31:30	0h RO	**SLOT_TYPE:** slot_type
29	1h RO	**ASYNCH_INTR_SUPPORT:** asynch_intr_support
28	1h RO	**SYS_ADDR_64BIT_SUPPORT_V3:** sys_addr_64bit_support_v3
27	1h RO	**SYS_ADDR_64BIT_SUPPORT_V4:** sys_addr_64bit_support_v4
26	1h RO	**VOLT1P8_SUPPORT:** volt1p8_support
25	0h RO	**VOLT3P0_SUPPORT:** volt3p0_support
24	1h RO	**VOLT3P3_SUPPORT:** volt3p3_support
23	0h RO	**SUSP_RESUME_SUPPORT:** susp_resume_support
22	1h RO	**SDMA_SUPPORT:** sdma_support
21	1h RO	**HIGH_SPEED_SUPPORT:** high_speed_support
20	0h RO	**Reserved**
19	1h RO	**ADMA2_SUPPORT:** adma2_support
18	0h RO	**EXTD_MEDIA_BUS:** extd_media_bus
17:16	0h RO	**MAX_BLK_LENGTH:** max_blk_length

Bit Range	Default & Access	Field Name (ID): Description
15:8	C8h RO	**BASE_CLK_FREQ:** base_clk_freq
7	1h RO	**TIMEOUT_CLK_UNIT:** timeout_clk_unit
6	0h RO	**Reserved**
5:0	01h RO	**TIMEOUT_CLKF_REQ:** timeout_clkf_req

13.2.32 REG MAXCURRENTCAP (MAXCURRENTCAP) - Offset 48h

Maximum Current Capabilities

Type	Size	Offset	Default
MMIO	64 bit	BAR + 48h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:40	0h RO	**Reserved**
39:32	00h RO	**MAXCURRENT_1P8V_VDD2:** maxcurrent_1p8v_vdd2
31:24	0h RO	**Reserved**
23:16	00h RW	**MAXCURRENT_1P8V:** maxcurrent_1p8v
15:8	00h RW	**MAXCURRENT_3P0V:** maxcurrent_3p0v
7:0	00h RW	**MAXCURRENT_3P3V:** maxcurrent_3p3v

13.2.33 REG FORCEEVENTFORAUTOCMDERRORSTATUS (FORCEEVENTFORAUTOCMDERRORSTATUS) - Offset 50h

Force Event REGISTER for AUTO CMD Error Status

Type	Size	Offset	Default
MMIO	16 bit	BAR + 50h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7	0h RO	**FORCECMD_NOTISSUEDBY_AUTOCMD12_ERR:** forcecmd_notissuedby_autocmd12_err
6	0h RO	**Reserved**
5	0h RO	**FORCEEVENTAUTOCMDRESPERR:** forceeventautocmdresperr
4	0h RO	**FORCEAUTOCMDINDEXERR:** forceautocmdindexerr
3	0h RO	**FORCEAUTOCMDENDBITERR:** forceautocmdendbiterr
2	0h RO	**FORCEAUTOCMDCRCERR:** forceautocmdcrcerr
1	0h RO	**FORCEAUTOCMDTIMEOUTERR:** forceautocmdtimeouterr
0	0h RO	**FORCEAUTOCMDNOTEXEC:** forceautocmdnotexec

13.2.34 REG FORCEEVENTFORERRINTSTS (FORCEEVENTFORERRINTSTS) - Offset 52h

Force Event Register for Error Interrupt Status

Type	Size	Offset	Default
MMIO	16 bit	BAR + 52h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h WO	**FORCEEVENTFORERRINTSTS_VENDORSPECERRSTS:** forceeventforerrintsts_VendorSpecErrSts
11	0h WO	**FORCEEVENTRESPERROR:** forceeventresperror
10	0h WO	**FORCETUNINGERR:** forcetuningerr
9	0h WO	**FORCEADMAERR:** forceadmaerr
8	0h WO	**FORCEAUTOCMDERR:** forceautocmderr
7	0h WO	**FORCECURRLIMERR:** forcecurrlimerr
6	0h WO	**FORCEDATENDBITERR:** forcedatendbiterr

Bit Range	Default & Access	Field Name (ID): Description
5	0h WO	**FORCEDATCRCERR:** forcedatcrcerr
4	0h WO	**FORCEDATTIMEOUTERR:** forcedattimeouterr
3	0h WO	**FORCECMDINDEXERR:** forcecmdindexerr
2	0h WO	**FORCECMDENDBITERR:** forcecmdendbiterr
1	0h WO	**FORCECMDCRCERR:** forcecmdcrcerr
0	0h WO	**FORCECMDTIMEOUTERR:** forcecmdtimeouterr

13.2.35 REG ADMAERRSTS (ADMAERRSTS) - Offset 54h

ADMA Error Status

Type	Size	Offset	Default
MMIO	8 bit	BAR + 54h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved**
2	0h RO	**ADMAERRSTS_ADMALENMISMATCHERR:** admaerrsts_admalenmismatcherr
1:0	0h RO	**ADMAERRSTS_ADMAERRORSTATE:** admaerrsts_admaerrorstate

13.2.36 REG ADMASYSADDR01 (ADMASYSADDR01) - Offset 58h

ADMA System Address Register01

Type	Size	Offset	Default
MMIO	32 bit	BAR + 58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**ADMA_32BIT_SYSADDRESS:** adma_32bit_sysaddress

13.2.37 REG ADMASYSADDR2 (ADMASYSADDR2) - Offset 5Ch

ADMA System Address Register2

Type	Size	Offset	Default
MMIO	16 bit	BAR + 5Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**ADMA_64BIT_SYSADDRESS2:** adma_64bit_sysaddress2

13.2.38 REG ADMASYSADDR3 (ADMASYSADDR3) - Offset 5Eh

ADMA System Address Register3

Type	Size	Offset	Default
MMIO	16 bit	BAR + 5Eh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**ADMA_64BIT_SYSADDRESS3:** adma_64bit_sysaddress3

13.2.39 REG PRESETVALUE0 (PRESETVALUE0) - Offset 60h

Preset Value Register for Initialization

Type	Size	Offset	Default
MMIO	16 bit	BAR + 60h	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**DRIVERSTRENGTHSELECTVALUE:** DriverStrengthSelectValue
13:11	0h RO	**Reserved**
10	0h RO	**CLOCKGENERATORSELECTVALUE:** ClockGeneratorSelectValue
9:0	004h RO	**SDCLKFREQUENCYSELECTVALUE:** SDCLKFrequencySelectValue

13.2.40 REG PRESETVALUE1 (PRESETVALUE1) - Offset 62h

Preset Value Register for Default Speed

Type	Size	Offset	Default
MMIO	16 bit	BAR + 62h	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**DRIVERSTRENGTHSELECTVALUE:** DriverStrengthSelectValue
13:11	0h RO	**Reserved**
10	0h RO	**CLOCKGENERATORSELECTVALUE:** ClockGeneratorSelectValue
9:0	004h RO	**SDCLKFREQUENCYSELECTVALUE:** SDCLKFrequencySelectValue

13.2.41 REG PRESETVALUE2 (PRESETVALUE2) - Offset 64h

Preset Value Register for High Speed

Type	Size	Offset	Default
MMIO	16 bit	BAR + 64h	0002h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**DRIVERSTRENGTHSELECTVALUE:** DriverStrengthSelectValue
13:11	0h RO	**Reserved**
10	0h RO	**CLOCKGENERATORSELECTVALUE:** ClockGeneratorSelectValue
9:0	002h RO	**SDCLKFREQUENCYSELECTVALUE:** SDCLKFrequencySelectValue

13.2.42 REG PRESETVALUE3 (PRESETVALUE3) - Offset 66h

Preset Value Register for SDR12

Type	Size	Offset	Default
MMIO	16 bit	BAR + 66h	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**DRIVERSTRENGTHSELECTVALUE:** DriverStrengthSelectValue
13:11	0h RO	**Reserved**
10	0h RO	**CLOCKGENERATORSELECTVALUE:** ClockGeneratorSelectValue
9:0	004h RO	**SDCLKFREQUENCYSELECTVALUE:** SDCLKFrequencySelectValue

13.2.43 REG PRESETVALUE4 (PRESETVALUE4) - Offset 68h

Preset Value Register for SDR25

Type	Size	Offset	Default
MMIO	16 bit	BAR + 68h	0002h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**DRIVERSTRENGTHSELECTVALUE:** DriverStrengthSelectValue
13:11	0h RO	**Reserved**
10	0h RO	**CLOCKGENERATORSELECTVALUE:** ClockGeneratorSelectValue
9:0	002h RO	**SDCLKFREQUENCYSELECTVALUE:** SDCLKFrequencySelectValue

13.2.44 REG PRESETVALUE5 (PRESETVALUE5) - Offset 6Ah

Preset Value Register for SDR50

Type	Size	Offset	Default
MMIO	16 bit	BAR + 6Ah	0001h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**DRIVERSTRENGTHSELECTVALUE:** DriverStrengthSelectValue

Bit Range	Default & Access	Field Name (ID): Description
13:11	0h RO	**Reserved**
10	0h RO	**CLOCKGENERATORSELECTVALUE:** ClockGeneratorSelectValue
9:0	001h RO	**SDCLKFREQUENCYSELECTVALUE:** SDCLKFrequencySelectValue

13.2.45 REG PRESETVALUE6 (PRESETVALUE6) - Offset 6Ch

Preset Value Register for SDR104

Type	Size	Offset	Default
MMIO	16 bit	BAR + 6Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**DRIVERSTRENGTHSELECTVALUE:** DriverStrengthSelectValue
13:11	0h RO	**Reserved**
10	0h RO	**CLOCKGENERATORSELECTVALUE:** ClockGeneratorSelectValue
9:0	000h RO	**SDCLKFREQUENCYSELECTVALUE:** SDCLKFrequencySelectValue

13.2.46 REG PRESETVALUE7 (PRESETVALUE7) - Offset 6Eh

Preset Value Register for DDR50

Type	Size	Offset	Default
MMIO	16 bit	BAR + 6Eh	0002h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**DRIVERSTRENGTHSELECTVALUE:** DriverStrengthSelectValue
13:11	0h RO	**Reserved**
10	0h RO	**CLOCKGENERATORSELECTVALUE:** ClockGeneratorSelectValue
9:0	002h RO	**SDCLKFREQUENCYSELECTVALUE:** SDCLKFrequencySelectValue

13.2.47 REG BOOTTIMEOUTCNT (BOOTTIMEOUTCNT) - Offset 70h

Boot Timeout Control

Type	Size	Offset	Default
MMIO	32 bit	BAR + 70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**BOOT_TIMEOUTCNT:** boot_timeoutcnt

13.2.48 REG PRESETVALUE8 (PRESETVALUE8) - Offset 74h

Preset Value for UHS2

Type	Size	Offset	Default
MMIO	16 bit	BAR + 74h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**DRIVERSTRENGTHSELECTVALUE:** DriverStrengthSelectValue
13:11	0h RO	**Reserved**
10	0h RO	**CLOCKGENERATORSELECTVALUE:** ClockGeneratorSelectValue
9:0	000h RO	**SDCLKFREQUENCYSELECTVALUE:** SDCLKFrequencySelectValue

13.2.49 REG ADMA3_LOW (ADMA3_LOW) - Offset 78h

ADMA3 Integrated Descriptor Address Low

Type	Size	Offset	Default
MMIO	32 bit	BAR + 78h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**ADMA3_DESC_ADDR_LOW:** adma3_desc_addr_low

13.2.50 REG SLOTINTRSTS (SLOTINTRSTS) - Offset FCh

Slot Interrupt Status

Type	Size	Offset	Default
MMIO	16 bit	BAR + FCh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:1	00h RO	**SDHCHOSTIF_SLOTINTRSTSSLOT1TO8:** sdhchostif_slotintrstsslot1to8
0	0h RO	**SDHCHOSTIF_SLOTINTRSTSSLOT0:** sdhchostif_slotintrstsslot0

13.2.51 REG HOSTCONTROLLERVER (HOSTCONTROLLERVER) - Offset FEh

Host Controller Version

Type	Size	Offset	Default
MMIO	16 bit	BAR + FEh	1002h

Bit Range	Default & Access	Field Name (ID): Description
15:8	10h RO	**SDHC_VENVERNUM:** SDHC_VENVERNUM
7:0	02h RO	**HOSTCTRL_SPECIFICATIONVERSIONNUMBER:** hostctrl_SpecificationVersionNumber

13.3 SDIO Converge Layer Registers Summary

Table 13-3. Summary of SDIO Converge Layer Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
804h	2	REG SDCARD_SW_LTR_VAL_REG (SW_LTR_VAL)	0000h
808h	2	REG SDCARD_AUTO_LTR_VAL_REG (AUTO_LTR_VAL)	0000h
810h	4	REG SDCARD_CAP_BYP_CTRL_REG (CAP_BYPS)	00000000h
814h	4	REG SDCARD_CAP_BYP_REG_I (CAP_BYPS_REG1)	00000000h
818h	4	REG SDCARD_CAP_BYP_REG_II (CAP_BYPS_REG2)	00000000h
81Ch	4	REG SDCARD_D0I3_CTRL (REG_D0I3)	00000000h
820h	4	REG SDCARD_TX_CMD_DELAY_CONTROL (TX_CMD_DLY)	00000000h
824h	4	REG SDCARD_TX_DELAY_CONTROL_1 (TX_DATA_DLY_1)	00000000h
828h	4	REG SDCARD_TX_DELAY_CONTROL_2 (TX_DATA_DLY_2)	00000000h
82Ch	4	REG SDCARD_RX_DATA_PATH_DELAY_CONTROL_1 (RX_CMD_DATA_DLY_1)	00000000h
834h	4	REG SDCARD_RX_DATA_PATH_DELAY_CONTROL_2 (RX_CMD_DATA_DLY_2)	00000000h
838h	4	REG SDCARD_MASTER_DLL_SW_CTRL (MASTER_DLL)	00000000h
840h	4	REG SDCARD_AUTO_TUNING_VALUE (AUTO_TUNING)	00000000h

13.3.1 REG SDCARD_SW_LTR_VAL_REG (SW_LTR_VAL) — Offset 804h

Software LTR VAL_REG Register

Type	Size	Offset	Default
MMIO	16 bit	BAR + 804h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO	**Reserved**

13.3.2 REG SDCARD_AUTO_LTR_VAL_REG (AUTO_LTR_VAL) — Offset 808h

Auto LTR VAL_REG Register

Note: **NOTE:** Bit definitions are the same as SW_LTR_VAL, offset 804h.

13.3.3 REG SDCARD_CAP_BYP_CTRL_REG (CAP_BYPS) — Offset 810h

Capabilities Bypass Control Register

Note: **NOTE:** Bit definitions are the same as SW_LTR_VAL, offset 804h.

13.3.4 REG SDCARD_CAP_BYP_REG_I (CAP_BYPS_REG1) — Offset 814h

Capabilities Bypass Register I

Note: **NOTE:** Bit definitions are the same as SW_LTR_VAL, offset 804h.

13.3.5 REG SDCARD_CAP_BYP_REG_II (CAP_BYPS_REG2) — Offset 818h

Capabilities Bypass Register II

Note: **NOTE:** Bit definitions are the same as SW_LTR_VAL, offset 804h.

13.3.6 REG SDCARD_D0I3_CTRL (REG_D0I3) — Offset 81Ch

Device Idle D0i3 Register

Note: **NOTE:** Bit definitions are the same as SW_LTR_VAL, offset 804h.

13.3.7 REG SDCARD_TX_CMD_DELAY_CONTROL (TX_CMD_DLY) — Offset 820h

Tx CMD Delay Control Register

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14:8	04h RW	**DDR Mode**: Tx CMD Delay (DDR Mode). 0-39: Select number of active delay elements. Each = 125pSec. 40-127: Reserved
7	0h RO	**Reversed**
6:0	00h RW	**SDR_MODE**: Tx CMD Delay (SDR Mode). 0-39: Select number of active delay elements. Each = 125pSec. 40-127: Reserved

Note: **NOTE:** Bit definitions are the same as SW_LTR_VAL, offset 804h.

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13.3.8 REG SDCARD_TX_DELAY_CONTROL_1 (TX_DATA_DLY_1) — Offset 824h

Tx Delay Control 1 Register

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14:8	0Ah RW	**HS400_MODE**: Tx Data Delay (HS400 Mode). 0-78: Select number of active delay elements. Each = 125pSec. 79-127: Reserved
7	0h RO	**Reversed**
6:0	18h RW	**SDR104_HS200_MODE:** Tx Data Delay (SDR104/HS200 Mode) 0-79: Select number of active delay elements. Each = 125pSec. 80-127: Reserved

Note: **NOTE:** Bit definitions are the same as SW_LTR_VAL, offset 804h.

<Enter text here>

13.3.9 REG SDCARD_TX_DELAY_CONTROL_2 (TX_DATA_DLY_2) — Offset 828h

Tx Delay Control 2 Register

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:24	1Ch RW	**SDR50_MODE**: Tx Data Delay (SDR50 Mode). 0-79: Select number of active delay elements. Each = 125pSec. 80-127: Reserved
23	0h RO	**Reversed**
22:16	1Ch RW	**DDR50_MODE:** Tx Data Delay (DDR50 Mode). 0-78: Select number of active delay elements. Each = 125pSec. 79-127: Reserved
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:8	1Ch RW	**SDR25_HS50_MODE:** Tx Data Delay (SDR25/HS50 Mode). 0-79: Select number of active delay elements. Each = 125pSec. 80-127: Reserved
7	0h RO	**Reserved**
6:0	00h RW	**SDR12_COMP_MODE:** Tx Data Delay (SDR12/Compatibility Mode). 0-79: Select number of active delay elements. Each = 125pSec. 80-127: Reserved

Note: **NOTE:** Bit definitions are the same as SW_LTR_VAL, offset 804h.

13.3.10 REG SDCARD_RX_DATA_PATH_DELAY_CONTROL_1 (RX_CMD_DATA_DLY_1) — Offset 82Ch

Rx CMD Data Delay Control 1 Register

Note: **NOTE:** Bit definitions are the same as SW_LTR_VAL, offset 804h.

13.3.11 REG SDCARD_RX_DATA_PATH_DELAY_CONTROL_2 (RX_CMD_DATA_DLY_2) — Offset 834h

Rx CMD Data Path Delay Control 2 Register

<Enter text here>

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RW	**CLK_SOURCE**: Clock Source for Rx Path 00: Rx Clock after Output Buffer 01: Rx Clock before Output Buffer 10: Automatic Selection based on mode (HS 200 before buffer, all others after buffer) 11: Reserved
15:14	0h RO	**Reversed**
13:8	18h RW	**PATH_PLL:** Rx Path PLL #3 Delay value For Auto Tuning Mode 0-39: Select the required delay, as a multiple of 125pSec. 40-63: Reserved
7	0h RO	**Reserved**
6:0	1Ch RW	**CMD_DATA_SDR104_HS200:** Rx CMD + Data Delay (SDR104/HS200 Mode) 0-79: Select the required delay, as a multiple of 125pSec. 80-127: Reserved

Note: **NOTE:** Bit definitions are the same as SW_LTR_VAL, offset 804h.

13.3.12 REG SDCARD_MASTER_DLL_SW_CTRL (MASTER_DLL) — Offset 838h

Master DLL Software CTRL Register

Note: **NOTE:** Bit definitions are the same as SW_LTR_VAL, offset 804h.

13.3.13 REG SDCARD_AUTO_TUNING_VALUE (AUTO_TUNING) — Offset 840h

Auto Tuning Value Register

Note: **NOTE:** Bit definitions are the same as SW_LTR_VAL, offset 804h.

14 Inter-Integrated Circuit (I^2C) Controller

14.1 I^2C Configuration Registers Summary

This chapter records the registers of the I^2C device. The device contains multiple I^2C controller:

- I^2C Controller #0 - Bus: 0, Device: 21, Function 0
- I^2C Controller #1 - Bus: 0, Device: 21, Function 1
- I^2C Controller #2 - Bus: 0, Device: 21, Function 2
- I^2C Controller #3 - Bus: 0, Device: 21, Function 3
- I^2C Controller #4 - Bus: 0, Device: 25, Function 0
- I^2C Controller #5 - Bus: 0, Device: 25, Function 1
- I^2C Controller #6 - Bus: 0, Device: 16, Function 0
- I^2C Controller #7 - Bus: 0, Device: 16, Function 1

DID Values:

- I^2C Controller #0:- D21:F0 - 4B78h
- I^2C Controller #1:- D21:F1 - 4B79h
- I^2C Controller #2:- D21:F2 - 4B7Ah
- I^2C Controller #3:- D21:F3 - 4B7Bh
- I^2C Controller #4:- D25:F0 - 4B4Bh
- I^2C Controller #5:- D25:F1 - 4B4Ch
- I^2C Controller #6:- D16:F0 - 4B44h
- I^2C Controller #7:- D16:F1 - 4B45h

Table 14-1. Summary of Bus: 0, Device: 21, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID And Vendor ID Register (DEVVENDID)	4B788086h
4h	4	Status And Command (STATUSCOMMAND)	00100000h
8h	4	Revision ID And Class Code (REVCLASSCODE)	0C800000h
Ch	4	Cache Line Latency Header And BIST (CLLATHEADERBIST)	00800000h
10h	4	Base Address Register (BAR)	00000000h
14h	4	Base Address Register High (BAR_HIGH)	00000000h
18h	4	Base Address Register1 (BAR1)	00000004h
1Ch	4	Base Address Register1 High (BAR1_HIGH)	00000000h
2Ch	4	Subsystem Vendor And Subsystem ID (SUBSYSTEMID)	00000000h
30h	4	Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)	00000000h
34h	4	Capabilities Pointer Register (CAPABILITYPTR)	00000080h
3Ch	4	Interrupt Register (INTERRUPTREG)	00000000h
80h	4	PowerManagement Capability ID (POWERCAPID)	00039001h
84h	4	Power Management Control And Status Register (PMECTRLSTATUS)	00000008h
90h	4	PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD)	F0140009h
94h	4	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG)	01400010h
98h	4	Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)	00002101h
9Ch	4	Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG)	000024C1h
A0h	4	D0i3 And Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG)	000F0800h
B0h	4	General Purpose Read Write Register1 (GEN_REGRW1)	00000000h
B4h	4	General Purpose Read Write Register2 (GEN_REGRW2)	00000000h
B8h	4	General Purpose Read Write Register3 (GEN_REGRW3)	00000000h
BCh	4	General Purpose Read Write Register4 (GEN_REGRW4)	00000000h
C0h	4	General Purpose Input Register (GEN_INPUT_REG)	00000000h
F8h	4	Manufacturers ID (MANID)	00000000h

14.1.1 Device ID And Vendor ID Register (DEVVENDID) - Offset 0h

Device ID and Vendor ID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + 0h	4B788086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4B78h RO/P	**Device ID Field (DEVICEID):** Device ID identifies the particular PCI device
15:0	8086h RO	**Vendor ID Field (VENDORID):** Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device

14.1.2 Status And Command (STATUSCOMMAND) - Offset 4h

Command register and Status register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW/1C	**RMA Field (RMA):** Received Master Abort
28	0h RW/1C	**RTA Field (RTA):** Received Target Abort
27:21	0h RO	**Reserved**
20	1h RO	**Cap List Field (CAPLIST):** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**Interrupt Status Field (INTR_STATUS):** Interrupt Status: This bit reflects state of interrupt in the device
18:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** Interrupt Disable
9	0h RO	**Reserved**
8	0h RW	**SERR Enable Field (SERR_ENABLE):** SERR Enable Not implemented
7:3	0h RO	**Reserved**
2	0h RW	**BME Field (BME):** Bus Master Enable
1	0h RW	**MSE Field (MSE):** Memory Space Enable
0	0h RO	**Reserved**

14.1.3 Revision ID And Class Code (REVCLASSCODE) - Offset 8h

Revision ID register and Class Code register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + 8h	0C800000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0C8000h RO	**Revision ID Field (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	00h RO/P	**Class Code Field (RID):** Revision ID identifies the revision of particular PCI device.

14.1.4 Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch

Cache Line size as RW with def 0 Latency timer RW with def 0 Header type with Type 0 configuration header and Reserved BIST register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + Ch	00800000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	1h RO	**Multi Function Device Field (MULFNDEV):** Multi-Function Device
22:16	00h RO	**Header Type Field (HEADERTYPE):** Header Type: Implements Type 0 Configuration header
15:8	00h RO	**Latency Timer Field (LATTIMER):** Latency Timer:. This register is implemented as R/W with default as 0
7:0	00h RW/P	**Cache Line Size Field (CACHELINE_SIZE):** Cache line Size

14.1.5 Base Address Register (BAR) - Offset 10h

Base Address Register Low [31:2] type[2:1] in 32bit or 64bit address range and memory space indicator [0].

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR):** Base Address Register Low Base address of the OCP fabric memory space. Taken from Strap values as ones
11:4	00h RO	**Size Field (SIZEINDICATOR):** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**Prefetchable Field (PREFETCHABLE):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE0):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** Memory Space Indicator: 0 indicates this BAR is present in the memory space.

14.1.6 Base Address Register High (BAR_HIGH) - Offset 14h

Base Address Register High enabled if [2:1] of BAR is 10.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR_HIGH):** Base Address High - MSB

14.1.7 Base Address Register1 (BAR1) - Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K type in [2:1] and Memory Space Indicator in [0].

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + 18h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR1):** Base Address1 This field is present if BAR1 is enabled through private configuration space.
11:4	00h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	2h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

14.1.8 Base Address Register1 High (BAR1_HIGH) - Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1 register is 10.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR1_HIGH):** Base Address: Base address of the OCP fabric memory space. Taken from Strap values as ones

14.1.9 Subsystem Vendor And Subsystem ID (SUBSYSTEMID) - Offset 2Ch

SVID register along with SID register is to distinguish subsystem from another.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system.
15:0	0000h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

14.1.10 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h

Expansion ROM Base Address register is a RO indicates support for Expansion ROMs.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION ROM base address field (EXPANSION_ROM_BASE):** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

14.1.11 Capabilities Pointer Register (CAPABILITYPTR) - Offset 34h

Capabilities Pointer register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Capabilities Pointer: Indicates what the next capability is.

14.1.12 Interrupt Register (INTERRUPTREG) - Offset 3Ch

Interrupt line Register isn't used in Bridge directly Interrupt Pin register reflects the IPIN value in private configuration space. Min_GNT register indicating the requirements of latency timers and Max_LAT register max latency.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + 3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**Min GNT Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers // Re-Check Desc Padma

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11:8	0h RO	**Interrupt Pin Field (INTPIN):** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW/P	**Int Line Field (INTLINE):** Interrupt Line: It is used to communicate to software the interrupt line to which the interrupt pin is connected

14.1.13 Power Management Capability ID (POWERCAPID) - Offset 80h

Power Management Capability ID register points to Next Capability Structure and Power Management Capability with Power Management Capabilities register for PME Support and Version.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + 80h	00039001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved**
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h RO	**Next Cap Field (NXTCAP):** Next Capability: Points to the next capability structure.
7:0	01h RO	**Power Capability ID Field (POWER_CAP):** Power Management Capability: Indicates this is power management capability

14.1.14 Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h

Power Management Control and Status register to set and read PME Status, PME Enable, No Soft Reset and Power State.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/P	**PME Status Field (PMESTATUS):** PME Status
14:9	0h RO	**Reserved**
8	0h RW/P	**PME Enable Field (PMEENABLE):** PME Enable
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset
2	0h RO	**Reserved**
1:0	0h RW	**Power State Field (POWERSTATE):** Power State: This field is used both to determine the current Power State and to set a new Power State

14.1.15 PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h

PCI Device Vendor Specific Capability register defines Vendor Specific Capability ID, Revision, Length, Next Capability and CAPID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + 90h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision ID Field (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	00h RO	**Next Capability Field (NEXT_CAP):** Next Capability
7:0	09h RO	**Capability ID Field (CAPID):** Capability ID

14.1.16 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h

Extended Vendor Capability register for VSEC Length, Revision and ID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific ID Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor specific Extended Capability revision
15:0	0010h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

14.1.17 Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h

Software location pointer in MMIO space as an offset specified by BAR.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + 98h	00002101h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000210h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR BAR Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	1h RO	**SW LTR Valid Field (SW_LAT_VALID):** This value is reflected from the SW LTR valid strap at the top level

14.1.18 Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch

Device IDLE Pointer register giving details on Device MMIO Offset Location, BAR NUM and D0i3 Valid Strap.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + 9Ch	000024C1h

Bit Range	Default & Access	Field Name (ID): Description
31:4	000024Ch RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** Contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** BAR Num: Indicates that the D0i3 MMIO location is always at BAR0
0	1h RO	**D0i3 Valid Field (VALID):** Valid: This value is reflected from the D0i3 valid strap at the top level.

14.1.19 D0i3 And Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h

D0idle_Max_Power_On_Latency register set at boot and power control enable register to enable communication with the PGCB block below the Bridge.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + A0h	000F0800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW/P	**HAE Field (HAE):** Hardware Autonomous Enable
20	0h RO	**Reserved**
19	1h RW/P	**Sleep Enable Field (SLEEP_EN):** Sleep Enable
18	1h RW/P	**D3 Hen Field (PGE):** DEVIDLE Enable (DEVIDLEN): If '1', then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set.
17	1h RW/P	**Device Idle En Field (I3E):** PMCRE: PMC Request Enable
16	1h RW/P	**PMC Request Enable Field (PMCRE):** D3-Hot Enable (D3HEN): If '1', then function will power gate when idle and the PMCSR[1:0] register in the function = '11' (D3).
15:13	0h RO	**Reserved**
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** Power On Latency Scale
9:0	000h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** Power On Latency value

14.1.20 General Purpose Read Write Register1 (GEN_REGRW1) - Offset B0h

General Purpose PCI Read Write Register1.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_REG_RW1):** General Purpose I2C Register: This register value is brought out as GEN_REG_RW1

14.1.21 General Purpose Read Write Register2 (GEN_REGRW2) - Offset B4h

General Purpose PCI Read Write Register2.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_REG_RW2):** General Purpose I2C Register: This register value is brought out as GEN_REG_RW2

14.1.22 General Purpose Read Write Register3 (GEN_REGRW3) - Offset B8h

General Purpose PCI Read Write Register3.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_REG_RW3):** General Purpose I2C Register: This register value is brought out as GEN_REG_RW3

14.1.23 General Purpose Read Write Register4 (GEN_REGRW4) - Offset BCh

General Purpose PCI Read Write Register4.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_REG_RW4):** General Purpose I2C Register: This register value is brought out as GEN_REG_RW4

14.1.24 General Purpose Input Register (GEN_INPUT_REG) - Offset C0h

General Purpose Input Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General Purpose I2C Register: This register value is brought out as GEN_REG_INPUT_RW

14.1.25 Manufacturers ID (MANID) - Offset F8h

Manufacturers ID register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:21, F:0] + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/P	**Manufacturers ID Field (MANID):** Manufacturer ID: Default value comes from straps.

14.2 I²C Memory Mapped Registers Summary

Table 14-2. Summary of I²C Memory Mapped Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	REG IC_CON (IC_CON)	00000077h
4h	4	REG IC_TAR (IC_TAR)	00001055h
Ch	4	REG IC_HS_MADDR (IC_HS_MADDR)	00000001h
10h	4	REG IC_DATA_CMD (IC_DATA_CMD)	00000000h
14h	4	REG IC_SS_SCL_HCNT (IC_SS_SCL_HCNT)	000001F4h
18h	4	REG IC_SS_SCL_LCNT (IC_SS_SCL_LCNT)	0000024Ch
1Ch	4	REG IC_FS_SCL_HCNT (IC_FS_SCL_HCNT)	0000004Bh
20h	4	REG IC_FS_SCL_LCNT (IC_FS_SCL_LCNT)	000000A3h
24h	4	REG IC_HS_SCL_HCNT (IC_HS_SCL_HCNT)	00000008h
28h	4	REG IC_HS_SCL_LCNT (IC_HS_SCL_LCNT)	00000014h
2Ch	4	REG IC_INTR_STAT (IC_INTR_STAT)	00000000h
30h	4	REG IC_INTR_MASK (IC_INTR_MASK)	000008FFh
34h	4	REG IC_RAW_INTR_STAT (IC_RAW_INTR_STAT)	00000000h
38h	4	REG IC_RX_TL (IC_RX_TL)	00000000h
3Ch	4	REG IC_TX_TL (IC_TX_TL)	00000000h
40h	4	REG IC_CLR_INTR (IC_CLR_INTR)	00000000h
44h	4	REG IC_CLR_RX_UNDER (IC_CLR_RX_UNDER)	00000000h
48h	4	REG IC_CLR_RX_OVER (IC_CLR_RX_OVER)	00000000h
4Ch	4	REG IC_CLR_TX_OVER (IC_CLR_TX_OVER)	00000000h
50h	4	REG IC_CLR_RD_REQ (IC_CLR_RD_REQ)	00000000h
54h	4	REG IC_CLR_TX_ABRT (IC_CLR_TX_ABRT)	00000000h
58h	4	REG IC_CLR_RX_DONE (IC_CLR_RX_DONE)	00000000h
5Ch	4	REG IC_CLR_ACTIVITY (IC_CLR_ACTIVITY)	00000000h
60h	4	REG IC_CLR_STOP_DET (IC_CLR_STOP_DET)	00000000h
64h	4	REG IC_CLR_START_DET (IC_CLR_START_DET)	00000000h
68h	4	REG IC_CLR_GEN_CALL (IC_CLR_GEN_CALL)	00000000h
6Ch	4	REG IC_ENABLE (IC_ENABLE)	00000000h
70h	4	REG IC_STATUS (IC_STATUS)	00000006h
74h	4	REG IC_TXFLR (IC_TXFLR)	00000000h
78h	4	REG IC_RXFLR (IC_RXFLR)	00000000h
7Ch	4	REG IC_SDA_HOLD (IC_SDA_HOLD)	00000001h
80h	4	REG IC_TX_ABRT_SOURCE (IC_TX_ABRT_SOURCE)	00000000h
88h	4	REG IC_DMA_CR (IC_DMA_CR)	00000000h
8Ch	4	REG IC_DMA_TDLR (IC_DMA_TDLR)	00000000h
90h	4	REG IC_DMA_RDLR (IC_DMA_RDLR)	00000000h
94h	4	REG IC_SDA_SETUP (IC_SDA_SETUP)	00000064h
98h	4	REG IC_ACK_GENERAL_CALL (IC_ACK_GENERAL_CALL)	00000001h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
9Ch	4	REG IC_ENABLE_STATUS (IC_ENABLE_STATUS)	00000000h
A0h	4	REG IC_FS_SPKLEN (IC_FS_SPKLEN)	00000007h
204h	4	REG RESETS (RESETS)	00000000h
210h	4	REG ACTIVELTR_VALUE (ACTIVELTR_VALUE)	00000800h
214h	4	REG IDLELTR_VALUE (IDLELTR_VALUE)	00000800h
218h	4	REG TX_ACK_COUNT (TX_ACK_COUNT)	00000000h
21Ch	4	REG RX_BYTE_COUNT (RX_BYTE_COUNT)	00000000h
220h	4	REG TX_COMPLETE_INTR_STAT (TX_COMPLETE_INTR_STAT)	00000000h
224h	4	REG TX_COMPLETE_INTR_CLR (TX_COMPLETE_INTR_CLR)	00000000h
228h	4	REG SW_SCRATCH_0 (SW_SCRATCH_0)	00000000h
22Ch	4	REG SW_SCRATCH_1 (SW_SCRATCH_1)	00000000h
230h	4	REG SW_SCRATCH_2 (SW_SCRATCH_2)	00000000h
234h	4	REG SW_SCRATCH_3 (SW_SCRATCH_3)	00000000h
238h	4	REG CLOCK_GATE (CLOCK_GATE)	00000000h
240h	4	REG REMAP_ADDR_LO (REMAP_ADDR_LO)	00000000h
244h	4	REG REMAP_ADDR_HI (REMAP_ADDR_HI)	00000000h
24Ch	4	REG DEVIDLE_CONTROL (DEVIDLE_CONTROL)	00000008h
280h	4	REG I2C_HVM_MISR_CRCOUT (I2C_HVM_MISR_CRCOUT)	0000FFFFh
2FCh	4	REG CAPABLITIES (CAPABLITIES)	00000000h
800h	4	REG SAR_LO0 (SAR_LO0)	00000000h
804h	4	REG SAR_HI0 (SAR_HI0)	00000000h
808h	4	REG DAR_LO0 (DAR_LO0)	00000000h
80Ch	4	REG DAR_HI0 (DAR_HI0)	00000000h
810h	4	REG LLP_LO0 (LLP_LO0)	00000000h
814h	4	REG LLP_HI0 (LLP_HI0)	00000000h
818h	4	REG CTL_LO0 (CTL_LO0)	00000000h
81Ch	4	REG CTL_HI0 (CTL_HI0)	00000000h
820h	4	REG SSTAT0 (SSTAT0)	00000000h
828h	4	REG DSTAT0 (DSTAT0)	00000000h
830h	4	REG SSTATAR_LO0 (SSTATAR_LO0)	00000000h
834h	4	REG SSTATAR_HI0 (SSTATAR_HI0)	00000000h
838h	4	REG DSTATAR_LO0 (DSTATAR_LO0)	00000000h
83Ch	4	REG DSTATAR_HI0 (DSTATAR_HI0)	00000000h
840h	4	REG CFG_LO0 (CFG_LO0)	00000203h
844h	4	REG CFG_HI0 (CFG_HI0)	00000000h
848h	4	REG SGR0 (SGR0)	00000000h
850h	4	REG DSR0 (DSR0)	00000000h
AC0h	4	REG RawTfr (RAWTFR)	00000000h
AC8h	4	REG RawBlock (RAWBLOCK)	00000000h
AD0h	4	REG RawSrcTran (RAWSRCTRAN)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
AD8h	4	REG RawDstTran (RAWDSTTRAN)	00000000h
AE0h	4	REG RawErr (RAWERR)	00000000h
AE8h	4	REG StatusTfr (STATUSTFR)	00000000h
AF0h	4	REG StatusBlock (STATUSBLOCK)	00000000h
AF8h	4	REG StatusSrcTran (STATUSSRCTRAN)	00000000h
B00h	4	REG StatusDstTran (STATUSDSTTRAN)	00000000h
B08h	4	REG StatusErr (STATUSERR)	00000000h
B10h	4	REG MaskTfr (MASKTFR)	00000000h
B18h	4	REG MaskBlock (MASKBLOCK)	00000000h
B20h	4	REG MaskSrcTran (MASKSRCTRAN)	00000000h
B28h	4	REG MaskDstTran (MASKDSTTRAN)	00000000h
B30h	4	REG MaskErr (MASKERR)	00000000h
B38h	4	REG ClearTfr (CLEARTFR)	00000000h
B40h	4	REG ClearBlock (CLEARBLOCK)	00000000h
B48h	4	REG ClearSrcTran (CLEARSRCTRAN)	00000000h
B50h	4	REG ClearDstTran (CLEARDSTTRAN)	00000000h
B58h	4	REG ClearErr (CLEARERR)	00000000h
B60h	4	REG StatusInt (STATUSINT)	00000000h
B98h	4	REG DmaCfgReg (DMACFGREG)	00000000h
BA0h	4	REG ChEnReg (CHENREG)	00000000h

14.2.1 REG IC_CON (IC_CON) - Offset 0h

I2C Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 0h	00000077h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9	0h RW	**RX_FIFO_FULL_HLD_CTRL:** This bit controls whether DW_apb_i2c should hold the bus when the Rx FIFO is physically full to its RX_BUFFER_DEPTH, as in the IC_RX_FULL_HLD_BUS_EN parameter.
8	0h RW	**TX_EMPTY_CTRL:** This bit controls the generation of the TX_EMPTY interrupt, as in the IC_RAW_INTR_STAT register .

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**STOP_DET_IFADDRESSED:** Dependencies: This register bit value is applicable in the slave mode only (MASTER_MODE = 1b0) In slave mode: 1b1 issues the STOP_DET interrupt only when it is addressed. 1b0 issues the STOP_DET irrespective of whether it's addressed or not.
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled. If this bit is set (slave is disabled), the function only works as a master and does not perform any action that requires a slave. 0:Reserved 1: slave is disabled
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when I2C is acting as a master. 0: Restart disable 1: Restart enable When the RESTART is disabled, the IP is incapable of performing the following functions: Sending a START BYTE Performing any high-speed mode operation Performing direction changes in combined format mode Performing a read operation with a 10-bit address By replacing RESTART condition followed by a STOP and a subsequent START condition, split operations are broken down into multiple transfers. If the above operations are performed, it will result in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register
4	1h RO	**IC_10BITADDR_MASTER_RD_ONLY:** Identifies if I2C operates in 7 or 10 bit addressing, 0: 7-bit addressing 1: 10-bit addressing
3	0h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7-bit or 10-bit addresses.
2:1	3h RW	**SPEED:** These bits controls at which speed the I2C operates; its setting is relevant only if one is operating the I2C in master mode. 01: standard mode (0 to 100 kbit/s) 10: fast mode (<= 400 kbit/s) 11: High Speed Mode (<= 3.4 Mbit/s)
0	1h RW	**MASTER_MODE:** This bit controls whether I2C master is enabled. 0 = Reserved 1 = Master Enabled Note: For Master Device Configuration Software must ensure that this bit is set to 1, and bit 6 must also be set to 1. Else this will result in configuration error.

14.2.2 REG IC_TAR (IC_TAR) - Offset 4h

I2C Target Address Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4h	00001055h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	1h RW	**IC_10BITADDR_MASTER:** This bit controls whether the I2C starts its transfers in 7-or 10-bit addressing mode when acting as a master. 0: 7 bit addressing 1: 10-bit addressing
11	0h RW	**SPECIAL:** This bit indicates whether software performs a General Call or START BYTE command. 0: ignore bit 10 GC_OR_START and use IC_TAR normally. 1: perform special I2C command as specified in GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call or START byte command is to be performed by the I2C. 0: General Call Address after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. The I2C remains in General Call mode until the SPECIAL bit value (bit 11) is cleared. 1: START BYTE
9:0	055h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. Note: If the IC_TAR and IC_SAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself; it can transmit to only a slave.

14.2.3 REG IC_HS_MADDR (IC_HS_MADDR) - Offset Ch

I2C High Speed Master Mode Code Address Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + Ch	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight high speed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0s if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2).

14.2.4 REG IC_DATA_CMD (IC_DATA_CMD) - Offset 10h

I2C Data Command Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h WO	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. 1 RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; 0 - RESTART is issued only if the transfer direction is changing from the previous command

Bit Range	Default & Access	Field Name (ID): Description
9	0h WO	**STOP:** This bit controls whether a STOP is issued after the byte is sent or received. 1 - STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus. 0 - STOP is not issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.
8	0h WO	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the I2C acts as a slave. It controls only the direction when it acts as a master. 1 = Read. 0 = Write When a command is entered in the TX FIFO, this bit distinguishes the write and read commands. In slave-receiver mode, this bit is a don't care because writes to this register are not required. In slave-transmitter mode, a 0 indicates that the data in IC_DATA_CMD is to be transmitted. When programming this bit, you should remember the following: attempting to perform a read operation after a General Call command has been sent results in a TX_ABRT interrupt (bit 6 of the IC_RAW_INTR_STAT register), unless bit 11 (SPECIAL) in the IC_TAR register has been cleared. If a 1 is written to this bit after receiving a RD_REQ interrupt, then a TX_ABRT interrupt occurs.
7:0	00h RW	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the I2C. However, when you read this register, these bits return the value of data received on the I2C interface.

14.2.5 REG IC_SS_SCL_HCNT (IC_SS_SCL_HCNT) - Offset 14h

Standard Speed I2C Clock SCL High Count Register. This register sets the SCL clock high-period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The register is only used in Master mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14h	000001F4h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	01F4h RW	**IC_SS_SCL_HCNT:** This register sets the SCL clock high-period count for standard speed. The value of the registers should be within the range {6,65525}.

14.2.6 REG IC_SS_SCL_LCNT (IC_SS_SCL_LCNT) - Offset 18h

Standard Speed I2C Clock SCL Low Count Register. This register sets the SCL clock low-period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The register is only used in Master mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 18h	0000024Ch

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	024Ch RW	**IC_SS_SCL_LCNT:** Standard Speed I2C Clock SCL Low Count Register. The register value should always be >= 8

14.2.7 REG IC_FS_SCL_HCNT (IC_FS_SCL_HCNT) - Offset 1Ch

Fast Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1Ch	0000004Bh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	004Bh RW	**IC_FS_SCL_HCNT:** This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and STARTBYTE or General CALL. The minimum value of this field is 6.

14.2.8 REG IC_FS_SCL_LCNT (IC_FS_SCL_LCNT) - Offset 20h

Fast Speed I2C Clock SCL Low Count Register. This register must be set before any I2C bus transaction can take place to ensure proper I/O timing.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 20h	000000A3h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	00A3h RW	**IC_FS_SCL_LCNT:** This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. The register should be programmed with a minimum value of 8.

14.2.9 REG IC_HS_SCL_HCNT (IC_HS_SCL_HCNT) - Offset 24h

High Speed I2C Clock SCL High Count Register. This register must be set before any I2C bus transaction can take place to ensure proper I/O timing.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 24h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0008h RW	**IC_HS_SCL_HCNT:** IC_HS_SCL_HCNT_Field

14.2.10 REG IC_HS_SCL_LCNT (IC_HS_SCL_LCNT) - Offset 28h

High Speed I2C Clock SCL Low Count Register. This register must be set before any I2C bus transaction can take place to ensure proper I/O timing.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 28h	00000014h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0014h RW	**IC_HS_SCL_LCNT:** IC_HS_SCL_LCNT_Field

14.2.11 REG IC_INTR_STAT (IC_INTR_STAT) - Offset 2Ch

I2C Interrupt Status Register. Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RO	**R_MASTER_ON_HOLD:** Indicates whether a master is holding the bus and the TX FIFO is empty. Enabled only when I2C_DYNAMIC_TAR_UPDATE = 1 and IC_EMPTYFIFO_HOLD_MASTER_EN = 1
12	0h RO	**R_RESTART_DET:** Indicates whether a RESTART condition has occurred on the I2C interface when DW_apb_i2c is operating in slave mode and the slave is the addressed slave. Enabled only when IC_SLV_RESTART_DET_EN = 1 NOTE: However, in high-speed mode or during a START BYTE transfer, the RESTART comes before the address field as per the I2C protocol. In this case, the slave is not the addressed slave when the RESTART is issued, therefore DW_apb_i2c does not generate the RESTART_DET interrupt.
11	0h RO	**R_GEN_CALL:** Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register.
10	0h RO	**R_START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO	**R_STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode
8	0h RO	**R_ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the DW_apb_i2c, Reading the IC_CLR_ACTIVITY register, Reading the IC_CLR_INTR register, System reset
7	0h RO	**R_RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0h RO	**R_TX_ABRT:** This bit indicates if DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I2C master or an I2C slave, as a transmit abort. When this bit is set to 1, the IC_TX_ABRT_SOURCE register indicates the reason why the transmit abort takes places. NOTE: The DW_apb_i2c flushes/resets/empties the TX FIFO whenever this bit is set. The TX FIFO remains in this flushed state until the register IC_CLR_TX_ABRT is read. Once this read is performed, the TX FIFO is then ready to accept more data bytes from the APB interface.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**R_RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c. The DW_apb_i2c holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the IC_DATA_CMD register. This bit is set to 0 just after the processor reads the IC_CLR_RD_REQ register
4	0h RO	**R_TX_EMPTY:** The behavior of the TX_EMPTY interrupt status differs based on the TX_EMPTY_CTRL selection in the IC_CON register. When TX_EMPTY_CTRL = 0: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register. When TX_EMPTY_CTRL = 1: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register and the transmission of the address/data from the internal shift register for the most recently popped command is completed. It is automatically cleared by hardware when the buffer level goes above the threshold. When IC_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer any activity, then with ic_en=0, this bit is set to 0.
3	0h RO	**R_TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.
2	0h RO	**R_RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (IC_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the IC_ENABLE bit 0 is programmed with a 0, regardless of the activity that continues.
1	0h RO	**R_RX_OVER:** Set if the receive buffer is completely filled to IC_RX_BUFFER_DEPTH and an additional byte is received from an external I2C device. The DW_apb_i2c acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.
0	0h RO	**R_RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.

14.2.12 REG IC_INTR_MASK (IC_INTR_MASK) - Offset 30h

I2C Interrupt Mask Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 30h	000008FFh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW	**M_MASTER_ON_HOLD:** This bit masks the R_MST_ON_HOLD interrupt bit in the IC_INTR_STAT register.
12	0h RO	**M_RESTART_DET_READ_ONLY:** This bit masks the R_RESTART_DET interrupt status bit in the IC_INTR_STAT register.
11	1h RW	**M_GEN_CALL:** M_GEN_CALL_Field
10	0h RW	**M_START_DET:** M_START_DET_Field
9	0h RW	**M_STOP_DET:** M_STOP_DET_Field
8	0h RW	**M_ACTIVITY:** M_ACTIVITY_Field
7	1h RW	**M_RX_DONE:** M_RX_DONE_Field
6	1h RW	**M_TX_ABRT:** M_TX_ABRT_Field
5	1h RW	**M_RD_REQ:** M_RD_REQ_Field
4	1h RW	**M_TX_EMPTY:** M_TX_EMPTY_Field
3	1h RW	**M_TX_OVER:** M_TX_OVER_Field
2	1h RW	**M_RX_FULL:** M_RX_FULL_Field
1	1h RW	**M_RX_OVER:** M_RX_OVER_Field
0	1h RW	**M_RX_UNDER:** M_RX_UNDER_Field

14.2.13 REG IC_RAW_INTR_STAT (IC_RAW_INTR_STAT) - Offset 34h

I2C Raw Interrupt Status Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RO	**MASTER_ON_HOLD:** Same as in Reg_IC_INTR_STAT
12	0h RO	**RESTART_DET:** Same as in Reg_IC_INTR_STAT
11	0h RO	**GEN_CALL:** Same as in Reg_IC_INTR_STAT
10	0h RO	**START_DET:** Same as in Reg_IC_INTR_STAT
9	0h RO	**STOP_DET:** Same as in Reg_IC_INTR_STAT
8	0h RO	**RAW_INTR_ACTIVITY:** Same as in Reg_IC_INTR_STAT
7	0h RO	**RX_DONE:** Same as in Reg_IC_INTR_STAT
6	0h RO	**TX_ABRT:** Same as in Reg_IC_INTR_STAT
5	0h RO	**RD_REQ:** Same as in Reg_IC_INTR_STAT
4	0h RO	**TX_EMPTY:** Same as in Reg_IC_INTR_STAT
3	0h RO	**TX_OVER:** Same as in Reg_IC_INTR_STAT
2	0h RO	**RX_FULL:** Same as in Reg_IC_INTR_STAT
1	0h RO	**RX_OVER:** Same as in Reg_IC_INTR_STAT
0	0h RO	**RX_UNDER:** Same as in Reg_IC_INTR_STAT

14.2.14 REG IC_RX_TL (IC_RX_TL) - Offset 38h

I2C Receive FIFO Threshold Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RX_TL:** Receive FIFO Threshold Level. Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in IC_RAW_INTR_STAT register). The valid range is 0-0x3F. (Values > 0x3F are set to depth of the buffer). A value of 0 sets the threshold for 1 entry, and a value of 63 sets the threshold for 64 entries.

14.2.15 REG IC_TX_TL (IC_TX_TL) - Offset 3Ch

I2C Transmit FIFO Threshold Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**TX_TL:** Transmit FIFO Threshold Level Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 0 entries, and a value of 255 sets the threshold for 255 entries.

14.2.16 REG IC_CLR_INTR (IC_CLR_INTR) - Offset 40h

Clear Combined and Individual Interrupt Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts. For an exception to clearing IC_TX_ABRT_SOURCE through Bit 9 of the IC_TX_ABRT_SOURCE register.

14.2.17 REG IC_CLR_RX_UNDER (IC_CLR_RX_UNDER) - Offset 44h

Clear RX_UNDER Interrupt Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 44h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

14.2.18 REG IC_CLR_RX_OVER (IC_CLR_RX_OVER) - Offset 48h

Clear RX_OVER Interrupt Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

14.2.19 REG IC_CLR_TX_OVER (IC_CLR_TX_OVER) - Offset 4Ch

Clear TX_OVER Interrupt Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

14.2.20 REG IC_CLR_RD_REQ (IC_CLR_RD_REQ) - Offset 50h

Clear RD_REQ Interrupt Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

14.2.21 REG IC_CLR_TX_ABRT (IC_CLR_TX_ABRT) - Offset 54h

Clear TX_ABRT Interrupt Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 54h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. For an exception to clearing IC_TX_ABRT_SOURCE through Bit 9 of the IC_TX_ABRT_SOURCE register.

14.2.22 REG IC_CLR_RX_DONE (IC_CLR_RX_DONE) - Offset 58h

Clear RX_DONE Interrupt Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

14.2.23 REG IC_CLR_ACTIVITY (IC_CLR_ACTIVITY) - Offset 5Ch

Clear ACTIVITY Interrupt Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

14.2.24 REG IC_CLR_STOP_DET (IC_CLR_STOP_DET) - Offset 60h

Clear STOP_DET Interrupt Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

14.2.25 REG IC_CLR_START_DET (IC_CLR_START_DET) - Offset 64h

Clear START_DET Interrupt Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

14.2.26 REG IC_CLR_GEN_CALL (IC_CLR_GEN_CALL) - Offset 68h

Clear GEN_CALL Interrupt Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

14.2.27 REG IC_ENABLE (IC_ENABLE) - Offset 6Ch

I2C Enable Register. The register IC_ENABLE_STATUS is added to allow software to unambiguously determine when the hardware has completely shutdown in response to the IC_ENABLE register being set from 1 to 0. Procedure to disable I2C:

1. Define a timer interval (ti2c_poll) equal to the 10 times the signaling period for the highest I2C transfer speed used in the system and supported by DW_apb_i2c. For example, if the highest I2C transfer mode is 400 kb/s, then this ti2c_poll is 25us.

2. Define a maximum time-out parameter, MAX_T_POLL_COUNT, such that if any repeated polling operation exceeds this maximum value, an error is reported.

3. Execute a blocking thread/process/function that prevents any further I2C master transactions to be a started by software, but allows any pending transfers to be completed. This is only needed for master mode.

4. The variable POLL_COUNT is initialized to zero.

5. Set IC_ENABLE to 0.

6. Read the IC_ENABLE_STATUS register and test the IC_EN bit (bit 0). Increment POLL_COUNT by one. If POLL_COUNT >= MAX_T_POLL_COUNT, exit with the relevant error code.

7. If IC_ENABLE_STATUS[0] is 1, then sleep for ti2c_poll and proceed to the previous step. Otherwise, exit with a relevant success code.

Abort control bit:

Will override every other command. It will produce a Stop condition, even if the IC_DATA_CMD[9] register is not set. Will not be set or enabled as the system comes out of reset.

Can be written at any time; however should not be written unless active transactions are taking place.

Applicable only when DW_apb_i2c is programmed to act as a master, i.e., IC_CON[0] == 1 or Master_mode == 1

Force Stop sequence:

IC_ENABLE register will have a bit USER_ABORT (which is a write-only bit). The user can set this bit only when eIC_ENABLE[0] is set. Otherwise, the controller will ignore the USER_ABORT bit.

In response to the USER_ABORT request, the controller will issue STOP and flush the Tx FIFO during the safe period as in:

Issues NACK+STOP when ABORT is seen in HOLD_RX_BYTE state OR

Issues STOP when ABORT is seen in HOLD_TX_BYTE state OR

Issues STOP after RX/TX completion when ABORT is not seen in HOLD_RX_BYTE / HOLD_TX_BYTE states.

Then the controller flushes the TX FIFO and sets the TX_ABORT interrupt after the abort operation.

In response to the TX_ABORT interrupt, the user must read the IC_TX_ABRT_SOURCE register to find out the cause for TX_ABORT (USER_ABORT will be an additional status bit) and then read the IC_CLR_TX_ABRT register to clear the interrupt.

The controller will latch the TXFLR value just before the Tx FIFO flush and outputs in the IC_CLR_ABRT register (Read only register).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**ABORT:** Software can abort I2C transfer by setting this bit. Hardware will clear this ABORT bit once the STOP has been detected.
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. 0: Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) 1: Enables DW_apb_i2c Software can disable DW_apb_i2c while it is active. However, it is important that care be taken to ensure that DW_apb_i2c is disabled properly. When DW_apb_i2c is disabled, the following occurs: The TX FIFO and RX FIFO get flushed. Status bits in the IC_INTR_STAT register are still active until DW_apb_i2c goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the DW_apb_i2c stops the current transfer at the end of the current byte and does not acknowledge the transfer.

14.2.28 REG IC_STATUS (IC_STATUS) - Offset 70h

I2C Status Register. This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt.

When the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register:

- Bits 1 and 2 are set to 1

- Bits 3 and 4 are set to 0

When the master or slave state machines goes to idle and IC_ENABLE=0:

- Bits 5 and 6 are set to 0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 70h	00000006h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6	0h RO	**SLV_ACTIVITY:** Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set. 0: Slave FSM is in IDLE state so the Slave part of DW_apb_i2c is not Active 1: Slave FSM is not in IDLE state so the Slave part of DW_apb_i2c is Active. Note: IC_STATUS[0] that is, ACTIVITY bit is the OR of SLV_ACTIVITY and MST_ACTIVITY bits.
5	0h RO	**MST_ACTIVITY:** Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set. 0: Master FSM is in IDLE state so the Master part of DW_apb_i2c is not Active 1: Master FSM is not in IDLE state so the Master part of DW_apb_i2c is Active Note: IC_STATUS[0] that is, ACTIVITY bit is the OR of SLV_ACTIVITY and MST_ACTIVITY bits
4	0h RO	**RFF:** Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty locations, this bit is cleared. 0: Receive FIFO is not full 1: Receive FIFO is full
3	0h RO	**RFNE:** Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. 0: Receive FIFO is empty 1: Receive FIFO is not empty
2	1h RO	**TFE:** Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty
1	1h RO	**TFNF:** Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. 0: Transmit FIFO is full 1: Transmit FIFO is not full
0	0h RO	**IC_STATUS_ACTIVITY:** I2C Activity Status

14.2.29 REG IC_TXFLR (IC_TXFLR) - Offset 74h

I2C Transmit FIFO Level Register. This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever:

- The I2C is disabled

- There is a transmit abort that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register

- The slave bulk transmit mode is aborted

The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 74h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO	**TXFLR:** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO

14.2.30 REG IC_RXFLR (IC_RXFLR) - Offset 78h

I2C Receive FIFO Level Register. This register contains the number of valid data entries in the receive FIFO buffer. It is cleared whenever:

- The I2C is disabled

- Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE

The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 78h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO	**RXFLR:** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

14.2.31 REG IC_SDA_HOLD (IC_SDA_HOLD) - Offset 7Ch

I2C SDA Hold Time Length Register. This register controls the amount of hold time on the SDA signal after a negative edge of SCL in both master and slave mode, in units of ic_clk period (10Mhz). The value programmed must be greater than the minimum hold time in each mode for the value to be implemented one cycle in master mode, seven cycles in slave mode. Writes to this register succeed only when IC_ENABLE=0.

The programmed SDA hold time cannot exceed at any time the duration of the low part of SCL. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the SCL period measured in ic_clk cycles.

The bits [15:0] of this register are used to control the hold time of SDA during transmit in both slave and master mode (after SCL goes from HIGH to LOW).

The bits [23:16] of this register are used to extend the SDA transition (if any) whenever SCL is HIGH in the receiver.

Writes to this register succeed only when IC_ENABLE[0]=0.

The values in this register are in units of ic_clk period. The value programmed in IC_SDA_TX_HOLD must be greater than the minimum hold time in each mode one cycle in master mode, seven cycles in slave mode for the value to be implemented.

The programmed SDA hold time during transmit (IC_SDA_TX_HOLD) cannot exceed at any time the duration of the low part of SCL. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7Ch	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW	**IC_SDA_RX_HOLD:** Sets the required SDA hold time in units of ic_clk period, when the I2C Host Controller acts as a receiver
15:0	0001h RW	**IC_SDA_TX_HOLD:** Sets the required SDA hold time in units of ic_clk period, when the I2C Host Controller acts as a transmitter

14.2.32 REG IC_TX_ABRT_SOURCE (IC_TX_ABRT_SOURCE) - Offset 80h

This register has 32 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]).

Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	000h RO	**TX_FLUSH_CNT:** This field preserves the TXFLR value prior to the last TX_ABRT event. It is cleared whenever I2C is disabled. Mode Applicable: Master-Transmitter
22:17	0h RO	**Reserved**
16	0h RO	**ABRT_USER_ABRT:** This is a master-mode-only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]) Mode Applicable: Master-Transmitter
15	0h RO	**ABRT_SLVRD_INTX:** 1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register. Mode Applicable: Slave Transmitter 14 RO 1'h0
14	0h RO	**ABRT_SLV_ARBLOST:** 1: Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time. Note: Even though the slave never owns the bus, something could go wrong on the bus. This is a fail safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then DW_apb_i2c no longer own the bus. Mode Applicable: Slave Transmitter
13	0h RO	**ABRT_SLVFLUSH_TXFIFO:** 1: Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO. Mode Applicable: Slave Transmitter
12	0h RO	**ARB_LOST:** 1: Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration. Mode Applicable: Master or Slave Transmitter
11	0h RO	**ABRT_MASTER_DIS:** 1: User tries to initiate a Master operation with the Master mode disabled. Mode Applicable: Master Transmitter or Receiver
10	0h RO	**ABRT_10B_RD_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode. Mode Applicable: Master Receiver
9	0h RO	**ABRT_SBYTE_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), OR the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets re-asserted. Mode Applicable: Master

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**ABRT_HS_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode. Mode Applicable: Master Transmitter or Receiver
7	0h RO	**ABRT_SBYTE_ACKDET:** 1: Master has sent a START Byte and the START Byte was acknowledged (wrong behavior). Mode Applicable: Master
6	0h RO	**ABRT_HS_ACKDET:** 1: Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior). Mode Applicable: Master
5	0h RO	**ABRT_GCALL_READ:** 1: DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1). Mode Applicable: Master Transmitter
4	0h RO	**ABRT_GCALL_NOACK:** 1: DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call. Mode Applicable: Master Transmitter
3	0h RO	**ABRT_TXDATA_NOACK:** 1: This is a master-mode only bit. Master has received an acknowledgment for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s). Mode Applicable: Master Transmitter
2	0h RO	**ABRT_10ADDR2_NOACK:** 1: Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave. Mode Applicable: Master Transmitter or Receiver
1	0h RO	**ABRT_10ADDR1_NOACK:** 1: Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave. Mode Applicable: Master Transmitter or Receiver
0	0h RO	**ABRT_7B_ADDR_NOACK:** 1: Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave. Mode Applicable: Master Transmitter or Receiver

14.2.33 REG IC_DMA_CR (IC_DMA_CR) - Offset 88h

DMA Control Register. This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the registers address has no effect and reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**TDMAE:** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel. 0 = Transmit DMA disabled 1 = Transmit DMA enabled
0	0h RW	**RDMAE:** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel. 0 = Receive DMA disabled 1 = Receive DMA enabled

14.2.34 REG IC_DMA_TDLR (IC_DMA_TDLR) - Offset 8Ch

DMA Transmit Data Level Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMATDL:** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

14.2.35 REG IC_DMA_RDLR (IC_DMA_RDLR) - Offset 90h

I2C Receive Data Level Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMARDL:** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

14.2.36 REG IC_SDA_SETUP (IC_SDA_SETUP) - Offset 94h

I2C SDA Setup Register. This register controls the amount of time delay (in terms of number of ic_clk clock periods 100Mhz) introduced in the rising edge of SCL relative to SDA changing by holding SCL low when DW_apb_i2c services a read request while operating as a slave-transmitter. The relevant I2C requirement is tSU:DAT (note 4) as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2.

Note: The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 94h	00000064h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	64h RW	**SDA_SETUP:** SDA Setup in terms of ic_clk cycles.

14.2.37 REG IC_ACK_GENERAL_CALL (IC_ACK_GENERAL_CALL) - Offset 98h

I2C ACK General Call Register. The register controls whether DW_apb_i2c responds with a ACK or NACK when it receives an I2C General Call address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 98h	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	1h RW	**ACK_GEN_CALL:** ACK General Call. When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts.

14.2.38 REG IC_ENABLE_STATUS (IC_ENABLE_STATUS) - Offset 9Ch

I2C Enable Status Register. The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE register is set from 1 to 0; that is, when DW_apb_i2c is disabled.

If IC_ENABLE has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.

If IC_ENABLE has been set to 0, bits 2:1 is only been valid as soon as bit 0 is read as 0.

When IC_ENABLE has been written with 0 a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RO	**SLV_RX_DATA_LOST:** This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0. When read as 1, DW_apb_i2c is deemed to have been actively engaged in an aborted I2C transfer (with matching address) and the data phase of the I2C transfer has been entered, even though a data byte has been responded with a NACK. NOTE: If the remote I2C master terminates the transfer with a STOP condition before the DW_apb_i2c has a chance to NACK a transfer, and IC_ENABLE has been set to 0, then this bit is also set to 1. When read as 0, DW_apb_i2c is deemed to have been disabled without being actively involved in the data phase of a Slave-Receiver transfer.
1	0h RO	**SLV_DISABLED_WHILE_BUSY:** This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0. This bit is set when the CPU writes a 0 to the IC_ENABLE register while: (a) DW_apb_i2c is receiving the address byte of the Slave-Transmitter operation from a remote master; OR, (b) address and data bytes of the Slave-Receiver operation from a remote master. When read as 1, DW_apb_i2c is deemed to have forced a NACK during any part of an I2C transfer, irrespective of whether the I2C address matches the slave address set in DW_apb_i2c (IC_SAR register) OR if the transfer is completed before IC_ENABLE is set to 0 but has not taken effect. When read as 0, DW_apb_i2c is deemed to have been disabled when there is master activity, or when the I2C bus is idle.
0	0h RO	**IC_EN:** ic_en Status. This bit always reflects the value driven on the output port ic_en. When read as 1, DW_apb_i2c is deemed to be in an enabled state. When read as 0, DW_apb_i2c is deemed completely inactive.

14.2.39 REG IC_FS_SPKLEN (IC_FS_SPKLEN) - Offset A0h

I2C SS and FS Spike Suppression Limit Register.

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS or FS modes. The relevant I2C requirement is tSP as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + A0h	00000007h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	07h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set.

14.2.40 REG RESETS (RESETS) - Offset 204h

Soft reset register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 204h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW	**RESET_DMA:** iDMA Software Reset Control 0 IP is in reset (Reset Asserted) 1 IP is NOT at reset (Reset Released)
1:0	0h RW	**RESET_IP:** reset_i2c (reset_i2c) I2C Host Controller reset. Used to reset the I2C Host Controller by SW control. All I2C Configuration State and Operational State will be forced to the Default state. There is no timing requirement (SW can assert and de-assert in back to back transactions). This reset does NOT impact the LPSS cluster level settings by BIOS, the PCI configuration header information, DMA channel configuration and interrupt assignment/mapping/etc. Driver should re-initialize registers related to Driver context following an I2C host controller reset. 00 = I2C Host Controller is in reset (Reset Asserted) 01 = Reserved 10 = Reserved 11 = I2C Host Controller is NOT at reset (Reset Released)

14.2.41 REG ACTIVELTR_VALUE (ACTIVELTR_VALUE) - Offset 210h

ACTIVELTR_VALUE

Type	Size	Offset	Default
MMIO	32 bit	BAR + 210h	00000800h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**SNOOP_REQUIRMENT:** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10 -bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	**Reserved**
12:10	2h RW	**I2C_SW_LTR_SNOOP_SCALE_REG_12_10:** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which don't match those values will be dropped completely, next read will return previous value.
9:0	000h RW	**SNOOP_VALUE:** 10-bit latency value

14.2.42 REG IDLELTR_VALUE (IDLELTR_VALUE) - Offset 214h

IDLELTR_VALUE

Type	Size	Offset	Default
MMIO	32 bit	BAR + 214h	00000800h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**SNOOP_REQUIRMENT:** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10 -bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time
14:13	0h RO	**Reserved**
12:10	2h RW	**SNOOP_LATENCY_SCALE:** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which don't match those values will be dropped completely, next read will return previous value.
9:0	000h RW	**SNOOP_VALUE:** SNOOP_VALUE, 10-bit latency value

14.2.43 REG TX_ACK_COUNT (TX_ACK_COUNT) - Offset 218h

TX_ACK_COUNT

Type	Size	Offset	Default
MMIO	32 bit	BAR + 218h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**TX_ACK_COUNT_OVERFLOW:** Count overflow indication; 0= count valid 1= count overflow/invalid
30:24	0h RO	**Reserved**
23:0	000000h RO	**TX_ACK_COUNT:** Count ACK seen on Write commands, 24-bit up-counter which counts the number of TX ACKs on the I2C bus. The Counter is forced to be cleared by software Read.

14.2.44 REG RX_BYTE_COUNT (RX_BYTE_COUNT) - Offset 21Ch

RX_ACK_COUNT

Type	Size	Offset	Default
MMIO	32 bit	BAR + 21Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**RX_ACK_COUNT_OVERFLOW:** count overflow indication; 0= count valid 1= count overflow/invalid
30:24	0h RO	**Reserved**
23:0	000000h RO	**RX_ACK_COUNT:** Counts ACK seen on Read commands, 24-bit readable (MMIO) up-counter which counts the number of RX bytes received on the I2C bus. The Counter is forced to be cleared by software Read

14.2.45 REG TX_COMPLETE_INTR_STAT (TX_COMPLETE_INTR_STAT) - Offset 220h

Interrupt status register for Tx Complete

Type	Size	Offset	Default
MMIO	32 bit	BAR + 220h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**TX_INTR_STAT_MASK:** I2C Tx completion interrupt mask, 0 = Unmask 1= Mask
0	0h RO	**TX_INTR_STAT:** I2C Tx completion interrupt status indication, 0 = Low 1 = High

14.2.46 REG TX_COMPLETE_INTR_CLR (TX_COMPLETE_INTR_CLR) - Offset 224h

I2C Tx complete interrupt clear indication

Type	Size	Offset	Default
MMIO	32 bit	BAR + 224h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO	**I2C_TX_COMPLETE_INTR_CLR_0:** I2C Tx completion interrupt clear indication

14.2.47 REG SW_SCRATCH_0 (SW_SCRATCH_0) - Offset 228h

SW Scratch Register 0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 228h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SW_SCRATCH_0:** SW scratch reg 0, Scratch Pad Register for SW to generated Local CMD or DATA for iDMA

14.2.48 REG SW_SCRATCH_1 (SW_SCRATCH_1) - Offset 22Ch

SW Scratch Register 1

Type	Size	Offset	Default
MMIO	32 bit	BAR + 22Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SW_SCRATCH_1:** SW scratch reg 1, Scratch Pad Register for SW to generated Local CMD or DATA for iDMA

14.2.49 REG SW_SCRATCH_2 (SW_SCRATCH_2) - Offset 230h

SW Scratch Register 2

Type	Size	Offset	Default
MMIO	32 bit	BAR + 230h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SW_SCRATCH_2:** SW scratch reg 2, Scratch Pad Register for SW to generated Local CMD or DATA for iDMA

14.2.50 REG SW_SCRATCH_3 (SW_SCRATCH_3) - Offset 234h

SW Scratch Register 3

Type	Size	Offset	Default
MMIO	32 bit	BAR + 234h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SW_SCRATCH_3:** SW scratch reg 3, Scratch Pad Register for SW to generated Local CMD or DATA for iDMA

14.2.51 REG CLOCK_GATE (CLOCK_GATE) - Offset 238h

CLOCK_GATE_Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 238h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:2	0h RW	**SW_DMA_CLK_CTL:** DMA clock gate control bits, iDMA Clock Control 00 = Dynamic Clock Gate Enable 01 = Reserved 10 = Force iDMA Clock off 11 = Force iDMA Clock on
1:0	0h RW	**SW_IP_CLK_CTL:** IP clock gate control bits, IP Clock Control 00 = Dynamic Clock Gate Enable 01 = Reserved 10 = Force IP Clocks off 11 = Force IP Clocks on

14.2.52 REG REMAP_ADDR_LO (REMAP_ADDR_LO) - Offset 240h

I2C Remap Address Lo Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 240h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**I2C_REMAP_ADDR_LO_REG:** Remap Address Low Must be programed to the same value as low 32 bits (0x 010 BAR Low) Note: Must be programed for all Slice configurations (iDMA or PIO only)

14.2.53 REG REMAP_ADDR_HI (REMAP_ADDR_HI) - Offset 244h

I2C Remap Address Hi Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 244h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**I2C_REMAP_ADDR_HI:** Remap Address High Must be programmed to the same value as low 32 bits (0x 014 BAR High)

14.2.54 REG DEVIDLE_CONTROL (DEVIDLE_CONTROL) - Offset 24Ch

I2C Dev Idle Control Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 24Ch	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**INTR_REQ_CAPABLE:** INTR_REQ_CAPABLE, Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0
3	1h RW/1C	**RESTORE_REQUIRED:** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up. Note: If SW is setting bit 3 together with any other bit of this register, only bit 3 is written; SW is required to do 2 writes in this case : bit 3 first and all other bits second. This (Restore Required) field of the D0i3C register needs to be preserved during the S0ix restore window even though the D0i3C register is being restored (during restore window, RR bit should be restored to 1
2	0h RW	**DEVIDLE:** DEVIDLE, SW sets this bit to 1 to move the function into the DevIdle state. Writing this bit to 0 will return the function to the fully active D0 state (D0i0)
1	0h NA	**INTR_REQ:** INTR_REQ, Reserved
0	0h RO	**CMD_IN_PROGRESS:** CMD_IN_PROGRESS, HW sets this bit on a 1->0 or 0->1 transition of DEVIDLE. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. HW clears this bit upon completing the DevIdle transition command. When clear, all the other bits in the register are valid and SW may write to any bit. If Interrupt Request (IR) was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect.

14.2.55 REG I2C_HVM_MISR_CRCOUT (I2C_HVM_MISR_CRCOUT) - Offset 280h

I2C HVM MISR CRCOUT

Type	Size	Offset	Default
MMIO	32 bit	BAR + 280h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	FFFFh RO	**I2C_HVM_MISR_CRCOUT:** I2C MISR Output for HVM

14.2.56 REG CAPABLITIES (CAPABLITIES) - Offset 2FCh

I2C Capabilities Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2FCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9	0h RO	**SERIAL_CLK_FREQ**
8	0h RO	**IDMA_PRESENT:** 0= DMA present 1= DMA not present
7:4	0h RO	**INSTANCE_TYPE:** I2C, SPI or UART, Instance Type: 0000 = IC2 0001 = UART 0010 = SPI 0011 1111 = Reserved
3:0	0h RO	**INSTANCE_NUMBER:** i2c0 - 000 i2c1 - 001 ... i2c5- 101

14.2.57 REG SAR_LO0 (SAR_LO0) - Offset 800h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer. Source Address Register for lower 32-bits for Channels 0-1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 800h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SAR_LO:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

14.2.58 REG SAR_HI0 (SAR_HI0) - Offset 804h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer. Source Address Register for upper 32-bits for Channels 0-1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 804h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SAR_HI:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

14.2.59 REG DAR_LO0 (DAR_LO0) - Offset 808h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer. Destination Address Register for Channels 0-1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 808h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DAR_LO:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

14.2.60 REG DAR_HI0 (DAR_HI0) - Offset 80Ch

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer. Destination Address Register for Upper 32-bits for Channels 0-1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 80Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DAR_HI:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

14.2.61 REG LLP_LO0 (LLP_LO0) - Offset 810h

You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled. The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. It shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists. The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 810h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**Reserved**

14.2.62 REG LLP_HI0 (LLP_HI0) - Offset 814h

You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled. The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. It shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists. The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 814h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.

14.2.63 REG CTL_LO0 (CTL_LO0) - Offset 818h

This register contains fields that control the DMA transfer. The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 818h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Reserved (00) Memory to Peripheral (01) Peripheral to Memory (10) Reserved (11) Flow Control is always assigned to the DMA.
19	0h RO	**Reserved**
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. Source BURST SIZE (in DW) = (2 ^ SRC_TR_WIDTH)
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**Reserved**
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE (IN DW) = (2^ MSIZE) (i.e. 2 to-the-power-of MSIZE) 1.Transferred Bytes Per Burst = BURST_SIZE * (2 ^ TR_WIDTH) Since Max Burst Length is limited by the OCP fabric to 16 DW, encodings 101 (32 DW), 110 (64 DW) and 111 (128 DW) are not supported by the fabric. 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
3:1	0h RW	**DST_TR_WIDTH:** BURST SIZE (in DW) = (2^ MSIZE) (i.e. 2 to-the-power-of MSIZE) Transferred Bytes Per Burst = BURST_SIZE * (2 ^ TR_WIDTH) Since Max Burst Length is limited by the South-Complex OCP fabric to 16 DW, encodings 101 (32 DW), 110 (64 DW) and 111 (128 DW) are not supported by the fabric. For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

14.2.64 REG CTL_HI0 (CTL_HI0) - Offset 81Ch

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled. If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 81Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.

Bit Range	Default & Access	Field Name (ID): Description
28:18	0h RO	**Reserved**
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	00000h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesn't mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register.

14.2.65 REG SSTAT0 (SSTAT0) - Offset 820h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 820h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

14.2.66 REG DSTAT0 (DSTAT0) - Offset 828h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI.

Note: This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information

should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 828h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

14.2.67 REG SSTATAR_LO0 (SSTATAR_LO0) - Offset 830h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 830h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTATAR_LO:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

14.2.68 REG SSTATAR_HI0 (SSTATAR_HI0) - Offset 834h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 834h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTATAR_HI:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block

14.2.69 REG DSTATAR_LO0 (DSTATAR_LO0) - Offset 838h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 838h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTATAR_LO:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

14.2.70 REG DSTATAR_HI0 (DSTATAR_HI0) - Offset 83Ch

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 83Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTATAR_HI:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

14.2.71 REG CFG_LO0 (CFG_LO0) - Offset 840h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 840h	00000203h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0h RO	**Reserved**
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length: 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE))
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length: 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE))
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17:11	0h RO	**Reserved**
10	0h RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit affects only when CH_SUSPEND is asserted
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**Reserved**
3	0h RW	**HSHAKE_NP_WR:** 0x1: Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0: Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1: Forces ALL writes to be Non-Posted on DMA Write Port 0x0: Non-Posted Writes will only be used at end of block transfers and in HW Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used
1	1h RW	**SRC_BURST_ALIGN:** 0x1: SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0: SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1: DST Burst Transfers are broken at a Burst Length aligned boundary 0x0: DST Burst Transfers are not broken at a Burst Length aligned boundary

14.2.72 REG CFG_HI0 (CFG_HI0) - Offset 844h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 844h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:18	000h RW	**WR_ISSUE_THD:** Write Issue Threshold. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
17:8	000h RW	**RD_ISSUE_THD:** Read Issue Threshold. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID: Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface.
3:0	0h RW	**SRC_PER:** Source Peripheral ID: Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface.

14.2.73 REG SGR0 (SGR0) - Offset 848h

The Source Gather register contains two fields: Source gathers count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gathers interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 848h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	00000h RW	**SGI:** Source gather interval.

14.2.74 REG DSR0 (DSR0) - Offset 850h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC). Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI). Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 850h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries
19:0	00000h RW	**DSI:** Destination scatter interval

14.2.75 REG RawTfr (RAWTFR) - Offset AC0h

Interrupt events are stored in this Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + AC0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**RAW:** Raw interrupt status for ch1 and ch0

14.2.76 REG RawBlock (RAWBLOCK) - Offset AC8h

RawBlock - Raw Status for Block Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + AC8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**RAW:** Raw interrupt status for ch 1 and ch0

14.2.77 REG RawSrcTran (RAWSRCTRAN) - Offset AD0h

RawSrcTran - Raw Status for Source Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + AD0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**RAW:** Raw interrupt status for ch1 and ch0

14.2.78 REG RawDstTran (RAWDSTTRAN) - Offset AD8h

RawDstTran - Raw Status for Destination Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + AD8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**RAW:** Raw interrupt status for ch1 and ch0

14.2.79 REG RawErr (RAWERR) - Offset AE0h

RawErr - Raw Status for Error Interrupts Register Error interrupt will be asserted by the DMA in the following cases:

IOSF Fabric returns an Unsuccessful Completion with UR Completion Status for a Non-Posted transaction issued by the DMA to Memory. This error occurs when an invalid address range is programed into the DMA SRC/Dest Field outside of the Host memory region on the memory side of the DMA transaction IOSF2OCP bridge will return error (triggering error interrupt from DMA) if the IOSF2OCP Bridge is programmed incorrectly.

Peripheral side transactions where invalid addressing can result in an OCP fabric error which will be translated into an Error Interrupt.

The SW should view this error as a serious programming error and handle it according to the specified error handling procedures for the product and OS.

Type	Size	Offset	Default
MMIO	32 bit	BAR + AE0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**RAW:** Raw interrupt status for ch1 and ch0

14.2.80 REG StatusTfr (STATUSTFR) - Offset AE8h

Status for Transfer Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + AE8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**STATUS:** Status for interrupt for ch1 and ch0

14.2.81 REG StatusBlock (STATUSBLOCK) - Offset AF0h

StatusBlock: Status for Block Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + AF0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**STATUS:** Status for interrupt for ch1 and ch0

14.2.82 REG StatusSrcTran (STATUSSRCTRAN) - Offset AF8h

StatusSrcTran: Status for Source Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + AF8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**STATUS:** Status for interrupt for ch1 and ch0

14.2.83 REG StatusDstTran (STATUSDSTTRAN) - Offset B00h

StatusDstTran: Status for Destination Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B00h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**STATUS:** Status for interrupt for ch 1 and ch0

14.2.84 REG StatusErr (STATUSERR) - Offset B08h

StatusErr: Status for Error Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B08h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**STATUS:** Status for interrupt for ch1 and ch0

14.2.85 REG MaskTfr (MASKTFR) - Offset B10h

Mask for Transfer Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	**Reserved**
1:0	0h RW	**INT_MASK:** Interrupt mask per ch1 and ch0. 0 - mask 1 - unmask

14.2.86 REG MaskBlock (MASKBLOCK) - Offset B18h

MaskBlock: Mask for Block Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	**Reserved**
1:0	0h RW	**INT_MASK:** Interrupt mask ch1 and ch0. 0 - mask 1 - unmask

14.2.87 REG MaskSrcTran (MASKSRCTRAN) - Offset B20h

Mask for Source Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	**Reserved**
1:0	0h RW	**INT_MASK:** Interrupt mask ch1 and ch0. 0 - mask 1 - unmask

14.2.88 REG MaskDstTran (MASKDSTTRAN) - Offset B28h

Mask for Destination Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B28h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	**Reserved**
1:0	0h RW	**INT_MASK:** Interrupt mask ch1 and ch0. 0 - mask 1 - unmask

14.2.89 REG MaskErr (MASKERR) - Offset B30h

Mask for Error Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	**Reserved**
1:0	0h RW	**INT_MASK:** Interrupt mask ch1 and ch0. 0 - mask 1 - unmask

14.2.90 REG ClearTfr (CLEARTFR) - Offset B38h

Clear for Transfer Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h WO	**CLEAR:** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

14.2.91 REG ClearBlock (CLEARBLOCK) - Offset B40h

Clear for Block Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h WO	**CLEAR:** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

14.2.92 REG ClearSrcTran (CLEARSRCTRAN) - Offset B48h

Clear for Source Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h WO	**CLEAR:** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

14.2.93 REG ClearDstTran (CLEARDSTTRAN) - Offset B50h

Clear for Destination Transaction Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + B50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h WO	**CLEAR:** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

14.2.94 REG ClearErr (CLEARERR) - Offset B58h

Clear for Error Interrupts Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h WO	**CLEAR:** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

14.2.95 REG StatusInt (STATUSINT) - Offset B60h

The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran, StatusErr is Ored to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**ERR:** OR of the contents of StatusErr register.
3	0h RO	**DSTT:** OR of the contents of StatusDst register.
2	0h RO	**SRCT:** OR of the contents of StatusSrcTran register
1	0h RO	**BLOCK:** OR of the contents of StatusBlock register.
0	0h RO	**TFR:** OR of the contents of StatusTfr register.

14.2.96 REG DmaCfgReg (DMACFGREG) - Offset B98h

This register is used to enable the DMA, which must be done before any channel activity can begin. If the global channel enable bit is cleared while any channel is still active, then DmaCfgReg.DMA_EN still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DmaCfgReg.DMA_EN bit returns 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**DMA_EN:** DMA Enable bit. 0 = DMA Disabled 1 = DMA Enabled

14.2.97 REG ChEnReg (CHENREG) - Offset BA0h

This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive, it can then enable an inactive channel with the required priority.

All bits of this register are cleared to 0 when the global DMA channel enable bit, DmaCfgReg(0), is 0. When the global channel enable bit is 0, then a write to the ChEnReg register is ignored and a read will always read back 0. The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel writes enable bit, ChEnReg.CH_EN_WE, is asserted on the same OCP write transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BA0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:8	0h WO	**CH_EN_WE:** Channel enable write enable.
7:2	0h RO	**Reserved**
1:0	0h RW	**CH_EN:** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

14.3 I²C PCR Registers Summary

Table 14-3. Summary of I²C PCR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
200h	4	PCICFGCTR1 PCI Configuration Control 1 Register (PCICFGCTR1)	00000100h
204h	4	PCICFGCTR2 PCI Configuration Control 2 Register (PCICFGCTR2)	00000100h
208h	4	PCICFGCTR3 PCI Configuration Control 3 Register (PCICFGCTR3)	00000100h
20Ch	4	PCICFGCTR4 PCI Configuration Control 4 Register (PCICFGCTR4)	00000100h
210h	4	PCICFGCTR5 PCI Configuration Control 5 Register (PCICFGCTR5)	00000100h
214h	4	PCICFGCTR6 PCI Configuration Control 6 Register (PCICFGCTR6)	00000100h
218h	4	PCICFGCTR7 PCI Configuration Control 7 Register (PCICFGCTR7)	00000100h
21Ch	4	PCICFGCTR8 PCI Configuration Control 8 Register (PCICFGCTR8)	00000100h

14.3.1 PCICFGCTR1 PCI Configuration Control 1 Register (PCICFGCTR1) - Offset 200h

Controls The PCI Configuration Space

Type	Size	Offset	Default
MMIO	32 bit	FDCD0000h + 200h	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**DIS_PCI_IDLE_CAP1:** This is a bit to disable the PCI Device Idle capability structure.
27:20	00h RW	**PCI_IRQ1:** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	00h RW	**ACPI_IRQ1:** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	1h RW	**IPIN1:** Interrupt Pin: This register indicates the values to be used for Global Interrupts.
7	0h RW	**BAR1_DISABLE1:** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	00h RW	**PME_SUPPORT1:** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI_INTR_EN1:** When set, the Bridge uses ACPI Sideband opcodes for messages When cleared, the Bridge uses global IOSF opcodes
0	0h RW	**PCI_CFG_DIS1:** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

14.3.2 PCICFGCTR2 PCI Configuration Control 2 Register (PCICFGCTR2) - Offset 204h

Controls the PCI configuration space

Type	Size	Offset	Default
MMIO	32 bit	FDCD0000h + 204h	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**DIS_PCI_IDLE_CAP2:** This is a bit to disable the PCI Device Idle capability structure.
27:20	00h RW	**PCI_IRQ2:** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	00h RW	**ACPI_IRQ2:** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	1h RW	**IPIN2:** Interrupt Pin: This register indicates the values to be used for Global Interrupts.
7	0h RW	**BAR1_DISABLE2:** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	00h RW	**PME_SUPPORT2:** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI_INTR_EN2:** When set, the Bridge uses ACPI Sideband opcodes for messages When cleared, the Bridge uses global IOSF opcodes
0	0h RW	**PCI_CFG_DIS2:** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

14.3.3 PCICFGCTR3 PCI Configuration Control 3 Register (PCICFGCTR3) - Offset 208h

Controls the PCI configuration space

Type	Size	Offset	Default
MMIO	32 bit	FDCD0000h + 208h	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Reserved**
27:20	00h RW	**PCI_IRQ3:** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	00h RW	**ACPI_IRQ3:** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	1h RW	**IPIN3:** Interrupt Pin: This register indicates the values to be used for Global Interrupts.
7	0h RW	**BAR1_DISABLE3:** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	00h RW	**PME_SUPPORT3:** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI_INTR_EN3:** When set, the Bridge uses ACPI Sideband opcodes for messages When cleared, the Bridge uses global IOSF opcodes
0	0h RW	**PCI_CFG_DIS3:** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

14.3.4 PCICFGCTR4 PCI Configuration Control 4 Register (PCICFGCTR4) - Offset 20Ch

Controls The PCI Configuration Space

Type	Size	Offset	Default
MMIO	32 bit	FDCD0000h + 20Ch	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Reserved**
27:20	00h RW	**PCI_IRQ4:** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	00h RW	**ACPI_IRQ4:** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	1h RW	**IPIN4:** Interrupt Pin: This register indicates the values to be used for Global Interrupts.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**BAR1_DISABLE4:** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	00h RW	**PME_SUPPORT4:** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI_INTR_EN4:** When set, the Bridge uses ACPI Sideband opcodes for messages When cleared, the Bridge uses global IOSF opcodes
0	0h RW	**PCI_CFG_DIS4:** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

14.3.5 PCICFGCTR5 PCI Configuration Control 5 Register (PCICFGCTR5) - Offset 210h

Controls the PCI configuration space

Type	Size	Offset	Default
MMIO	32 bit	FDCD0000h + 210h	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Reserved**
27:20	00h RW	**PCI_IRQ5:** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	00h RW	**ACPI_IRQ5:** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	1h RW	**IPIN5:** Interrupt Pin: This register indicates the values to be used for Global Interrupts.
7	0h RW	**BAR1_DISABLE5:** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	00h RW	**PME_SUPPORT5:** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI_INTR_EN5:** When set, the Bridge uses ACPI Sideband opcodes for messages When cleared, the Bridge uses global IOSF opcodes
0	0h RW	**PCI_CFG_DIS5:** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

14.3.6 PCICFGCTR6 PCI Configuration Control 6 Register (PCICFGCTR6) - Offset 214h

Controls the PCI configuration space

Type	Size	Offset	Default
MMIO	32 bit	FDCD0000h + 214h	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Reserved**
27:20	00h RW	**PCI_IRQ6:** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	00h RW	**ACPI_IRQ6:** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	1h RW	**IPIN6:** Interrupt Pin: This register indicates the values to be used for Global Interrupts.
7	0h RW	**BAR1_DISABLE6:** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	00h RW	**PME_SUPPORT6:** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI_INTR_EN6:** When set, the Bridge uses ACPI Sideband opcodes for messages When cleared, the Bridge uses global IOSF opcodes
0	0h RW	**PCI_CFG_DIS6:** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

14.3.7 PCICFGCTR7 PCI Configuration Control 7 Register (PCICFGCTR7) - Offset 218h

Controls The PCI Configuration Space

Type	Size	Offset	Default
MMIO	32 bit	FDCD0000h + 218h	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Reserved**
27:20	00h RW	**PCI_IRQ7:** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	00h RW	**ACPI_IRQ7:** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	1h RW	**IPIN7:** Interrupt Pin: This register indicates the values to be used for Global Interrupts.
7	0h RW	**BAR1_DISABLE7:** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	00h RW	**PME_SUPPORT7:** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI_INTR_EN7:** When set, the Bridge uses ACPI Sideband opcodes for messages When cleared, the Bridge uses global IOSF opcodes
0	0h RW	**PCI_CFG_DIS7:** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

14.3.8 PCICFGCTR8 PCI Configuration Control 8 Register (PCICFGCTR8) - Offset 21Ch

Controls The PCI Configuration Space

Type	Size	Offset	Default
MMIO	32 bit	FDCD0000h + 21Ch	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Reserved**
27:20	00h RW	**PCI_IRQ8:** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	00h RW	**ACPI_IRQ8:** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	1h RW	**IPIN8:** Interrupt Pin: This register indicates the values to be used for Global Interrupts.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**BAR1_DISABLE8:** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	00h RW	**PME_SUPPORT8:** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI_INTR_EN8:** When set, the Bridge uses ACPI Sideband opcodes for messages When cleared, the Bridge uses global IOSF opcodes
0	0h RW	**PCI_CFG_DIS8:** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

15 SATA Controller

15.1 SATA Configuration Registers Summary

This chapter records the registers in Bus: 0, Device 23, Function 0.

Table 15-1. Summary of Bus: 0, Device: 23, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	ID	4B608086h
4h	2	CMD	0000h
6h	2	Device Status (STS)	0210h
8h	1	Revision ID (RID)	00h
9h	1	Programming Interface (PI)	01h
Ah	2	Class Code (CC)	0106h
Ch	1	Cache Line Size (CLS)	00h
Dh	1	Master Latency Timer (MLT)	00h
Eh	1	Header Type (HTYPE)	00h
10h	4	MSI-X Table Base Address (MXTBA)	00000000h
14h	4	MSI-X Pending Bit Array Base Address (MXPBA)	00000000h
20h	4	AHCI Index Data Pair Base Address (AIDPBA)	00000001h
24h	4	AHCI Base Address (ABAR)	00000000h
2Ch	4	Sub System Identifiers (SS)	00000000h
34h	1	Capabilities Pointer (CAP)	80h
3Ch	2	Interrupt Information (INTR)	0100h
70h	2	PCI Power Management Capability ID (PID)	A801h
72h	2	PCI Power Management Capabilities (PC)	4003h
74h	2	PCI Power Management Control And Status (PMCS)	0008h
80h	2	Message Signalled Interrupt Identifier (MID)	7005h
82h	2	Message Signalled Interrupt Message Control (MC)	0000h
84h	4	Message Signalled Interrupt Message Address (MA)	00000000h
88h	2	Message Signalled Interrupt Message Data (MD)	0000h
90h	4	Port Mapping Register (MAP)	00000000h
94h	4	Port Control And Status (PCS)	00000000h
9Ch	4	SATA General Configuration (SATAGC)	00000000h
A0h	1	SATA Initialization Register Index (SIRI)	00h
A4h	4	SATA Initialization Register Data (SIRD)	00000000h
A8h	4	Serial ATA Capability Register 0 (SATACR0)	00100012h
ACh	4	Serial ATA Capability Register 1 (SATACR1)	00000048h
C0h	4	Scratch Pad (SP)	00000000h
D0h	2	MSI-X Identifiers (MXID)	0011h
D2h	2	MSI-X Message Control (MXC)	0000h
D4h	4	MSI-X Table Offset And Table BIR (MXT)	00000000h
D8h	4	MSI-X PBA Offset And PBA BIR (MXP)	00000001h
E0h	4	BIST FIS Control/Status (BFCS)	00000000h
E4h	4	BIST FIS Transmit Data 1 (BFTD1)	00000000h
E8h	4	BIST FIS Transmit Data 2 (BFTD2)	00000000h

15.1.1 ID - Offset 0h

When the MMIO RUN.RUNE=1, read access to this double-word is return with UR.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:23, F:0] + 0h	4B608086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4B60h RO	**Device ID (DID):** The specific value is dependent on config bits and fuses.
15:0	8086h RO	**Vendor ID (VID):** 16-bit field which indicates the company vendor as Intel.

15.1.2 CMD - Offset 4h

Command.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:23, F:0] + 4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts. This bit has no effect on MSI operation. When set, internal INTx# will not be generated. When cleared, internal INTx# are generated if there is an interrupt and MSI is not enabled.
9	0h RO	**Reserved**
8	0h RW	**SERR# Enable (SEE):** When set to 1, the HBA is allowed to generate SERR# on DPD or SATAGC.URD event that is enabled for SERR# generation. When cleared to 0, it is not.
7	0h RO	**Reserved**
6	0h RW	**Parity Error Response Enable (PEE):** When set, the SATA Controller will corrupt the outbound DATA FIS CRC if a forwarded data parity error is indicated.
5:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Bus Master Enable (BME):** Controls the SATA Controller's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transaction commands.
1	0h RW	**Memory Space Enable (MSE):** Controls access to the SATA Controller's target memory space (for AHCI). If Fabric Decoding scheme is used, this register bit is shadowed by the Fabric Decoder.
0	0h RW	**I/O Space Enable (IOSE):** Controls access to the SATA Controller's target I/O space. If Fabric Decoding scheme is used, this register bit is shadowed by the Fabric Decoder.

15.1.3 Device Status (STS) - Offset 6h

Device Status.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:23, F:0] + 6h	0210h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the SATA Controller detects a parity error on its interface.
14	0h RW/1C/V	**Signalled System Error (SSE):** Set when SATA Controller generates an SERR#.
13	0h RW/1C/V	**Received Master-Abort Status (RMA):** Set when the SATA Controller receives a master abort to a cycle it generated.
12	0h RW/1C/V	**Received Target-Abort Status (RTA):** Set when the SATA Controller receives a target abort to a cycle it generated.
11	0h RW/1C/V	**Signalled Target-Abort Status (STA):** This bit must be set by a target device whenever it terminates a transaction with Target-Abort. Devices that will never signal Target-Abort do not need to implement this bit.
10:9	1h RO	**DEVSEL# Timing Status (DEVT):** Controls the device select time for the SATA Controller's PCI interface.
8	0h RW/1C/V	**Master Data Parity Error Detected (DPD):** Set when the SATA Controller, as a master, either detects a parity error or sees the parity error line asserted, and the parity error response bit (bit 6 of the command register) is set. This bit can only be set on read completions received from the backbone where there is a parity error.
7:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	1h RO	**Capabilities List (CL):** Indicates the presence of a capabilities list. The minimum requirement for the capabilities list must be PCI power management for the SATA Controller.
3	0h RO/V	**Interrupt Status (IS):** Reflects the state of INTx# messages. This bit is set when the interrupt is to be asserted. This bit is a 0 after the interrupt is cleared (independent of the state of CMD.ID).
2:0	0h RO	**Reserved**

15.1.4 Revision ID (RID) - Offset 8h

Revision ID.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:23, F:0] + 8h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Revision ID (RID):** Indicates stepping of the host controller hardware.

15.1.5 Programming Interface (PI) - Offset 9h

Programming Interface.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:23, F:0] + 9h	01h

Bit Range	Default & Access	Field Name (ID): Description
7:0	01h RO	**IF:** If CC.SCC=06h(AHCI mode), it indicates that this is an AHCI HBA that has a major revision of 1 (as specified in the AHCI Version register). If CC.SCC=04h(RAID mode), it indicates that there is no programming interface(IF=00h). Internally, under this condition, the SATA controller is in native mode and its I/O spaces are only accessible through the I/O BARs.

15.1.6 Class Code (CC) - Offset Ah

Class Code.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:23, F:0] + Ah	0106h

Bit Range	Default & Access	Field Name (ID): Description
15:8	01h RO	**Base Class Code (BCC):** Indicates that this is a mass storage device.
7:0	06h RO	**Sub Class Code (SCC):** The value reported in this field is dependent on SATAGC.SMS and various fuses and configuration bits.

15.1.7 Cache Line Size (CLS) - Offset Ch

Cache Line Size.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:23, F:0] + Ch	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Cache Line Size (CLS):** This register has no meaning for the SATA controller.

15.1.8 Master Latency Timer (MLT) - Offset Dh

Master Latency Timer.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:23, F:0] + Dh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Master Latency Timer (MLT):** This register has no meaning for the SATA controller.

15.1.9 Header Type (HTYPE) - Offset Eh

Header Type.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:23, F:0] + Eh	00h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Multi-function Device (MFD):** 1 indicates this controller is part of a multi-function device. 0 indicates this controller is a single function device. The value of this bit depends on the wire strap istrap_c1_MultiFunctionDevice at the SATA Host Controller top level, driven by SoC.
6:0	00h RO	**Header Layout (HL):** Indicates that the controller uses a target device layout.

15.1.10 MSI-X Table Base Address (MXTBA) - Offset 10h

This BAR is used to allocate 32K, 16K or 8K Memory space for the MSI-X Table. The Memory space size is determined by BIOS by making bit-14 and bit-13 Read-Only '1' or Read-Write '0' based on SATAGC.MSS[1:0].

Note: If Fabric Decoding scheme is used, this register is shadowed by the Fabric Decoder.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:23, F:0] + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:15	00000h RW	**Base Address (BA):** Base address of memory space.
14	0h RW	**Base Address Bit 14 (BAB14):** When SATAGC.MSS[1:0]=00, this bit is Read Only '0' else it's Read Write '0'.
13	0h RW	**Base Address Bit 13 (BAB13):** When SATAGC.MSS[1:0]=00 or 01, this bit is Read Only '0' else it's Read Write '0'.
12:4	0h RO	**Reserved**
3	0h RO	**PF:** Indicates that this range is not pre-fetchable.
2:1	0h RO	**TP:** Indicates that this range can be mapped anywhere in 32-bit address space.
0	0h RO	**Resource Type Indicator (RTE):** Indicates a request for Memory space.

15.1.11 MSI-X Pending Bit Array Base Address (MXPBA) - Offset 14h

This BAR is used to allocate 256-byte Memory space for the MSI-X PBA. If Fabric Decoding scheme is used, this register is shadowed by the Fabric Decoder.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:23, F:0] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RW	**Base Address (BA):** Base address of memory space (aligned to 256B).
7:4	0h RO	**Reserved**
3	0h RO	**PF:** Indicates that this range is not pre-fetchable.
2:1	0h RO	**TP:** Indicates that this range can be mapped anywhere in 32-bit address space.
0	0h RO	**Resource Type Indicator (RTE):** Indicates a request for Memory space.

15.1.12 AHCI Index Data Pair Base Address (AIDPBA) - Offset 20h

This BAR is used to allocate I/O space for the AHCI index/data pair mechanism. If the Fabric Decoding scheme is used, this register is shadowed by the Fabric Decoder.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:23, F:0] + 20h	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:5	000h RW	**Base Address (BA):** Base address of the I/O space.
4:1	0h RO	**Reserved**
0	1h RO	**Resource Type Indicator (RTE):** Indicates a request for IO space.

15.1.13 AHCI Base Address (ABAR) - Offset 24h

This register represents a memory BAR allocating space for the AHCI memory registers. If the Fabric Decoding scheme is used, this register is shadowed by the Fabric Decoder. Note that Bit[31:16] of this register must be programmed to a value greater than 0 to ensure the memory is mapped to an address of 1 MBytes and greater (i.e. ABAR must be 00010000h or greater). Otherwise, memory cycle targeting the ABAR range may not be accepted. The Memory space size is determined by BIOS by making bit 15:11 Read-Only 1 or Read-Write 0 based on SATAGC.ASSEL[1:0].

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:23, F:0] + 24h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0000h RW	**Base Address (BA):** Base address of register memory space.
18	0h RW	**Base Address Bit 18 (BAB18):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 256K, this bit is Read Only '0' else it's Read Write '0'.
17	0h RW	**Base Address Bit 17 (BAB17):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 128K, this bit is Read Only '0' else it's Read Write '0'.
16	0h RW	**Base Address Bit 16 (BAB16):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 64K, this bit is Read Only '0' else it's Read Write '0'.
15	0h RW	**Base Address Bit 15 (BAB15):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 32K, this bit is Read Only '0' else it's Read Write '0'.
14	0h RW	**Base Address Bit 14 (BAB14):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 16K, this bit is Read Only '0' else it's Read Write '0'.
13:11	0h RW	**Base Address Bit 13-11 (BAB1311):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 2K, this bit is Read Only '0' else it's Read Write '0'.
10:4	0h RO	**Reserved**
3	0h RO	**PF:** Indicates that this range is not pre-fetchable
2:1	0h RO	**TP:** Indicates that this range can be mapped anywhere in 32-bit address space
0	0h RO	**Resource Type Indicator (RTE):** Indicates a request for register memory space.

15.1.14 Sub System Identifiers (SS) - Offset 2Ch

This register is initialized to logic 0 by the assertion of PLTRST#. This register can be written only once after PLTRST# de-assertion.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:23, F:0] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken on this value.
15:0	0000h RW/O	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action taken on this value.

15.1.15 Capabilities Pointer (CAP) - Offset 34h

Capabilities Pointer.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:23, F:0] + 34h	80h

Bit Range	Default & Access	Field Name (ID): Description
7:0	80h RW/L	**Capability Pointer (CP):** Indicates that the first capability pointer offset is offset 80h. Note: Refer to SATAGC.REGLOCK description in order to lock the register to become RO. This register is not reset by FLR. **Locked by:** SATAGC.REGLOCK

15.1.16 Interrupt Information (INTR) - Offset 3Ch

Interrupt Information.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:23, F:0] + 3Ch	0100h

Bit Range	Default & Access	Field Name (ID): Description
15:8	01h RW/O	**Interrupt Pin (IPIN):** This register tells which interrupt pin the device function uses. A value of 1 corresponds to INTA#. A value of 2 corresponds to INTB#. A value of 3 corresponds to INTC#. A value of 4 corresponds to INTD#. This register is not reset by FLR.
7:0	00h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register. Interrupt Line register is not reset by FLR.

15.1.17 PCI Power Management Capability ID (PID) - Offset 70h

PCI Power Management Capability ID.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:23, F:0] + 70h	A801h

Bit Range	Default & Access	Field Name (ID): Description
15:8	A8h RW/L	**Next Capability (NEXT):** A8h is location of the Serial ATA Capability structure. Note: Refer to SATAGC.REGLOCK description in order to lock the register to become RO. This register is not reset by FLR. **Locked by:** SATAGC.REGLOCK
7:0	01h RO	**Cap ID (CID):** Indicates that this pointer is a PCI power management capability.

15.1.18 PCI Power Management Capabilities (PC) - Offset 72h

PCI Power Management Capabilities.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:23, F:0] + 72h	4003h

Bit Range	Default & Access	Field Name (ID): Description
15:11	08h RO	**PME_SUPPORT:** The default value 01000 which indicates PME# can be generated from the D3HOT state in the SATA controller.
10	0h RO	**D2_SUPPORT:** The D2 state is not supported.
9	0h RO	**D1_SUPPORT:** The D1 state is not supported.
8:6	0h RO	**AUX_CURRENT:** PME# from D3COLD state is not supported, therefore this field is 000b.
5	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
4	0h RO	**Reserved**
3	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
2:0	3h RO	**VS:** Indicates support for Revision 1.2 of the PCI Power Management Specification.

15.1.19 PCI Power Management Control And Status (PMCS) - Offset 74h

PCI Power Management Control And Status.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:23, F:0] + 74h	0008h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**PME Status (PMES):** This bit is set when a PME event is to be requested, and if this bit is set and PMEE is set, a PME# will be generated. This register field is not reset by FLR.
14:9	0h RO	**Reserved**
8	0h RW	**PME Enable (PMEE):** When set, the SATA controller generates PME# from D3HOT on a wake event. ***Note:*** Software is advised to clear PMEE together with PMES prior to changing CC.SCC thru SATAGC.SMS. This register field is not reset by FLR.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset (NSFRST):** A 1 indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration context is preserved. Upon transition from the D3hot to the D0 state initialized state, no additional operating system intervention is required to preserve configuration context beyond writing to the PowerState bits. Regardless of this bit, the controller transition from D3hot to the D0 by a system or bus segment reset will return to the state D0 uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	**Reserved**
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the SATA Controller and to set a new power state. The values are: 00 = D0 state; 11 = D3HOT state. When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. If software attempts to write a 10 or 01 to these bits, the write will be ignored. If Fabric Decoding scheme is used, this register bit is shadowed by the Fabric Decoder.

15.1.20 Message Signalled Interrupt Identifier (MID) - Offset 80h

Message Signalled Interrupt Identifier.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:23, F:0] + 80h	7005h

Bit Range	Default & Access	Field Name (ID): Description
15:8	70h RW/L	**Next Pointer (NEXT):** Indicates the next item in the list is the PCI power management pointer. This is the recommended value. BIOS may program this field to A8h indicating that the next item is Serial ATA Capability structure. Note: Refer to SATAGC.REGLOCK description in order to lock the register to become RO. This register is not reset by FLR. **Locked by:** SATAGC.REGLOCK
7:0	05h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

15.1.21 Message Signalled Interrupt Message Control (MC) - Offset 82h

Message Signalled Interrupt Message Control.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:23, F:0] + 82h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7	0h RO	**64-Bit Address Capable (C64):** Capable of generating a 32-bit message only.
6:4	0h RO	**Multiple Message Enable (MME):** When this field is cleared to 000 (and MSIE is set), only a single MSI message will be generated for all SATA ports, and bits [15:0] of the message vector will be driven from MD[15:0].
3:1	0h RO	**Multiple Message Capable (MMC):** Not supported.
0	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. Note that CMD.ID bit has not effect on MSI. Software must clear this bit to 0 to disable MSI first before changing the number of messages allocated in the MMC field.

15.1.22 Message Signalled Interrupt Message Address (MA) - Offset 84h

Message Signalled Interrupt Message Address.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:23, F:0] + 84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**ADDR:** Lower 32 bits of the system specified message address, always DWORD aligned.
1:0	0h RO	**Reserved**

15.1.23 Message Signalled Interrupt Message Data (MD) - Offset 88h

Message Signalled Interrupt Message Data.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:23, F:0] + 88h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**DATA:** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word of the data bus of the MSI memory write transaction.

15.1.24 Port Mapping Register (MAP) - Offset 90h

Port Mapping Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:23, F:0] + 90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW/O	**SATA Port 7 Disable (SPD7):** Similar to SPD0 but for port 7. This bit is only applicable to project(s) that has port 7 physically.
22	0h RW/O	**SATA Port 6 Disable (SPD6):** Similar to SPD0 but for port 6. This bit is only applicable to project(s) that has port 6 physically.
21	0h RW/O	**SATA Port 5 Disable (SPD5):** Similar to SPD0 but for port 5. This bit is only applicable to project(s) that has port 5 physically.
20	0h RW/O	**SATA Port 4 Disable (SPD4):** Similar to SPD0 but for port 4. This bit is only applicable to project(s) that has port 4 physically.
19	0h RW/O	**SATA Port 3 Disable (SPD3):** Similar to SPD0 but for port 3. This bit is only applicable to project(s) that has port 3 physically.
18	0h RW/O	**SATA Port 2 Disable (SPD2):** Similar to SPD0 but for port 2. This bit is only applicable to project(s) that has port 2 physically.
17	0h RW/O	**SATA Port 1 Disable (SPD1):** Similar to SPD0 but for port 1. This bit is only applicable to project(s) that has port 1 physically.
16	0h RW/O	**SATA Port 0 Disable (SPD0):** A 1 prevents the SATA port from being enabled via config PCS.PxE. Write of 1 to PCS.PxE has no effect when the corresponding SPD[x] bit is 1. In preventing a port(s) from being enabled, BIOS shall first configure MAP.SPDx. And only then BIOS configures the PCS.PxE. This bit is only applicable to project(s) that has port 0 physically.
15:8	0h RO	**Reserved**
7:0	00h RW	**Port Clock Disable (PCD):** When any of these bits is set to 1, the backbone clock driven to the associated port logic is gated and will not toggle. When this bit is cleared to 0, all clocks to the associated port logic will operate normally. Assignment of the bits is: Bit 7: Port 7, this bit is applicable to projects that have port 7 physically; Bit 6: Port 6, this bit is only applicable to project(s) that has port 6 physically; Bit 5: Port 5, this bit is only applicable to project(s) that has port 5 physically; Bit 4: Port 4, this bit is only applicable to project(s) that has port 4 physically; Bit 3: Port 3, this bit is only applicable to project(s) that has port 3 physically; Bit 2: Port 2, this bit is only applicable to project(s) that has port 2 physically; Bit 1: Port 1, this bit is only applicable to project(s) that has port 1 physically; Bit 0: Port 0, this bit is only applicable to project(s) that has port 0 physically. Software cannot set the PCD[port x]=1 if the corresponding config PCS.PxE=1 or AHCI MMIO GHC.PI[x]=1. TM.PCD[x] statically gates clock into a SATA port hardware when set to 1. This renders the port non-functional.

15.1.25 Port Control And Status (PCS) - Offset 94h

By default, the SATA ports are set (by hardware) to the disabled state (e.g. bits[5:0] == '0') as a result of an initial power on reset. When enabled by software, the ports can transition between the on, partial, and slumber states and can detect devices. When disabled, the port is in the off state and cannot detect any devices.

Note: This register is not reset by FLR.

AHCI specific notes: If an AHCI-aware or RAID enabled operating system is being booted then system BIOS shall insure that all supported SATA ports are enabled prior to passing control to the OS. Once the AHCI aware OS is booted it becomes the enabling/disabling policy owner for the individual SATA ports. This is accomplished by manipulating a port's PxSCTL.DET and PxCMD.SUD fields. Because an AHCI or RAID aware OS will typically not have knowledge of the PxE bits and because the PxE bits act as master on/off switches for the ports, pre-boot software must insure that these bits are set to '1' prior to booting the OS, regardless as to whether or not a device is currently on the port.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:23, F:0] + 94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO/V	**Port 7 Present (P7P):** Same as P0P, except for port 7. This bit is only applicable to project(s) that has port 7 physically.
22	0h RO/V	**Port 6 Present (P6P):** Same as P0P, except for port 6. This bit is only applicable to project(s) that has port 6 physically.
21	0h RO/V	**Port 5 Present (P5P):** Same as P0P, except for port 5. This bit is only applicable to project(s) that has port 5 physically.
20	0h RO/V	**Port 4 Present (P4P):** Same as P0P, except for port 4. This bit is only applicable to project(s) that has port 4 physically.
19	0h RO/V	**Port 3 Present (P3P):** Same as P0P, except for port 3. This bit is only applicable to project(s) that has port 3 physically.
18	0h RO/V	**Port 2 Present (P2P):** Same as P0P, except for port 2. This bit is only applicable to project(s) that has port 2 physically.
17	0h RO/V	**Port 1 Present (P1P):** Same as P0P, except for port 1. This bit is only applicable to project(s) that has port 1 physically.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RO/V	**Port 0 Present (P0P):** This bit is set when COMINIT is received as a response to COMRESET. When set, the SATA controller has detected the presence of a device on port 0. It may change at any time. Clearing P0E bit leads to clearing of this bit after implementation delay. Software that intends to clear all PCS.PxE bits that are previously 1 to 0 and then to 1 again in two consecutive write cycles, software shall poll on this bit being 0 before setting P0E bit to 1. This bit is only applicable to project(s) that has port 0 physically.
15:8	0h RO	**Reserved**
7	0h RW/V	**Port 7 Enabled (P7E):** When MAP.SPD[7] is 1, this bit is reserved and is read-only 0. Otherwise this field is RW and the definition of this bit is same as P0E, except for port 7. This bit takes precedence over P7CMD.SUD. BIOS shall program the P7E to 1 prior to starting the AHCI initialization flow. RO-zero condition: MAP.SPD[7] is 1, OR SATA PORT muxing for port 7 based on fuses, soft straps and GPIO does not select SATA. This bit is only applicable to project(s) that has port 7 physically.
6	0h RW/V	**Port 6 Enabled (P6E):** When MAP.SPD[6] is 1, this bit is reserved and is read-only 0. Otherwise this field is RW and the definition of this bit is the same as P0E, except for port 6. This bit takes precedence over P6CMD.SUD. BIOS shall program the P6E to 1 prior to starting the AHCI initialization flow. RO-zero condition: MAP.SPD[6] is 1, OR SATA PORT muxing for port 6 based on fuses, soft straps and GPIO does not select SATA. This bit is only applicable to project(s) that have port 6 physically.
5	0h RW/V	**Port 5 Enabled (P5E):** When MAP.SPD[5] is 1, this bit is reserved and is read-only 0. Otherwise this field is RW and the definition of this bit is the same as P0E, except for port 5. This bit takes precedence over P5CMD.SUD. BIOS shall program the P5E to 1 prior to starting the AHCI initialization flow. RO-zero condition: MAP.SPD[5] is 1, OR SATA PORT muxing for port 5 based on fuses, soft straps and GPIO does not select SATA. This bit is only applicable to project(s) that has port 5 physically.
4	0h RW/V	**Port 4 Enabled (P4E):** When MAP.SPD[4] is 1, this bit is reserved and is read-only 0. Otherwise this bit is RW and same as P0E but for port 4 and takes precedence over P4CMD.SUD. BIOS shall program the P4E to 1 prior to starting the AHCI initialization flow. RO-zero condition: MAP.SPD[4] is 1, OR SATA PORT muxing for port 4 based on fuses, soft straps and GPIO does not select SATA. This bit is only applicable to project(s) that has port 4 physically.
3	0h RW/V	**Port 3 Enabled (P3E):** When MAP.SPD[3] is 1, this bit is reserved and is read-only 0. Otherwise this bit is RW and same as P0E but for port 3 and takes precedence over P3CMD.SUD. BIOS shall program the P3E to 1 prior to starting the AHCI initialization flow. RO-zero condition: MAP.SPD[3] is 1, OR SATA PORT muxing for port 3 based on fuses, soft straps and GPIO does not select SATA, OR Fuse FFSATA7 (disable port 2 & 3) is 1, OR Fuse FFSATA8 (disable port 1 & 3) is 1. This bit is only applicable to project(s) that has port 3 physically.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/V	**Port 2 Enabled (P2E):** When MAP.SPD[2] is 1, this bit is reserved and is read-only 0. Otherwise this bit is RW and same as P0E but for port 2 and takes precedence over P2CMD.SUD. . BIOS shall program the P2E to 1 prior to starting the AHCI initialization flow. RO-zero condition: MAP.SPD[2] is 1, OR SATA PORT muxing for port 2 based on fuses, soft straps and GPIO does not select SATA, OR Fuse FFSATA7 (disable port 2 & 3) is 1. This bit is only applicable to project(s) that has port 2 physically.
1	0h RW/V	**Port 1 Enabled (P1E):** When MAP.SPD[1] is 1, this bit is reserved and read-only 0. Otherwise this bit is RW and same as P0E but for port 1 and takes precedence over P1CMD.SUD. BIOS shall program the P1E to 1 prior to starting the AHCI initialization flow. RO-zero condition: MAP.SPD[1] is 1, OR SATA PORT muxing for port 1 based on fuses, soft straps and GPIO does not select SATA, OR Fuse FFSATA8 (disable port 1 & 3) is 1. This bit is only applicable to project(s) that has port 1 physically.
0	0h RW/V	**Port 0 Enabled (P0E):** When MAP.SPD[0] is 1, this bit is reserved and read-only 0. When set, the port is enabled. When cleared, the port is disabled. When enabled, the port can transition between the on, partial, and slumber states and can detect devices. When disabled, the port is in the off state and cannot detect any devices. This bit takes precedence over P0CMD.SUD. BIOS shall program the P0E to 1 prior to starting the AHCI initialization flow. RO-zero condition: MAP.SPD[0] is 1, OR SATA PORT muxing for port 0 based on fuses, soft straps and GPIO does not select SATA. The recommendation for software code that intends to clear all PCS.PxE bits that are previously 1 to 0 and then to 1 again immediately as in the polling requirement from P0P register bit. At any time that BIOS or software is clearing PCS.PxE from 1 to 0, due to time needed for port staggering hardware process (up to 8 ports) to complete, BIOS and software shall delay the write to set the TM.PCD register by 1.4us. This bit is only applicable to project(s) that has port 0 physically.

15.1.26 SATA General Configuration (SATAGC) - Offset 9Ch

SATA General Configuration.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:23, F:0] + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/O	**Register Lock (REGLOCK):** BIOS can set this bit to 1 to lock the following registers with RW/L attribute: CAP, CP, MID.NEXT, PIE.NEXT, SATACR0.NEXT. BIOS is required to program this field to 1 prior to handle off to OS. If BIOS needs the SATA host controller to change operation a few times (i.e. changing CC.SCC mode) and need different capability structures for each specific operation mode, BIOS needs not activate the lock until BIOS is ready to hand off to OS. BIOS may need to separate write access to this byte offset (x9Fh) from write to the lower 3-byte of the dword (x9C-9Eh) if there is a need to program the lower 3-byte dword location early during boot process. This field is not reset by FLR.
30:18	0h RO	**Reserved**
17	0h RW	**Do_Serr Disable (DOSERRD):** When 1, SERR reporting is disabled (DO_SERR Sideband message sending is disabled or SERR# Wire is suppressed. STS.SSE setting is not governed by this policy bit). When 0, SERR reporting is enabled (DO_SERR Sideband message sending is enabled or SERR# Wire is not suppressed). This register field is not reset by FLR.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**SATA Mode Select (SMS):** Software (SW) programs these bits to control the mode in which the SATA HBA should operate: 0b = AHCI mode; **Note:** SW shall not manipulate SATAGC.SMS during runtime operation; i.e. the OS will not do this.
15	0h RW	**Data Phase Parity Error Enable (DPPEE):** When 1, IOSF data phase parity error handling is enabled. When 0, the data phase parity error handling is disabled. This register field is not reset by FLR.
14:12	0h RW	**Write Request_Size Select/Max_Payload_Size (WRRSELMPS):** These two bits select the max write request size that SATA host controller will initiate for DMA write to memory. SATA host controller will internally break up larger write request based on these bits. The request is address-aligned to the selected size. Defined encodings for this field are: 000b = 128 address aligned bytes max payload size; 111b = 64 address aligned bytes max payload size. All other values are reserved for SATA host controller. This field is not reset by FLR.
11	0h RW	**Command Parity Error Enable (CPEE):** When 1, command parity error handing is enabled. When 0, the command parity error handling is disabled. This field is not reset by FLR.
10	0h RW	**SATA Controller Function Disable (SCFD):** BIOS program this bit to 1 to disable the SATA Controller function. When 0, SATA Controller function is enabled. When disable, SATA Host Controller will not claimed the register access targeting its Configuration Space. In IOSF primary Fabric Decode scheme, it's expected BIOS also program the corresponding bit used by the Fabric Decoder accordingly hence both SATA SIP and Fabric Decoder are in sync, and BIOS need to program this bit before programming the one in Fabric Decoder. Once this bit is set, BIOS is not able to revert it back to Function Enable until next round of platform reset. This register field is not reset by FLR.
9	0h RW	**Unsupported Request Reporting Enable (URRE):** If set to 1 by software, it allows reporting of an Unsupported Request as a system error. If both URRE and PCI configuration SERR# Enable registers are set to a 1, then the agent must set the Signaled System Error bit in the PCI Status register and send a DO_SERR message in IOSF-SB interface.
8	0h RW/1C/V	**Unsupported Request Detected (URD):** Set to 1 by hardware upon detecting an Unsupported Request on IOSF Primary interface that is not considered Advisory Non-Fatal. Cleared to 0 by SW. URD bit is only set based on IOSF primary bus interface activity. It is not set based on IOSF sideband bus interface activity.
7	0h RW/O	**Alternate ID Enable (AIE):** When programmed to 0, HW will report the following DID value to load the Window_InBox_Driver. When programmed to a 1, SATA Host Controller will not report the DID value to load the Windows_InBox_Driver. Programming this bit to a 1 will prevent the Windows in-box version of the Intel AHCI driver from loading on the platform - will require that the user perform an 'F6' installation of the Intel driver that is appropriate for the reported DID. This field is applicable when the AHCI is configured for RAID mode of operation. It has no impact for AHCI and IDE modes of operation. ***Note:*** BIOS is recommended to program this bit prior to programming the SATAGC.SMS field to reflect RAID. This field is reset by PLTRST# and BIOS is required to reprogram the value (either 0 or 1) after resuming from S3, S4 or S5. This insures that the value is properly and cannot be changed during runtime. This field is not reset by FLR.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/O/V	**AIE0 DevID Selection (DEVIDSEL):** This register allows BIOS to select Device ID when AIE=0 and Server Feature (SATA AIE DEVIDSEL) Disable Fuse =0. This bit only has effect in Desktop SKU. In Mobile SKU this bit has no effect at all. Check with config register offset 09h PI for usage. Server BIOS is required to program this field to 1 together with the write to the AIE bit in a single configuration write cycle. Client BIOS is required to program this bit to 0 together with the write to the AIE bit in a single configuration write cycle. When Server Feature (SATA AIE DEVIDSEL) Disable Fuse is programmed to 1, this disables the write-ability of this DEVIDSEL register bit, and becomes RO with a value of 0. This field is not reset by FLR.
5	0h RW/O	**FLR Capability Selection (FLRCSSEL):** This allows the FLR Capability to be bypassed. Check with config offset B0h. BIOS is required to program this bit to 1 and config offset A8h SATACR0.NEXT to 00h. This field is not reset by FLR.
4:3	0h RW/O	**MXTBA Size Select (MSS):** These 2 bits select the size of the Memory space for the MSI-X Table defined in BAR 0 (Configuration space offset 10h). MSI-X Table Memory space size is 32k when MSS[1:0]=00, 16k when MSS[1:0]=01, 8k when MSS[1:0]=10. This field is not reset by FLR.
2:0	0h RW/O	**ABAR Size Select (ASSEL):** These 3 bits select the size of the Memory space for the ABAR in BAR 5 (Configuration space offset 24h). ABAR Memory space size is 2k when ASSEL[2:0]=000, 16k when ASSEL[2:0]=001, 32k when ASSEL[2:0]=010, 64k when ASSEL[2:0]=011, 128k when ASSEL[2:0]=100, 256k when ASSEL[2:0]=101, 512k when ASSEL[2:0]=110. This field is not reset by FLR.

15.1.27 SATA Initialization Register Index (SIRI) - Offset A0h

SATA Initialization Register Index.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:23, F:0] + A0h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:2	00h RW	**IDX:** 6-bit index pointer into the 256-byte space. Data is written into the SIRD (DFTD) register and read from the SIRD register. This point to a DWord register. The byte enables on the SIRD register affect what will be written.
1:0	0h RO	**Reserved**

15.1.28 SATA Initialization Register Data (SIRD) - Offset A4h

SATA Initialization Register Data.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:23, F:0] + A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**DTA:** 32-bit data value that is written to the register pointed to by SIRI, or read from the register pointed to by SIRI.

15.1.29 Serial ATA Capability Register 0 (SATACR0) - Offset A8h

The SATACR0.NEXT is not changed from RO to become RWO because there is an existing method (SATAGC.FLRCSSEL bit) to bypass the FLR Capability structure, and since the FLR Capability ID.NEXT is already indicating end of capability structure, it does not need change to be RWO.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:23, F:0] + A8h	00100012h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	1h RO	**Major Revision (MAJREV):** Major revision number of the SATA Capability Pointer implemented.
19:16	0h RO	**Minor Revision (MINREV):** Minor revision number of the SATA Capability Pointer implemented.
15:8	00h RW/L	**Next Capability Pointer (NEXT):** 00h indicating the final item in the Capability List. Note: Refer to SATAGC.REGLOCK description in order to lock the register to become RO. This register is not reset by FLR. **Locked by:** SATAGC.REGLOCK
7:0	12h RO	**Capability ID (CAP):** The value of 12h has been assigned by the PCI SIG to designate the SATA Capability pointer.

15.1.30 Serial ATA Capability Register 1 (SATACR1) - Offset ACh

Serial ATA Capability Register 1.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:23, F:0] + ACh	00000048h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:4	004h RO	**BAR Offset (BAROFST):** Indicates the offset into the BAR where the AHCI Index/Data pair is located (in Dword granularity). The Index and Data I/O registers are located at offset 10h within the I/O space defined by AIDPBA(BAR4). A value of 004h indicates offset 10h. 000h = 0h offset; 001h = 4h offset; 002h = 8h offset; 003h = Ch offset; 004h = 10h offset; ...; FFFh = 3FFFh offset (max 16 KB)
3:0	8h RO	**BAR Location (BARLOC):** Indicates the absolute PCI Configuration Register address of the BAR containing the Index/Data pair (in Dword granularity). The Index and Data I/O registers reside within the space defined by AIDPBA(BAR4) in the SATA controller. A value of 8h indicates offset 20h, which is AIDPBA (BAR4). 0000 - 0011b = reserved; 0100b = 10h => BAR0; 0101b = 14h => BAR1; 0110b = 18h => BAR2; 0111b = 1Ch => BAR3; 1000b = 20h => AIDPBA; 1001b = 24h => BAR5; 1010 - 1110b = reserved; 1111b = Index/Data pair in PCI Configuration space which is not supported in SATA Host Controller.

15.1.31 Scratch Pad (SP) - Offset C0h

Scratch Pad.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:23, F:0] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DT:** This is a read/write register that is available for software to use. No hardware action is taken on this register.

15.1.32 MSI-X Identifiers (MXID) - Offset D0h

MSI-X Identifiers.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:23, F:0] + D0h	0011h

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RW/L	**Next Pointer (NEXT):** Indicates the next item in the list. This may be other capability pointers or it may be the last item in the list. Note: Refer to SATAGC.REGLOCK description in order to lock the register to become RO. This register is not reset by FLR. **Locked by:** SATAGC.REGLOCK
7:0	11h RO	**Capability ID (CID):** Capabilities ID indicates this is an MSI-X capability.

15.1.33 MSI-X Message Control (MXC) - Offset D2h

MSI-X Message Control.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:23, F:0] + D2h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**MSI-X Enable (MXE):** If set to '1' and the MSI Enable bit in the MSI Message Control register is cleared to '0', the function is permitted to use MSI-X to request service and is prohibited from using its INTx# pin (if implemented). If cleared to '0', the function is prohibited from using MSI-X to request service.
14	0h RW	**Function Mask (FM):** If set to '1', all of the vectors associated with the function are masked, regardless of their per vector Mask bit states. If cleared to '0', each vector's Mask bit determines whether the vector is masked or not. Setting or clearing the MSI-X Function Mask bit has no effect on the state of the per vector Mask bits.
13:11	0h RO	**Reserved**
10:0	000h RO	**Table Size (TS):** This value indicates the size of the MSI-X Table as the value n, which is encoded as n - 1. For example, a returned value of 3h corresponds to a table size of 4.

15.1.34 MSI-X Table Offset And Table BIR (MXT) - Offset D4h

MSI-X Table Offset And Table BIR.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:23, F:0] + D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW/O	**Table Offset (TO):** Used as an offset from the address contained by one of the function's Base Addresses registers to point to the base of the MSI-X Table. The lower three Table BIR bits are masked off (cleared to 000b) by system software to form a 32-bit Qword-aligned offset.
2:0	0h RO	**Table BIR (TBIR):** This field indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, is used to map the function's MSI-X Table into system memory. A read-only value of '0' means 10h.

15.1.35 MSI-X PBA Offset And PBA BIR (MXP) - Offset D8h

MSI-X PBA Offset And PBA BIR.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:23, F:0] + D8h	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW/O	**PBA Offset (PBAO):** Used as an offset from the address contained by one of the function's Base Addresses registers to point to the base of the MSI-X PBA. The lower three PBA BIR bits are masked off (cleared to 000b) by software to form a 32-bit Qword-aligned offset.
2:0	1h RO	**PBA BIR (PBIR):** This field indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, is used to map the function's MSI-X PBA into system memory. A read-only value of '1' means 14h.

15.1.36 BIST FIS Control/Status (BFCS) - Offset E0h

BIST FIS Control/Status.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:23, F:0] + E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RW	**Port 7 BIST FIS Initiate (P7BFI):** When a rising edge is detected on this bit, the SATA controller will initiate a BIST FIS to the device on port 7, using the parameters specified in this register and BFTD1 and BFTD2. The BIST FIS will only be initiated if a device is present and not in the partial or slumber states. After a BIST FIS is successfully completed, software must disable and re-enable the PCS.P7E prior to attempting additional BIST FISes or to return the SATA controller to a normal operational mode. If the BIST FIS fails, as indicated by BFF in this register, software can clear and then set this bit to initiate another BIST FIS. This bit is only applicable to project(s) that has port 7 physically.
16	0h RW	**Port 6 BIST FIS Initiate (P6BFI):** When a rising edge is detected on this bit, the SATA controller will initiate a BIST FIS to the device on port 6, using the parameters specified in this register and BFTD1 and BFTD2. The BIST FIS will only be initiated if a device is present and not in the partial or slumber states. After a BIST FIS is successfully completed, software must disable and re-enable the PCS.P6E prior to attempting additional BIST FISes or to return the SATA controller to a normal operational mode. If the BIST FIS fails, as indicated by BFF in this register, software can clear and then set this bit to initiate another BIST FIS. This bit is only applicable to project(s) that has port 6 physically.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Port 5 BIST FIS Initiate (P5BFI):** When a rising edge is detected on this bit, the SATA controller will initiate a BIST FIS to the device on port 5, using the parameters specified in this register and BFTD1 and BFTD2. The BIST FIS will only be initiated if a device is present and not in the partial or slumber states. After a BIST FIS is successfully completed, software must disable and re-enable the PCS.P5E prior to attempting additional BIST FISes or to return the SATA controller to a normal operational mode. If the BIST FIS fails, as indicated by BFF in this register, software can clear and then set this bit to initiate another BIST FIS. This bit is only applicable to project(s) that has port 5 physically.
14	0h RW	**Port 4 BIST FIS Initiate (P4BFI):** When a rising edge is detected on this bit, the SATA controller will initiate a BIST FIS to the device on port 4, using the parameters specified in this register and BFTD1 and BFTD2. The BIST FIS will only be initiated if a device is present and not in the partial or slumber states. After a BIST FIS is successfully completed, software must disable and re-enable PCS.P4E prior to attempting additional BIST FISes or to return the SATA controller to a normal operational mode. If the BIST FIS fails, as indicated by BFF in this register, software can clear and then set this bit to initiate another BIST FIS. This bit is only applicable to project(s) that has port 4 physically.
13	0h RW	**Port 3 BIST FIS Initiate (P3BFI):** When a rising edge is detected on this bit, the SATA controller will initiate a BIST FIS to the device on port 3, using the parameters specified in this register and BFTD1 and BFTD2. The BIST FIS will only be initiated if a device is present and not in the partial or slumber states. After a BIST FIS is successfully completed, software must disable and re-enable the PCS.P3E prior to attempting additional BIST FISes or to return the SATA controller to a normal operational mode. If the BIST FIS fails, as indicated by BFF in this register, software can clear and then set this bit to initiate another BIST FIS. This bit is only applicable to project(s) that has port 3 physically.
12	0h RW	**Port 2 BIST FIS Initiate (P2BFI):** When a rising edge is detected on this bit, the SATA controller will initiate a BIST FIS to the device on port 2, using the parameters specified in this register and BFTD1 and BFTD2. The BIST FIS will only be initiated if a device is present and not in the partial or slumber states. After a BIST FIS is successfully completed, software must disable and re-enable PCS.P2E prior to attempting additional BIST FISes or to return the SATA controller to a normal operational mode. If the BIST FIS fails, as indicated by BFF in this register, software can clear and then set this bit to initiate another BIST FIS. This bit is only applicable to project(s) that has port 2 physically.
11	0h RW/1C/V	**BIST FIS Successful (BFS):** This bit is set anytime a BIST FIS transmitted by the SATA controller receives an R_OK completion status from the device.
10	0h RW/1C/V	**BIST FIS Failed (BFF):** This bit is set anytime that a BIST FIS transmitted by the SATA controller receives an R_ERR completion status from the device.
9	0h RW	**Port 1 BIST FIS Initiate (P1BFI):** When a rising edge is detected on this bit, the SATA controller will initiate a BIST FIS to the device on port 1, using the parameters specified in this register and BFTD1 and BFTD2. The BIST FIS will only be initiated if a device is present and not in the partial or slumber states. After a BIST FIS is successfully completed, software must disable and re-enable PCS.P1E prior to attempting additional BIST FISes or to return the SATA controller to a normal operational mode. If the BIST FIS fails, as indicated by BFF in this register, software can clear and then set this bit to initiate another BIST FIS. This bit is only applicable to project(s) that has port 1 physically.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Port 0 BIST FIS Initiate (P0BFI):** When a rising edge is detected on this bit, the SATA controller will initiate a BIST FIS to the device on port 0, using the parameters specified in this register and BFTD1 and BFTD2. The BIST FIS will only be initiated if a device is present and not in the partial or slumber states. After a BIST FIS is successfully completed, software must disable and re-enable PCS.P0E prior to attempting additional BIST FISes or to return the SATA controller to a normal operational mode. If the BIST FIS fails, as indicated by BFF in this register, software can clear and then set this bit to initiate another BIST FIS. This bit is only applicable to project(s) that has port 0 physically.
7:2	00h RW	**BIST FIS Parameters (BFP):** These bits form the contents of the upper 6 bits of the BIST FIS Pattern Definition in the BIST FIS transmitted by the SATA controller. This field is not port specific - its contents will be used for any BIST FIS initiated on the SATA controller. The specific bit definitions are: Bit 7 (T) Far End Transmit mode; bit 6 (A) Align Bypass mode; bit 5 (S) Bypass Scrambling; bit 4 (L) Far End Retimed Loopback; bit 3 (F) Far End Analog Loopback; bit 2 (P) Primitive bit for use with Transmit mode.
1:0	0h RO	**Reserved**

15.1.37 BIST FIS Transmit Data 1 (BFTD1) - Offset E4h

BIST FIS Transmit Data 1.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:23, F:0] + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DATA:** The data programmed into this register will form the contents of the second DW of any BIST FIS initiated by the SATA controller. This register is not port specific - its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWs of the BIST FIS are only meaningful when the T bit of the BIST FIS is set to indicate Far-End Transmit mode, this register's contents will be transmitted as the BIST FIS 2nd DW regardless of whether or not the T bit is indicated in the BFCS register.

15.1.38 BIST FIS Transmit Data 2 (BFTD2) - Offset E8h

BIST FIS Transmit Data 2.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:23, F:0] + E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DATA:** The data programmed into this register will form the contents of the third DW of any BIST FIS initiated by the SATA controller. This register is not port specific - its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWs of the BIST FIS are only meaningful when the T bit of the BIST FIS is set to indicate Far-End Transmit mode, this register's contents will be transmitted as the BIST FIS 3rd DW regardless of whether or not the T bit is set in the BFCS register.

15.2 SATA ABAR Register Summary

This chapter records SATA ABAR Register.

Base address for this register is defined in SATA PCI register in Bus:0, Device:23 Function:0.

The offset value for this register: 24h

Table 15-2. Summary of SATA ABAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	HBA Capabilities (GHC_CAP)	FF36FF07h
4h	4	Global HBA Control (GHC)	80000000h
8h	4	Interrupt Status Register (IS)	00000000h
Ch	4	Ports Implemented (GHC_PI)	00000000h
10h	4	AHCI Version (VS)	00010301h
1Ch	4	Enclosure Management Location (EM_LOC)	01600002h
20h	4	Enclosure Management Control (EM_CTL)	07010000h
24h	4	HBA Capabilities Extended (GHC_CAP2)	0000003Ch
A0h	4	Vendor Specific (VSP)	00000048h
A4h	4	Vendor-Specific Capabilities Register (VS_CAP)	001002DEh
C0h	4	RAID Platform ID (RPID)	00311C02h
C4h	2	Premium Feature Block (PFB)	0000h
C8h	2	SW Feature Mask (SFM)	003Fh

15.2.1 HBA Capabilities (GHC_CAP) - Offset 0h

This register indicates basic capabilities of the HBA to driver software. The RWO bits in this register are only cleared upon PLTRST#. This register is not reset by FLR.

Type	Size	Offset	Default
MMIO	32 bit	ABAR + 0h	FF36FF07h

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW/O	**Supports 64-bit Addressing (S64A):** Indicates the S-ATA controller can access 64-bit data structures. The 32-bit upper bits of the port DMA Descriptor, the PRD Base, and each PRD entry are read/ write.
30	1h RW/O	**Supports Native Command Queuing Acceleration (SCQA):** Indicates the SATA controller supports Serial-ATA Native Command Queueing. The HBA will handle DMA Setup FISes in hardware, including support for auto-activiate optimization through the FIS.
29	1h RW/O	**Supports SNotification Register (SSNTF):** When set to 1, indicates that the HBA supports the PxSNTF (SNotification) register and its associated functionality. When cleared to 0, the HBA does not support the PxSNTF (SNotification) register and its associated functionality.

Bit Range	Default & Access	Field Name (ID): Description
28	1h RW/O	**Supports Mechanical Presence Switch (SMPS):** When set to 1, the HBA supports mechanical presence switches on its ports for use in hot plug operations. When cleared to 0, this function is not supported. This value is loaded by the BIOS prior to OS initialization.
27	1h RW/O	**Supports Staggered Spin-up (SSS):** Indicates whether the SATA controller supports staggered spin-up on its ports, for use in balancing power spikes. This value is loaded by platform BIOS prior to OS initialization.
26	1h RW/O	**Supports Aggressive Link Power Management (SALP):** Indicates the SATA controller supports auto-generating link requests to the partial or slumber states when there are no commands to process. When cleared to 0, software shall treat the PxCMD.ALPE and PxCMD.ASP bits as reserved.
25	1h RW/O	**Supports Activity LED (SAL):** Indicates the SATA controller supports a single output pin (SATALED#) which indicates activity.
24	1h RW/O	**Supports Command List Override (SCLO):** When set to 1, indicates that the HBA supports the PxCMD.CLO bit and it's associated function. When cleared to 0, The HBA is not capable of clearing the BSY and DRQ bits in the Status register in order to issue a software reset if these bits are still set from a previous operation.
23:20	3h RW/O	**Interface Speed Support (ISS):** Indicates the maximum speed the SATA controller can support on its ports. These encodings match the system software programmable PxSCTL.DET.SPD field. 0000 = Reserved; 0001 = Gen 1 (1.5 Gbps); 0010 = Gen 2 (3 Gbps); 0011 = Gen 3 (6 Gbps); 0100 - 1111 = Reserved. If (FFSATA0p0, FFSATA0p1, FFSATA0p2, FFSATA0p3, FFSATA0p4, FFSATA0p5, FFSATA0p6 and FFSATA0p7) are all 1, this field is RWO defaulting to 0010 and ignores software write value of 0011. If either FFSATA0p0, FFSATA0p1, FFSATA0p2, FFSATA0p3, FFSATA0p4, FFSATA0p5, FFSATA0p6 or FFSATA0p7 is 0, this field is RWO defaulting to 0011.
19	0h RO	**Reserved**
18	1h RO	**Supports AHCI mode only (SAM):** The SATA controller may optionally support AHCI access mechanism only. A value of 0 indicates that in addition to the native AHCI mechanism (via ABAR), the SATA controller implements a legacy, task-file based register interface such as SFF-8038i. A value of 1 indicates that the SATA controller does not implement a legacy, task-file based register interface.
17	1h RW/O	**Supports Port Multiplier (SPM):** The SATA controller may optionally support command-based switching Port Multipliers. BIOS must clear this bit if Port Multipliers are not supported.
16	0h RO	**FIS-based Switching Supported (FBSS):** Not supported.
15	1h RO	**PIO Multiple DRQ Block (PMD):** If set to 1, the HBA supports multiple DRQ block data transfers for the PIO command protocol.
14	1h RW/O	**Slumber State Capable (SSC):** The SATA controller supports the slumber state.
13	1h RW/O	**Partial State Capable (PSC):** The SATA controller supports the partial state.
12:8	1Fh RO	**Number of Command Slots (NCS):** 1Fh indicating support for 32 slots.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Command Completion Coalescing Supported (CCCS):** When set to 1, indicates that the HBA supports command completion coalescing. When command completion coalescing is supported, the HBA has implemented the CCC_CTL and the CCC_PORTS global HBA registers. When cleared to 0, indicates that the HBA does not support command completion coalescing and the CCC_CTL and CCC_PORTS global HBA registers are not implemented.
6	0h RW/O/V	**Enclosure Management Supported (EMS):** When set to 1, indicates that the HBA supports enclosure management. When enclosure management is supported, the HBA has implemented the EM_LOC and EM_CTL global HBA registers. When cleared to 0, indicates that the HBA does not support enclosure management and the EM_LOC and EM_CTL global HBA registers are not implemented. Implementation note: the default value is governed by the parameter SATA_EM_EN. When SATA_EM_EN=1, the attribute-reset is RWO-one. When SATA_EM_EN=0, the attribute-reset is RO-zero.
5	0h RW/O	**Supports External SATA (SXS):** When set to 1, indicates that the HBA has one or more Serial ATA ports that have a signal only connector that is externally accessible. If this bit is set, software may check with the PxCMD.ESP bit to determine whether a specific port has its signal connector externally accessible as a signal only connector (i.e. power is not part of that connector). When the bit is cleared to 0, indicates that the HBA has no Serial ATA ports that have a signal only connector externally accessible.
4:0	07h RO/V	**Number of Ports (NP):** 0's based value indicating the maximum number of ports supported. Note that the number of ports indicated in this field may be more than the number of ports indicated in the PI register. Number of ports shall be dependent on fuses (FFSATA7, FFSATA8) and SATA PORT MUXing configuration where if ANY of these parameter disables a particular port then that port is disabled and not counted.

15.2.2 Global HBA Control (GHC) - Offset 4h

This register controls various global actions of the HBA.

Type	Size	Offset	Default
MMIO	32 bit	ABAR + 4h	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**AHCI Enable (AE):** When set, indicates that an AHCI driver is loaded and communication to the HBA shall be via AHCI mechanisms. This can be used by an HBA that supports both legacy mechanisms (such as SFF-8038i) and AHCI to know when the HBA is running under an AHCI driver. When set, software shall only talk to the HBA using AHCI. The HBA will not have to allow command processing via both AHCI and legacy mechanisms. When cleared, software will only communicate with the HBA using legacy mechanisms. Software shall set this bit to 1 before accessing other AHCI registers. The implementation of this bit is dependent upon the value of the CAP.SAM bit. If CAP.SAM is 0, then GHC.AE should be RW and shall have a reset value of 0. If CAP.SAM is 1, then AE shall be read only and shall have a reset value of 1.
30:3	0h RO	**Reserved**
2	0h RO	**MSI Revert to Single Message (MRSM):** When set to 1 by hardware, indicates that the HBA requested more than one MSI vector but has reverted to using the first vector only. When this bit is cleared to 0, the HBA has not reverted to single MSI mode (i.e. hardware is already in single MSI mode, software has allocated the number of messages requested, or hardware is sharing interrupt vectors if MC.MME < MC.MMC). The HBA may revert to single MSI mode when the number of vectors allocated by the host is less than the number requested. This bit shall only be set to 1 when the following conditions hold: MC.MSIE = 1 (MSI is enabled); MC.MMC > 0 (multiple messages requested); MC.MME > 0 (more than one message allocated); MC.MME != MC.MMC (messages allocated not equal to number requested). When this bit is set to 1, single MSI mode operation is in use and software is responsible for clearing bits in the IS register to clear interrupts. This bit shall be cleared to 0 by hardware when any of the four conditions stated are false. This bit is also cleared to 0 when MC.MSIE = 1 and MC.MME = 0h. In this case, the hardware has been programmed to use single MSI mode, and is not reverting to that mode. The HBA shall always revert to single MSI mode when the number of vectors allocated by the host is less than the number requested.
1	0h RW	**Interrupt Enable (IE):** This global bit enables interrupts from the HBA. When cleared (reset default), all interrupt sources from all ports are disabled. When set, interrupts are enabled.
0	0h RW/1S/V	**HBA Reset (HR):** When set by SW, this bit causes an internal reset of the HBA. All state machines that relate to data transfers and native command queuing will return to an idle condition, and all ports will be re-initialized via COMRESET. When the HBA has performed the reset action, it will reset this bit to 0. A software writes of 0 will have no effect.

15.2.3 Interrupt Status Register (IS) - Offset 8h

This register indicates which of the ports within the controller have an interrupt pending and require service.

Type	Size	Offset	Default
MMIO	32 bit	ABAR + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW/1C/V	**Interrupt Pending Status Port 7 (IPS7):** If set, indicates that port 7 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt. This bit is only applicable to project(s) that has port 7 physically.
6	0h RW/1C/V	**Interrupt Pending Status Port 6 (IPS6):** If set, indicates that port 6 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt. This bit is only applicable to project(s) that has port 6 physically.
5	0h RW/1C/V	**Interrupt Pending Status Port 5 (IPS5):** If set, indicates that port 5 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt. This bit is only applicable to project(s) that has port 5 physically.
4	0h RW/1C/V	**Interrupt Pending Status Port 4 (IPS4):** If set, indicates that port 4 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt. This bit is only applicable to project(s) that has port 4 physically.
3	0h RW/1C/V	**Interrupt Pending Status Port 3 (IPS3):** If set, indicates that port 3 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt. This bit is only applicable to project(s) that has port 3 physically.
2	0h RW/1C/V	**Interrupt Pending Status Port 2 (IPS2):** If set, indicates that port 2 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt. This bit is only applicable to project(s) that has port 2 physically.
1	0h RW/1C/V	**Interrupt Pending Status Port 1 (IPS1):** If set, indicates that port 1 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt. This bit is only applicable to project(s) that has port 1 physically.
0	0h RW/1C/V	**Interrupt Pending Status Port 0 (IPS0):** If set, indicates that port 0 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt. This bit is only applicable to project(s) that has port 0 physically.

15.2.4 Ports Implemented (GHC_PI) - Offset Ch

This register indicates which ports are exposed to the HBA. It is loaded by platform BIOS. It indicates which ports that the device supports are available for software to use. Any available port may not be implemented.

Note: If a Fabric Decoding scheme is used, this register bit is shadowed by the Fabric Decoder.

Type	Size	Offset	Default
MMIO	32 bit	ABAR + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW/O/V	**Port 7 Implemented (PI7):** If set, then port 7 is available for use. If cleared, the port is not available for use. This bit is reserved and is read-only 0 if below condition is true else it's RWO-zero: Check with CAP.NP where port 7 is not available.
6	0h RW/O/V	**Port 6 Implemented (PI6):** If set, then port 6 is available for use. If cleared, the port is not available for use. This bit is reserved and is read-only 0 if below condition is true else it's RWO-zero: Check with CAP.NP where port 6 is not available.
5	0h RW/O/V	**Port 5 Implemented (PI5):** If set, then port 5 is available for use. If cleared, the port is not available for use. This bit is reserved and is read-only 0 if below condition is true else it's RWO-zero: Check with CAP.NP where port 5 is not available.
4	0h RW/O/V	**Port 4 Implemented (PI4):** If set, then port 4 is available for use. If cleared, the port is not available for use. This bit is reserved and is read-only 0 if below condition is true else it's RWO-zero: Check with CAP.NP where port 4 is not available.
3	0h RW/O/V	**Port 3 Implemented (PI3):** If set, then port 3 is available for use. If cleared, the port is not available for use. This bit is reserved and is read-only 0 if below condition is true else it's RWO-zero: Check with CAP.NP where port 3 is not available.
2	0h RW/O/V	**Port 2 Implemented (PI2):** If set, then port 2 is available for use. If cleared, the port is not available for use. This bit is reserved and is read-only 0 if below condition is true else it's RWO-zero: Check with CAP.NP where port 2 is not available.
1	0h RW/O/V	**Port 1 Implemented (PI1):** If set, then port 1 is available for use. If cleared, the port is not available for use. This bit is reserved and is read-only 0 if below condition is true else it's RWO-zero: Check with CAP.NP where port 1 is not available.
0	0h RW/O/V	**Port 0 Implemented (PI0):** If set, then port 0 is available for use. If cleared, the port is not available for use. This bit is reserved and is read-only 0 if below condition is true else it's RWO-zero: CHeck with CAP.NP where port 0 is not available.

15.2.5 AHCI Version (VS) - Offset 10h

This register indicates the major and minor version of the AHCI specification. It is BCD encoded. The upper two bytes represent the major version number, and the lower two bytes represent the minor version number. Example: Version 3.12 would be represented as 00030102h.

Type	Size	Offset	Default
MMIO	32 bit	ABAR + 10h	00010301h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0001h RO	**Major Version Number (MJR):** Indicates the major version is 1.
15:0	0301h RO	**Minor Version Number (MNR):** Indicates the minor version is 31.

15.2.6 Enclosure Management Location (EM_LOC) - Offset 1Ch

The enclosure management location register identifies the location and size of the enclosure management message buffer. This register is not implemented if enclosure management is not supported (i.e. CAP.EMS = 0).

Type	Size	Offset	Default
MMIO	32 bit	ABAR + 1Ch	01600002h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0160h RO	**OFST:** The offset of the message buffer in Dwords from the beginning of the ABAR.
15:0	0002h RO	**Buffer Size (SZ):** Specifies the size of the transmit message buffer area in Dwords. If both transmit and receive buffers are supported, then the transmit buffer begins at ABAR[EM_LOC.OFST*4] and the receive buffer directly follows it. If both transmit and receive buffers are supported, both buffers are of the size indicated in the Buffer Size field. A value of 0 is invalid. The SATA controller only supports transmit buffer.

15.2.7 Enclosure Management Control (EM_CTL) - Offset 20h

This register is used to control and obtain status for the enclosure management interface. The register includes information on the attributes of the implementation, enclosure management messages supported, the status of the interface, whether any messages are pending, and is used to initiate sending messages. This register is not implemented if enclosure management is not supported (i.e. CAP.EMS = 0).

Type	Size	Offset	Default
MMIO	32 bit	ABAR + 20h	07010000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**Port Multiplier Support (ATTR_PM):** The HBA does not support enclosure management messages for devices attached via a Port Multiplier. Software should use the Serial ATA enclosure management bridge that is built into many Port Multipliers for enclosure services with these devices. For more information on Serial ATA enclosure management bridges, check with the Serial ATA II: Extensions to Serial ATA 1.0a revision 1.2 specification.
26	1h RW/O	**Activity LED Hardware Driven (ATTR_ALHD):** If set to 1, the HBA drives the activity LED for the LED message type in hardware and does not utilize software settings for this LED. The HBA does not begin transmitting the hardware based activity signal until after software has written CTL.TM=1 after a reset condition.
25	1h RO	**Transmit Only (ATTR_XMT):** If set to 1, the HBA only supports transmitting messages and does not support receiving messages. If cleared to 0, the HBA supports transmitting and receiving messages.
24	1h RO	**Single Message Buffer (ATTR_SMB):** If set to 1, the HBA has one message buffer that is shared for messages to transmit and messages received. In this case, unsolicited receive messages are not supported and it is software's responsibility to manage access to this buffer. If cleared to 0, there are separate receive and transmit buffers such that unsolicited messages could be supported.
23:20	0h RO	**Reserved**
19	0h RO	**SGPIO Enclosure Management Messages (SUPP_SGPIO):** If set to 1, the HBA supports the SGPIO register interface message type.
18	0h RO	**SES-2 Enclosure Management Messages (SUPP_SES2):** If set to 1, the HBA supports the SES-2 message type.
17	0h RO	**SAF-TE Enclosure Management Messages (SUPP_SAFTE):** If set to 1, the HBA supports the SAF-TE message type.
16	1h RO	**LED Message Types (SUPP_LED):** If set to 1, the HBA supports the LED message type defined in LED Message Type.
15:10	0h RO	**Reserved**
9	0h RW/1S/V	**RST:** When set to 1 by software, the HBA shall reset all enclosure management message logic and take all appropriate reset actions to ensure messages can be transmitted/received after the reset. After the HBA completes the reset operation, the HBA shall set the value to 0. A write of 0 by software to this field shall have no effect.
8	0h RW/1S/V	**Transmit Message (CTL_TM):** When set to 1 by software, the HBA shall transmit the message contained in the message buffer. When the message is completely sent, the HBA shall clear this bit to 0. A write of 0 to this bit by software shall have no effect. Software shall not change the contents of the message buffer while CTL.TM is set to 1.
7:1	0h RO	**Reserved**
0	0h RO	**Message Received (STS_MR):** Message received is not supported.

15.2.8 HBA Capabilities Extended (GHC_CAP2) - Offset 24h

This register indicates basic capabilities of the HBA to driver software. The RWO bits in this register are only cleared upon PLTRST#.

Type	Size	Offset	Default
MMIO	32 bit	ABAR + 24h	0000003Ch

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	1h RW/O	**DEVSLP Entrance from Slumber Only (DESO):** This field specifies that the HBA shall only assert DEVSLP if the interface is in Slumber. When this bit is set to 1, the HBA shall ignore software directed entrance to DEVSLP via PxCMD.ICC unless PxSSTS.IPM = 6h. When this bit is cleared to 0, the HBA may enter DEVSLP from any link state (active, Partial, or Slumber). BIOS is required to program this field to 1.
4	1h RW/O/V	**Supports Aggressive DEVSLP Management (SADM):** When set to 1, the HBA supports hardware assertion of the DEVSLP signal after the idle timeout expires. When cleared to 0, this function is not supported and software shall treat the PxDEVSLP.ADSE field as reserved. If SATA PHY PM Disable Fuse is 1, this register will read 0. Else this register will read 1 with RWO attribute.
3	1h RW/O/V	**Supports DEVSLP (SDS):** When set to 1, the HBA supports the DEVSLP feature. When cleared to 0, DEVSLP is not supported. ***Note:*** If SATA PHY PM Disable Fuse is 1, this register will read 0. Else this register will read 1 with RWO attribute.
2	1h RW/O/V	**Automatic Partial to Slumber Transitions (APST):** When set to 1, the HBA supports Automatic Partial to Slumber Transitions. When cleared to 0, Automatic Partial to Slumber Transition is not supported. ***Note:*** If SATA PHY PM Disable Fuse is 1, this register will read only 0. Else this register will read 1 with RWO attribute.
1	0h RO	**Reserved**
0	0h RO	**BIOS/OS Handoff (BOH):** Not supported.

15.2.9 Vendor Specific (VSP) - Offset A0h

Vendor Specific.

Type	Size	Offset	Default
MMIO	32 bit	ABAR + A0h	00000048h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6	1h RO	**Software Feature Mask Supported (SFMS):** Set to 1 if the platform is enabled for premium storage features mask (SFM) as in VS MMIO space at offset ABAR[RPID.(OFST*4)+4].
5	0h RO/V	**Premium Features Supported (PFS):** Set to 1 if the platform is enabled for premium storage features (PFB) as in VS MMIO space at offset ABAR[RPID.OFST*4]. Set to 0 if the platform is not enabled for premium storage features. The state of this bit reflects the opposite state of fuse FFSATA5 & FFSATA 3 (PFS =1 if fuse values=10 or 11, else PFS=0) or the resulting state of Premium soft sku override (check with ME29 FLEXSKU.FLEXSKU_OVR or PMC MR_SSKUCONC.SHAD_SATA_PREMIUM_FEAT).
4	0h RO/V	**Platform Type (PT):** Set to 1 if mobile platform. Clear (0) if desktop.
3	1h RO	**Supports RAID Platform ID Reporting (SRPIR):** If set to 1, then indicates that the RAID Platform ID is reported via ABAR + C0h. Set to 0 if this ID is not reported via MMIO space.
2:0	0h RO	**Reserved**

15.2.10 Vendor-Specific Capabilities Register (VS_CAP) - Offset A4h

Vendor-Specific Capabilities Register.

Type	Size	Offset	Default
MMIO	32 bit	ABAR + A4h	001002DEh

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:16	010h RW/O	**NVM Remapped Register Offset (NRMO):** Specifies the offset (in 128B unit) within ABAR as to where the NVM Remap memory BAR register space is remapped. For example, NRMO=1 means ABAR + 128B. This allows the remapped offset to shift between ABAR + 0B, and ABAR + 512KK - 128B, with 128B step. The remapped offset into the AHCI memory space must not overlap with the memory space used for SATA. The remapped offset into the AHCI memory space and the remapped size must not exceed the allocated AHCI memory space of the integrated AHCI controller. Only valid when NRMBE = '1'. The reset default of this field is 10h, this places the start of the PCIe NAND memory BAR register space at ABAR + 2K. This field is not reset by FLR.

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**Reserved**
12:1	16Fh RW/O	**Memory Space Limit. (MSL):** This field specifies the size (in 128B unit) of the remapped memory space for the PCIe NAND device. It is a 0-based field. For example, MSL=1 means 256B. This allows the remapped size to shift between 128B and 512K with the step of 128B.Memory BAR offset from 0 to MSL of the PCIe NAND device are remapped under the integrated AHCI controller memory space. The remapped offset into the AHCI memory space and the value programmed in this field must not exceed the allocated AHCI memory space of the integrated AHCI controller. Only valid when NRMBE = 1. The reset default of this field is 16Fh which specifies the size of the remapped memory space as 34k.This field is not reset by FLR.
0	0h RW/O	**NVM Remap Memory BAR Enable (NRMBE):** Set to 1 if NVM Remap device is present and remapping of its memory BAR register space is enabled. Cleared to 0 if there is no PCIe NAND device present or the remapping of its memory BAR register space is disabled. This bit is not reset by FLR.

15.2.11 RAID Platform ID (RPID) - Offset C0h

This register is used by the Intel Matrix Storage Manager OROM to match the features supported by the OROM with the platform on which the OROM is executing. This prevents the use of an OROM designed for newer chipsets from being use on older chipsets as this could reduce up-sell potential.

Type	Size	Offset	Default
MMIO	32 bit	ABAR + C0h	00311C02h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0031h RO	**OFST:** The offset of the Premium Feature Block (PFB) in DWords from the beginning of the ABAR. SFM follows directly after PFB.
15:0	1C02h RO/V	**RAID Platform ID (RPID):** Specifies the DID value that has been assigned to the platform. This is the same DID that is reported by the SATA controller when SATAGC.AIE is set to 1 except that the DID is always reported through this register, regardless if the programming of SATAGC.AIE.

15.2.12 Premium Feature Block (PFB) - Offset C4h

Note: Bits 4-0 are not bit-mapped to individual fuses and/or soft SKU settings; rather FFSATA5& FFSATA 3 /soft sku is used to indicate support for all of these features (check with VSP.PFS). These registers indicate to the Intel Rapid Storage Technology AHCI driver that those premium RAID features that can be supported on the platform.

Type	Size	Offset	Default
MMIO	16 bit	ABAR + C4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**
1	0h RO	**Supports Email Alert (SEA):** Read value is the same as VSP.PFS. If set to 1, then this feature is supported as part of the premium feature set.
0	0h RO/V	**Supports OEM IOCTL (SOI):** Read value is the same as VSP.PFS. If set to 1, then this feature is supported as part of the premium feature set.

15.2.13 SW Feature Mask (SFM) - Offset C8h

The following will be programmed by the BIOS when VS_CAP.SFMS == 1. The feature mask is used by SW to determine which non-premium features shall be supported by SW. These register bits are not reset by FLR since they are programmed by BIOS.

Type	Size	Offset	Default
MMIO	16 bit	ABAR + C8h	003Fh

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11:10	0h RW/O	**OROM UI Normal Delay. (OROM_UI_NORMAL_DELAY):** Values of these bits specify the delay of the OROM UI Splash Screen in a normal status. 00 = 2 secs (default and previous value); 01 = 4 secs; 10 = 6 secs; 11 = 8 secs. If bit 5 == 0, then these values are disregarded.
9	0h RW/O	**Smart Response Technology. (SMART_RESPONSE_TECHNOLOGY):** If set to '1', then Smart Response Technology is enabled. If cleared to '0', the feature is disabled.
8	0h RW/O	**RRT Only on ESATA (IRRT_ONLY_ON_ESATA):** If set to 1, then only RRT volumes can span internal and external SATA ports (e.g. eSATA). If cleared to 0, then any RAID volume can span internal and external SATA ports (e.g. eSATA).
7	0h RW/O	**LED Locate (LED_LOCATE):** If set to 1, then LED/SGPIO hardware is attached and the ping to locate feature is enabled in the OS.
6	0h RW/O	**HDDUNLOCK:** If set to 1, then HDD password unlock is enabled in the OS.
5	1h RW/O	**OROM UI and BANNER (OROM_UI_AND_BANNER):** If set to 1, then the OROM UI is displayed. When cleared to 0, the OROM UI and BANNER are not displayed if all disks and volumes have a normal status.
4	1h RW/O	**IRRT:** If set to 1, then Rapid Recovery Technology is enabled.
3	1h RW/O	**R5:** If set to 1, then RAID5 is enabled

Bit Range	Default & Access	Field Name (ID): Description
2	1h RW/O	**R10:** If set to 1, then RAID10 is enabled
1	1h RW/O	**R1:** If set to 1, then RAID1 is enabled
0	1h RW/O	**R0:** If set to 1, then RAID0 is enabled

15.3 SATA AIDP Registers Summary

This chapter records SATA AIDP Register.

Base address for this register is defined in SATA PCI register in Bus:0, Device:23 Function:0.

The offset value for this register: 20h

Table 15-3. Summary of SATA AIDP Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
10h	4	AHCI Index Register (INDEX)	00000000h
14h	4	AHCI Data Register (DATA)	00000000h

15.3.1 AHCI Index Register (INDEX) - Offset 10h

This register is only available if CC.SCC is not 01h to index into all memory registers defined in Memory Registers and the message buffer used for enclosure management. If CC.SCC is 01h, these AHCI Index Data Pair registers are not accessible and SINDEX/SDATA register pair shall be used to index into a subset of the memory registers defined in (See Memory Registers for more information on which registers could be indexed).

Type	Size	Offset	Default
MMIO	32 bit	AIDP + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18:2	00000h RW	**INDEX:** This Index register is used to select the Dword offset of the Memory Mapped AHCI register to be accessed. A Dword, Word or Byte access is specified by the active byte enables of the I/O access to the Data register.
1:0	0h RO	**Reserved**

15.3.2 AHCI Data Register (DATA) - Offset 14h

This register is index into all memory registers defined in Memory Registers and the message buffer used for enclosure management.

Type	Size	Offset	Default
MMIO	32 bit	AIDP + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DATA:** This Data register is a window through which data is read or written to the memory mapped register pointed to by the Index register. Note that a physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the default value is the same as the default value of the register pointed to by Index.

15.4 SATA MXPBA Registers Summary

Table 15-4. Summary of SATA MXPBA Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	MSI-X Pending Bit Array QW 0 (MXPQW0_DW0)	00000000h

15.4.1 MSI-X Pending Bit Array QW 0 (MXPQW0_DW0) - Offset 0h

MSI-X Pending Bit Array QW 0.

Type	Size	Offset	Default
MMIO	32 bit	MXPBA + 0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO/V	**MSI-X vector Pending (MXVP):** For each Pending Bit that is set, the function has a pending message for the associated MSI-X Table entry. Pending bits that have no associated MSI-X Table entry are reserved. After reset, the state of reserved Pending bits must be 0. Software should never write, and should only read Pending Bits. If software writes to Pending Bits, the result is undefined. Each Pending Bit's state after reset is 0 (no message pending).

16 Host Embedded Controller Interface (HECI)

16.1 HECI Configuration Registers Summary

This chapter records the registers in Bus: 0, Device 22, Function 0, 1, 4 and 5.

DID Values:

- HECI #1:- D22: F0 - 4B70h
- HECI #2:- D22: F1 - 4B71h
- HECI #3:- D22: F4 - 4B74h
- HECI #4:- D22: F5 - 4B75h

Table 16-1. Summary of Bus: 0, Device: 22, Function: 5 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	HECI ID (HECI4_ID)	4B758086h
4h	2	HECI Command (HECI4_CMD)	0000h
6h	2	HECI Status (HECI4_STS)	0010h
8h	4	Revision ID And Class Code (HECI4_RID_CC)	07800000h
Ch	1	Cache Line Size (HECI4_CLS)	00h
Dh	1	Master Latency Timer (HECI4_MLT)	00h
Eh	1	Header Type (HECI4_HTYPE)	80h
Fh	1	Built In Self-Test (HECI4_BIST)	00h
10h	4	HECI MMIO Base Address Low (HECI4_MMIO_MBAR_LO)	00000004h
14h	4	HECI MMIO Base Address High (HECI4_MMIO_MBAR_HI)	00000000h
2Ch	4	Sub System Identifiers (HECI4_SS)	00000000h
34h	4	Capabilities Pointer (HECI4_CAP)	00000050h
3Ch	2	Interrupt Information (HECI4_INTR)	0100h
3Eh	1	Minimum Grant (HECI4_MGNT)	00h
3Fh	1	Maximum Latency (HECI4_MLAT)	00h
40h	4	Host Firmware Status (HECI4_HFS)	00000000h
48h	4	General Status Shadow 1 (HECI4_GS_SHDW1)	00000000h
4Ch	4	Host General Status (HECI4_H_GS1)	00000000h
50h	2	PCI Power Management Capability ID (HECI4_PID)	8C01h
52h	2	PCI Power Management Capabilities (HECI4_PC)	4003h
54h	2	PCI Power Management Control And Status (HECI4_PMCS)	0008h
60h	4	General Status Shadow 2 (HECI4_GS_SHDW2)	00000000h
64h	4	General Status Shadow 3 (HECI4_GS_SHDW3)	00000000h
68h	4	General Status Shadow 4 (HECI4_GS_SHDW4)	00000000h
6Ch	4	General Status Shadow 5 (HECI4_GS_SHDW5)	00000000h
70h	4	Host General Status 2 (HECI4_H_GS2)	00000000h
74h	4	Host General Status 3 (HECI4_H_GS3)	00000000h
8Ch	2	Message Signaled Interrupt Identifiers (HECI4_MID)	A405h
8Eh	2	Message Signaled Interrupt Message Control (HECI4_MC)	0080h
90h	4	Message Signaled Interrupt Message Address (HECI4_MA)	00000000h
94h	4	Message Signaled Interrupt Upper Address (HECI4_MUA)	00000000h
98h	2	Message Signaled Interrupt Message Data (HECI4_MD)	0000h
A0h	1	HECI Interrupt Delivery Mode (HECI4_HIDM)	00h
A4h	4	Vendor Specific Capability Register (HECI4_VSCR)	F0140009h
A8h	4	Vendor Specific Extended Capability Register (HECI4_VSEC)	01400010h
ACh	4	SW LTR Pointer Register (HECI4_SWLTRPTR)	00000000h
B0h	4	Device Idle Pointer Register (HECI4_DEVIDLEPTR)	00008001h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
B4h	2	Device Idle Power On Latency (HECI4_DEVIDLEPOL)	0D38h
B6h	2	DevIdle Power Control Enabled Register (HECI4_PWRCTRLEN)	000Eh
F8h	4	Manufacturer's ID (HECI4_MANID)	00000000h

16.1.1 HECI ID (HECI4_ID) - Offset 0h

Identification

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:22, F:5] + 0h	4B758086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4B75h RO/V	**Device ID (DID):** Indicates device number assigned by Intel. The upper 9 bits of this field are set by a special sideband message (SetIDValue). The lower 7 bits are set by soft straps. Note that the default value of this field is not 0, but depends on the value of soft straps.
15:0	8086h RO	**Vendor ID (VID):** 16-bit field which indicates Intel is the vendor, assigned by the PCI SIG.

16.1.2 HECI Command (HECI4_CMD) - Offset 4h

Command

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:22, F:5] + 4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable (ID):** Disables this device from generating PCI line based interrupts. This bit does not have any effect on MSI operation.
9	0h RO	**Fast Back-to-Back Enable (FBE):** Not implemented, hardwired to 0.
8	0h RO	**SERR# Enable (SEE):** Not implemented, hardwired to 0.
7	0h RO	**Wait Cycle Enable (WCC):** Not implemented, hardwired to 0.
6	0h RO	**Parity Error Response Enable (PEE):** Not implemented, hardwired to 0.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**VGA Palette Snooping Enable (VAG):** Not implemented, hardwired to 0
4	0h RO	**Memory Write And Invalidate Enable (MWIE):** Not implemented, hardwired to 0.
3	0h RO	**Special Cycle Enable (SCE):** Not implemented, hardwired to 0.
2	0h RW	**Bus Master Enable (BME):** Controls the HECI host controller's ability to act as a system memory master for data transfers. When this bit is cleared, HECI bus master activity stops and any active DMA engines return to an idle condition. This bit is made visible to firmware through the H_PCI_CSR register, and changes to this bit may be configured by the H_PCI_CSR register to generate an MSI to mIA. When this bit is '0', HECI is blocked from generating MSI to the host CPU. Note that this bit does not block HECI accesses to CSE-UMA.
1	0h RW	**Memory Space Enable (MSE):** Controls access to the HECI host controller's memory mapped register space.
0	0h RO	**I/O Space Enable (IOSE):** Not implemented, hardwired to 0.

16.1.3 HECI Status (HECI4_STS) - Offset 6h

Status

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:22, F:5] + 6h	0010h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Detected Parity Error (DPE):** Not implemented, hardwired to 0.
14	0h RO	**Signaled System Error (SSE):** Not implemented, hardwired to 0.
13	0h RO	**Received Master-Abort (RMA):** Not implemented, hardwired to 0.
12	0h RO	**Received Target Abort (RTA):** Not implemented, hardwired to 0.
11	0h RO	**Signaled Target-Abort (STA):** Not implemented, hardwired to 0.
10:9	0h RO	**DEVSEL# Timing (DEVT):** These bits are hardwired to 00.
8	0h RO	**Master Data Parity Error Detected (DPD):** Not implemented, hardwired to 0.
7	0h RO	**Fast Back-to-Back Capable (FBC):** Not implemented, hardwired to 0.
6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**66 MHz Capable (C66):** Not implemented, hardwired to 0.
4	1h RO	**Capabilities List (CL):** Indicates the presence of a capabilities list, hardwired to 1.
3	0h RO/V	**Interrupt Status (IS):** Reflects the state of the INTx# signal at the input of the enable/disable circuit. This bit is a 1 when the INTx# is asserted. This bit is a 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the command register). Note that this bit is not set by an MSI.
2:0	0h RO	**Reserved**

16.1.4 Revision ID And Class Code (HECI4_RID_CC) - Offset 8h

Revision ID And Class Code

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:22, F:5] + 8h	07800000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	07h RO	**Base Class Code (BCC):** Indicates the base class code of the HECI host controller device.
23:16	80h RO	**Sub Class Code (SCC):** Indicates the sub class code of the HECI host controller device.
15:8	00h RO	**Programming Interface (PI):** Indicates the programming interface of the HECI host controller device.
7:0	00h RO/V	**Revision ID (RID):** Indicates stepping of the HECI host controller. This field is set by a special IOSF SB message (SetIDValue).

16.1.5 Cache Line Size (HECI4_CLS) - Offset Ch

Cache Line Size

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:22, F:5] + Ch	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Cache Line Size (CLS):** Not implemented, hardwired to 0.

16.1.6 Master Latency Timer (HECI4_MLT) - Offset Dh

Master Latency Timer

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:22, F:5] + Dh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Master Latency Timer (MLT):** Not implemented, hardwired to 0.

16.1.7 Header Type (HECI4_HTYPE) - Offset Eh

Header Type

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:22, F:5] + Eh	80h

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Multi-Function Device (MFD):** Indicates the HECI host controller is part of a multi-function device.
6:0	00h RO	**Header Layout (HL):** Indicates that the HECI host controller uses a target device layout.

16.1.8 Built In Self-Test (HECI4_BIST) - Offset Fh

Built In Self-Test

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:22, F:5] + Fh	00h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**BIST Capable (BC):** Not implemented, hardwired to 0.
6:0	0h RO	**Reserved**

16.1.9 HECI MMIO Base Address Low (HECI4_MMIO_MBAR_LO) - Offset 10h

HECI MMIO Base Address Low

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:22, F:5] + 10h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Low (BA_LO):** Lower 32 bits of base address of register memory space.
11:4	00h RO	**Memory Size (MS):** This field is hardwired to 0 to indicate that HECI device requests 4KB of memory space.
3	0h RO	**PF:** Indicates that this range is not pre-fetchable.
2:1	2h RO	**TP:** Indicates that this range can be mapped anywhere in 64-bit address space.
0	0h RO	**Resource Type Indicator (RTE):** Indicates a request for register memory space.

16.1.10 HECI MMIO Base Address High (HECI4_MMIO_MBAR_HI) - Offset 14h

HECI MMIO Base Address High

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:22, F:5] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High (BA_HI):** Upper 32 bits of base address of register memory space.

16.1.11 Sub System Identifiers (HECI4_SS) - Offset 2Ch

Sub System Identifiers

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:22, F:5] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SSID):** Indicates the subsystem identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only.
15:0	0000h RW/O	**Subsystem Vendor ID (SSVID):** Indicates the subsystem vendor identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only.

16.1.12 Capabilities Pointer (HECI4_CAP) - Offset 34h

Capabilities Pointer

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:22, F:5] + 34h	00000050h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	50h RO	**Capability Pointer (CP):** Indicates the first capability pointer offset. It points to the PCI power management capability offset.

16.1.13 Interrupt Information (HECI4_INTR) - Offset 3Ch

Interrupt Information

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:22, F:5] + 3Ch	0100h

Bit Range	Default & Access	Field Name (ID): Description
15:8	01h RO/V	**Interrupt Pin (IPIN):** This field indicates the virtual interrupt pin the HECI host controller uses. A value of 0x1/0x2/0x3/0x4 indicates that this function implements legacy interrupt on INTA/INTB/INTC/INTD, respectively. When legacy interrupt is not used this register should be set to 0x0. Programmed by BIOS over IOSF SB through corresponding Private CR register.
7:0	00h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this field.

16.1.14 Minimum Grant (HECI4_MGNT) - Offset 3Eh

Minimum Grant

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:22, F:5] + 3Eh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**GNT:** Not implemented, hardwired to 0.

16.1.15 Maximum Latency (HECI4_MLAT) - Offset 3Fh

Maximum Latency

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:22, F:5] + 3Fh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**LAT:** Not implemented, hardwired to 0.

16.1.16 Host Firmware Status (HECI4_HFS) - Offset 40h

Host Firmware Status

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:22, F:5] + 40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Firmware Status Host Access (FS_HA):** Indicates current status of the firmware for the HECI controller. This field is the host's read only access to the FS field in the CSE Firmware Status register.

16.1.17 General Status Shadow 1 (HECI4_GS_SHDW1) - Offset 48h

General Status Shadow 1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:22, F:5] + 48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**General Status Shadow 1 (GSS1):** This field is host side shadow of CSE General Status 1 (CSE_GS1).

16.1.18 Host General Status (HECI4_H_GS1) - Offset 4Ch

Host General Status

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:22, F:5] + 4Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Host General Status (H_GS1):** General status of Host. This field is not used by hardware.

16.1.19 PCI Power Management Capability ID (HECI4_PID) - Offset 50h

PCI Power Management Capability ID

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:22, F:5] + 50h	8C01h

Bit Range	Default & Access	Field Name (ID): Description
15:8	8Ch RO	**Next Capability (NEXT):** Indicates the location of the next capability item in the list. This is the Message Signaled Interrupts capability.
7:0	01h RO	**Cap ID (CID):** Indicates that this pointer is a PCI power management.

16.1.20 PCI Power Management Capabilities (HECI4_PC) - Offset 52h

PCI Power Management Capabilities

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:22, F:5] + 52h	4003h

Bit Range	Default & Access	Field Name (ID): Description
15:11	08h RO	**PME Support (PSUP):** Indicates the states that can generate PME#. HECI can assert PME# from D3hot only.
10	0h RO	**D2 Support (D2S):** The D2 state is not supported for the HECI host controller.
9	0h RO	**D1 Support (D1S):** The D1 state is not supported for the HECI host controller.
8:6	0h RO	**Aux Current (AUXC):** Reports the maximum Suspend well current required when in the D3COLD state. Value of 0 is reported.
5	0h RO	**Device Specific Initialization (DSI):** Indicates whether device-specific initialization is required.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**Reserved**
3	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
2:0	3h RO	**VS:** Indicates support for Revision 1.2 of the PCI Power Management Specification.

16.1.21 PCI Power Management Control And Status (HECI4_PMCS) - Offset 54h

PCI Power Management Control And Status

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:22, F:5] + 54h	0008h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**PME Status (PMES):** The PME Status bit in HECI space can be set to '1' by CSE FW performing a write into CSE side register to set PMES. This bit is cleared by host CPU writing a '1' to it. CSE cannot clear this bit. Host CPU writes with value '0' have no effect on this bit.
14:9	0h RO	**Reserved**
8	0h RW	**PME Enable (PMEE):** When set, PME_assert and PME_deassert messages are sent over Sideband to PMC based on the PMES bit. When reset these messages may not be sent.
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset (NSR):** This bit indicates that when the HECI host controller is transitioning from D3hot to D0 due to power state command, it does not perform an internal reset.
2	0h RO	**Reserved**
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the HECI host controller and to set a new power state. The values are: 00 - D0 state 11 - D3HOT state The D1 and D2 states are not supported for this HECI host controller. If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus; however, the data is discarded and no state change occurs. When in the D3HOT state, the HBA's configuration space is available, but the registers memory space is not. Additionally, interrupts are blocked. This field is visible to firmware through the H_PCI_CSR register, and changes to this field may be configured by the H_PCI_CSR register to generate an MSI to mIA.

16.1.22 General Status Shadow 2 (HECI4_GS_SHDW2) - Offset 60h

General Status Shadow 2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:22, F:5] + 60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**General Status Shadow 2 (GSS2):** This field is host side shadow of CSE General Status 2 (CSE_GS2).

16.1.23 General Status Shadow 3 (HECI4_GS_SHDW3) - Offset 64h

General Status Shadow 3

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:22, F:5] + 64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**General Status Shadow 3 (GSS3):** This field is host side shadow of CSE General Status 3 (CSE_GS3).

16.1.24 General Status Shadow 4 (HECI4_GS_SHDW4) - Offset 68h

General Status Shadow 4

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:22, F:5] + 68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**General Status Shadow 4 (GSS4):** This field is host side shadow of CSE General Status 4 (CSE_GS4).

16.1.25 General Status Shadow 5 (HECI4_GS_SHDW5) - Offset 6Ch

General Status Shadow 5

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:22, F:5] + 6Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**General Status Shadow 5 (GSS5):** This field is host side shadow of CSE General Status 5 (CSE_GS5).

16.1.26 Host General Status 2 (HECI4_H_GS2) - Offset 70h

Host General Status 2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:22, F:5] + 70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Host General Status 2 (H_GS2):** General status of Host. This field is not used by hardware.

16.1.27 Host General Status 3 (HECI4_H_GS3) - Offset 74h

Host General Status 3

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:22, F:5] + 74h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Host General Status 3 (H_GS3):** General status of Host. This field is not used by hardware.

16.1.28 Message Signaled Interrupt Identifiers (HECI4_MID) - Offset 8Ch

Message Signaled Interrupt Identifiers

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:22, F:5] + 8Ch	A405h

Bit Range	Default & Access	Field Name (ID): Description
15:8	A4h RO	**Next Pointer (NEXT):** Indicates the location of the next capability item in the list. This is the DevIdle conventional PCI vendor specific capability.
7:0	05h RO	**Capability ID (CID):** Indicates MSI.

16.1.29 Message Signaled Interrupt Message Control (HECI4_MC) - Offset 8Eh

Message Signaled Interrupt Message Control

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:22, F:5] + 8Eh	0080h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7	1h RO	**64 Bit Address Capable (C64):** Specifies whether capable of generating 64-bit messages.
6:4	0h RO	**Multiple Message Enable (MME):** Not implemented, hardwired to 0.
3:1	0h RO	**Multiple Message Capable (MMC):** Not implemented, hardwired to 0.
0	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and INTx virtual wires are not used to generate interrupts.

16.1.30 Message Signaled Interrupt Message Address (HECI4_MA) - Offset 90h

Message Signaled Interrupt Message Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:22, F:5] + 90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**ADDR:** Lower 32 bits of the system specified message address, always DW aligned.
1:0	0h RO	**Reserved**

16.1.31 Message Signaled Interrupt Upper Address (HECI4_MUA) - Offset 94h

Message Signaled Interrupt Upper Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:22, F:5] + 94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Upper Address (UADDR):** Upper 32 bits of the system specified message address. This register is optional and only implemented if MC.C64=1.

16.1.32 Message Signaled Interrupt Message Data (HECI4_MD) - Offset 98h

Message Signaled Interrupt Message Data

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:22, F:5] + 98h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**DATA:** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the FSB during the data phase of the MSI memory write transaction.

16.1.33 HECI Interrupt Delivery Mode (HECI4_HIDM) - Offset A0h

HECI Interrupt Delivery Mode

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:22, F:5] + A0h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved**
2	0h RW/1S/V	**HIDM Lock (HIDM_L):** Writing 1 to this bit locks the HIDM field.
1:0	0h RW/L	**HECI Interrupt Delivery Mode (HIDM):** These bits control what type of interrupt the HECI will send when CSE FW writes to set the CSE_IG bit. They are interpreted as follows: 00 - Generate Legacy or MSI interrupt; 01 - Generate SCI; 10 - Generate SMI; This field may be locked by writing 1 to HIDM_L bit. **Locked by:** HECI4_HIDM.HIDM_L

16.1.34 Vendor Specific Capability Register (HECI4_VSCR) - Offset A4h

Vendor Specific Capability Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:22, F:5] + A4h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor-Specific Capability ID (VSID):** A value of 4'hF in this 4-bit field identifies this Vendor Specific Capability as an Extended Capability, which uses a VSEC 16-bit Extended Capability ID in the subsequent four bytes. This field allows software to differentiate this capability from other Vendor Specific capabilities.
27:24	0h RO	**Vendor Specific Capability Revision (VSREV):** For a VSID of 4'hF, this field is reserved 4'h0.
23:16	14h RO	**Vendor Specific Capability Length (VSLEN):** This field indicates the number of bytes of this Vendor Specific capability as required by the PCI spec inclusive of the CapID and Next Pointer. It has the value of 8'h14 for the DevIdle Capability.
15:8	00h RO	**Next Capability Pointer (NEXT):** Pointer to the configuration offset of the next Capability item. It is 8'h00 since it is the final item in the Capability list.
7:0	09h RO	**Capability ID (CAPID):** The value of 8h09 in this field indicates a Vendor Specific capability.

16.1.35 Vendor Specific Extended Capability Register (HECI4_VSEC) - Offset A8h

Vendor Specific Extended Capability Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:22, F:5] + A8h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific Extended Capability Length (VSECLEN):** This field indicates the number of bytes of this Vendor Specific capability inclusive of the 1st DW which includes the capability ID and Next pointer. For DevIdle, this is 12'h14.
19:16	0h RO	**Vendor Specific Extended Capability Revision (VSECREV):** For this revision of DevIdle, this field is 4h0.
15:0	0010h RO	**Vendor Specific Extended Capability ID (NEXT):** DevIdle has been assigned the Intel VSEC ID of 16h10.

16.1.36 SW LTR Pointer Register (HECI4_SWLTRPTR) - Offset ACh

Software Latency Tolerance Reporting (LTR) Pointer Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:22, F:5] + ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**SW LTR Update MMIO Offset Location (SWLTRLOC):** This register contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR. The value of this register is not valid, if the Valid bit is not set.
3:1	0h RO	**Base Address Register Number (BARNUM):** Contains the 0's based AR Number of the BAR which contains the location of the SW LTR MMIO register. When counting BAR Numbers, all BARs, regardless of size and type, consume one BAR Number. Bar 0 is the 1st BAR. The value of this register is not valid, if the Valid bit is not set.
0	0h RO	**VALID:** Set to 1'b1 to indicate that the function has implemented a SW LTR register as specified in the DevIdle that can be located using the SWLTRLOC register and BARNUM. Set to 1'b0 to indicate that the function has not implemented a SW LTR register that is compliant to the DevIdle definition. This could be because the function has not implemented SW LTR at all, or has a device specific version of SW LTR.

16.1.37 Device Idle Pointer Register (HECI4_DEVIDLEPTR) - Offset B0h

Device Idle Pointer Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:22, F:5] + B0h	00008001h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000800h RO	**Device Idle MMIO Offset Location (DEVIDLELOC):** This register contains the location pointer to the DevIdle register in MMIO space, as an offset from the specified BAR. The value of this register is not valid, if the Valid bit is not set.
3:1	0h RO	**Base Address Register Number (BARNUM):** Contains the 0's based AR Number of the BAR which contains the location of the SW LTR MMIO register. When counting BAR Numbers, all BARs, regardless of size and type, consume one BAR Number. Bar 0 is the 1st BAR. The value of this register is not valid, if the Valid bit is not set.
0	1h RO	**VALID:** Set to 1'b1 to indicate that the function has implemented a SW LTR register as specified DevIdle that can be located using the DEVIDLELOC register and BARNUM. Set to 1'b0 to indicate that the function has not implemented a DevIdle register that is compliant to the DevIdle definition. This could be because the function has not implemented SW LTR at all, or has a device specific version of device idle.

16.1.38 Device Idle Power On Latency (HECI4_DEVIDLEPOL) - Offset B4h

Device Idle Power On Latency

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:22, F:5] + B4h	0D38h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**Reserved**
12:10	3h RW/O	**Power On Latency Scale (POLS):** Latency Scale multiplier: 010: 1us 011: 32us All other settings are reserved (not enforced by HW). The value of this register is multiplied with the Power On Latency Value (POLV) to provide the DevIdle power on exit latency multiplier scale from 1us to 32ms. This register is defined to be RWO (read-write-once) to allow BIOS to set the initial value. This register is undefined if the device idle valid bit is 1'b0.
9:0	138h RW/O	**Power On Latency Value (POLV):** 10-bit value that is multiplied by the Power On Latency Scale. A value of 0 indicates a power on latency of less than 1us. This register is defined to be RWO (read-write-once) to allow BIOS to set the initial value. This register is undefined if the device idle valid bit is 1'b0.

16.1.39 DevIdle Power Control Enabled Register (HECI4_PWRCTRLEN) - Offset B6h

DevIdle Power Control Enabled Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:22, F:5] + B6h	000Eh

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RO	**Hardware Autonomous Enable (HAE):** CSE does not support autonomous power gating on idle.
4	0h RO	**Reserved**
3	1h RO	**Sleep Enable (SE):** CSE always asserts the sleep signal during power gating.
2	1h RO	**D3-Hot Enable (D3HEN):** CSE could power gate when idle and the PMCSR[1:0] register in the function =2'b11 (D3).
1	1h RO	**DEVIDLE Enable (DEVIDLEN):** CSE could power gate when idle and the DevIdle register (DevIdleC[2] = 1'b1) is set.
0	0h RO	**PMC Request Enable (PMCRE):** CSE will not power gate due to pmc_ip_sw_pg_req_b = LOW.

16.1.40 Manufacturer's ID (HECI4_MANID) - Offset F8h

Manufacturer's ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:22, F:5] + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/P	**Manufacturers ID Field (MANID)**: Manufacturer ID: Default value comes from straps

16.2 HECI Memory Mapped Registers Summary

Table 16-2. Summary of HECI Memory Mapped Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Host CB Write Window (HECI4_H_CB_WW)	00000000h
4h	4	Host Control And Status Register (HECI4_H_CSR)	80000000h
8h	4	CSE Circular Buffer Read Window (HECI4_CSE_CB_RW)	FFFFFFFFh
Ch	4	CSE Control And Status Register Host Access (HECI4_CSE_CSR_HA)	80000000h
800h	4	DEVIDLE Control (HECI4_DEVIDLEC)	00000010h

16.2.1 Host CB Write Window (HECI4_H_CB_WW) - Offset 0h

This register is for host to write into its Circular Buffer

Type	Size	Offset	Default
MMIO	32 bit	HECI_MMIO_MBAR + 0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**Host Circular Buffer Write Window Field (H_CB_WWF):** This field is for host to write into its circular buffer. This field is write only, reads will return arbitrary data. Writes to this register will increment the H_CBWP as long as CSE_RDY is 1. When CSE_RDY is 0, writes to this register have no effect and are not delivered to the H_CB, nor is H_CBWP incremented.

16.2.2 Host Control And Status Register (HECI4_H_CSR) - Offset 4h

This register reports status information about the host circular buffer (H_CB) and allows host software to control interrupt generation.

Note to software: Reserved bits in this register must be set to 0 whenever this register is written.

Type	Size	Offset	Default
MMIO	32 bit	HECI_MMIO_MBAR + 4h	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	80h RO	**Host Circular Buffer Depth (H_CBD):** This field indicates the maximum number of 32 bit entries available in the host circular buffer (H_CB). Host software uses this field along with the H_CBRP and H_CBWP fields to calculate the number of valid entries in the H_CB to read or number of entries available for write. Programmer's note: This field is implemented with a '1-hot' scheme. Only one bit will be set to a '1' at a time. Each bit position represents the value n of a buffer depth of (2^n). For example, when bit# 1 is 1, the buffer depth is 2; when bit#2 is 1, the buffer depth is 4, etc. **This field is hardwired to represent** a depth of 128 entries.
23:16	00h RO/V	**Host CB Write Pointer (H_CBWP):** Points to next location in the H_CB for host to write the data. Software uses this field along with H_CBRP and H_CBD fields to calculate the number of valid entries in the H_CB to read or number of entries available for write.
15:8	00h RO/V	**Host CB Read Pointer (H_CBRP):** Points to next location in the H_CB where a valid data is available for embedded controller to read. Software uses this field along with H_CBWR and H_CBD fields to calculate the number of valid entries in the host CB to read or number of entries available for write.
7	0h RO	**Reserved**
6	0h RW/1C/V	**Host DEVIDLEC Interrupt Status (H_DEVIDLEC_IS):** HW sets this bit to 1 when DEVIDLEC.IR is set and DEVIDLEC.CIP transitions from 1 to 0. Host clears this bit to 0 by writing a 1 to this bit position. H_DEVIDLEC_IE has no effect on this bit.
5	0h RW	**Host DEVIDLEC Interrupt Enable (H_DEVIDLEC_IE):** Host sets this bit to 1 to enable the host interrupt (MSI, INTx, SMI or SCI) to be asserted when H_DEVIDLEC_IS is set to 1.
4	0h RW	**Host Reset (H_RST):** Setting this bit to 1 will initiate the HECI reset sequence to get the circular buffers into a known good state for host and CSE communication. When this bit transitions from 0 to 1, hardware will clear the H_RDY and CSE_RDY bits.
3	0h RW/V	**Host Ready (H_RDY):** This bit indicates that the host is ready to process messages.
2	0h RW/V	**Host Interrupt Generate (H_IG):** Once message(s) are written into its CB, the host sets this bit to one for the HW to set the CSE_IS bit in the CSE_CSR and to generate an interrupt message to mIA. HW then clears this bit to 0.
1	0h RW/1C/V	**Host Interrupt Status (H_IS):** HW sets this bit to 1 when CSE_IG bit is set to 1. Host clears this bit to 0 by writing a 1 to this bit position. H_IE has no effect on this bit.
0	0h RW	**Host Interrupt Enable (H_IE):** Host sets this bit to 1 to enable the host interrupt (MSI, INTx, SMI or SCI) to be asserted when H_IS is set to 1.

16.2.3 CSE Circular Buffer Read Window (HECI4_CSE_CB_RW) - Offset 8h

This register is for host to read from the CSE Circular Buffer (CSE_CB)

Type	Size	Offset	Default
MMIO	32 bit	HECI_MMIO_MBAR + 8h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RO	**CSE Circular Buffer Read Window Field (CSE_CB_RWF):** This bit field is for host to read from the CSE Circular Buffer. This field is read only, writes have no effect. Reads to this register will increment the CSE_CBRP as long as CSE_RDY is 1. When CSE_RDY is 0, reads to this register have no effect, all 1s are returned, and CSE_CBRP is not incremented.

16.2.4 CSE Control And Status Register Host Access (HECI4_CSE_CSR_HA) - Offset Ch

This register allows host software to read the CSE Control Status register (CSE_CSR)

Type	Size	Offset	Default
MMIO	32 bit	HECI_MMIO_MBAR + Ch	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	80h RO	**CSE Circular Buffer Depth Host Read Access (CSE_CBD_HRA):** Host read access to CSE_CBD. **This field is hardwired to represent** A depth of 128 entries.
23:16	00h RO/V	**CSE CB Write Pointer Host Read Access (CSE_CBWP_HRA):** Host read only access to CSE_CBWP.
15:8	00h RO/V	**CSE CB Read Pointer Host Read Access (CSE_CBRP_HRA):** Host read only access to CSE_CBRP.
7	0h RO/V	**NMI Status Host Read Access (NMI_STS_HRA):** Host read access to NMI_STS.
6	0h RO	**Reserved**
5	0h RO/V	**Pointer Reset Host Read Access (PTR_RST_HRA):** Host read access to PTR_RST.
4	0h RO/V	**CSE Reset Host Read Access (CSE_RST_HRA):** Host read access to CSE_RST.
3	0h RO/V	**CSE Ready Host Read Access (CSE_RDY_HRA):** Host read access to CSE_RDY.
2	0h RO/V	**CSE Interrupt Generate Host Read Access (CSE_IG_HRA):** Host read only access to CSE_IG.
1	0h RO/V	**CSE Interrupt Status Host Read Access (CSE_IS_HRA):** Host read only access to CSE_IS.
0	0h RO/V	**CSE Interrupt Enable Host Read Access (CSE_IE_HRA):** Host read only access to CSE_IE.

16.2.5 DEVIDLE Control (HECI4_DEVIDLEC) - Offset 800h

This register allows host to configure the power mode using D0i0/D0i3 support

Type	Size	Offset	Default
MMIO	32 bit	HECI_MMIO_MBAR + 800h	00000010h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	1h RO	**Interrupt Request Capable (IRC):** Set to be always 1'b1 since CSE is capable of generating an interrupt on command completion.
3	0h RO	**Restore Required (RR):** When this bit is set (by HW), SW must restore the state of the IP. This bit is cleared by SW writing a 1. **In CSE this bit is never set so it does not need to be** cleared by SW.
2	0h RW	**DEVIDLE:** SW sets this bit to 1'b1 to move the function into the DevIdle state. Writing this bit to 1'b0 will return the function to the fully active D0 state (D0i0). When this bit changes state, mIA may be interrupted (see H_PCI_CSR.DEVIDLEC_IS register's description).
1	0h RW	**Interrupt Request (IR):** SW sets this bit to 1'b1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register. When this bit is set to 1'b1, Command-in-Progress deassertion is captured in H_CSR. H_DEVIDLEC_IS. If H_CSR.H_DEVIDLEC_IE is 1b1 as well, host interrupt will be initiated.
0	0h RO/V	**CIP:** HW sets this bit on a 1'b1->1'b0 or 1'b0->1'b1 transition of DEVIDLE. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. HW clears this bit when CSE FW clears its own DevIdle interrupt status bit indicating completion of the DevIdle transition command. When clear, all the other bits in the register are valid and SW may write to any bit. If Interrupt Request (IR) was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect.

17 USB eXtensible Host Controller Interface (xHCI)

17.1 xHCI Configuration Registers Summary

This chapter records the registers in Bus: 0, Device 20, Function 0.

Table 17-1. Summary of Bus: 0, Device: 20, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	Vendor ID (VID)	8086h
2h	2	Device ID (DID)	4B7Dh
4h	2	Command Reg (CMD)	0000h
6h	2	Device Status (STS)	0290h
8h	1	Revision ID (RID)	00h
9h	1	Programming Interface (PI)	30h
Ah	1	Sub Class Code (SCC)	03h
Bh	1	Base Class Code (BCC)	0Ch
Dh	1	Master Latency Timer (MLT)	00h
Eh	1	Header Type (HT)	80h
10h	8	Memory Base Address (MBAR)	0000000000000004h
2Ch	2	USB Subsystem Vendor ID (SSVID)	0000h
2Eh	2	USB Subsystem ID (SSID)	0000h
34h	1	Capabilities Pointer (CAP_PTR)	70h
3Ch	1	Interrupt Line (ILINE)	00h
3Dh	1	Interrupt Pin (IPIN)	00h
58h	4	Audio Time Synchronization (AUDSYNC)	00000000h
60h	1	Serial Bus Release Number (SBRN)	31h
61h	1	Frame Length Adjustment (FLADJ)	60h
62h	1	Best Effort Service Latency (BESL)	00h
70h	1	PCI Power Management Capability ID (PM_CID)	01h
71h	1	Next Item Pointer 1 (PM_NEXT)	80h
72h	2	Power Management Capabilities (PM_CAP)	C1C2h
74h	2	Power Management Control/Status (PM_CS)	0008h
80h	1	Message Signaled Interrupt CID (MSI_CID)	05h
81h	1	Next Item Pointer (MSI_NEXT)	90h
82h	2	Message Signaled Interrupt Message Control (MSI_MCTL)	0086h
84h	4	Message Signaled Interrupt Message Address (MSI_MAD)	00000000h
88h	4	Message Signaled Interrupt Upper Address (MSI_MUAD)	00000000h
8Ch	2	Message Signaled Interrupt Message Data (MSI_MD)	0000h
A4h	4	High Speed Configuration 2 (HSCFG2)	00003800h

17.1.1 Vendor ID (VID) - Offset 0h

Vendor ID.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:20, F:0] + 0h	8086h

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**Vendor ID (VID):** Vendor ID

17.1.2 Device ID (DID) - Offset 2h

Device ID.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:20, F:0] + 2h	4B7Dh

Bit Range	Default & Access	Field Name (ID): Description
15:0	4B7Dh RO/V	**Device ID (DID):** See Global Device ID table for value

17.1.3 Command Reg (CMD) - Offset 4h

Command Reg.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:20, F:0] + 4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable (INTR_DIS):** When cleared to 0, the function is capable of generating interrupts. When 1, the function cannot generate its interrupt to the interrupt controller. Note that the corresponding Interrupt Status bit is not affected by the interrupt enable.
9	0h RO	**Fast Back to Back Enable (FBE):** Fast Back to Back Enable
8	0h RW	**SERR# Enable (SERR):** When set to 1, the XHC is capable of generating (internally) SERR#.
7	0h RO	**Wait Cycle Control (WCC):** Wait Cycle Control
6	0h RW	**Parity Error Response (PER):** When set to 1, the XHCI Host Controller will check for correct parity (on its internal interface) and halt operation when bad parity is detected during the data phase as recommended by the XHCI specification. Note that this applies to both requests and completions from the system interface. This bit must be set in order for the parity errors to generate SERR#.
5	0h RO	**VGA Palette Snoop (VPS):** VGA Palette Snoop

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**Memory Write Invalidate (MWI):** Memory Write Invalidate
3	0h RO	**Special Cycle Enable (SCE):** Special Cycle Enable
2	0h RW	**Bus Master Enable (BME):** When set, it allows XHC to act as a bus master. When cleared, it disables XHC from initiating transactions on the system bus.
1	0h RW	**Memory Space Enable (MSE):** This bit controls access to the XHC Memory Space registers. If this bit is set, accesses to the XHC registers are enabled. The Base Address register for the XHC should be programmed before this bit is set.
0	0h RO	**I/O Space Enable (IOSE):** Reserved

17.1.4 Device Status (STS) - Offset 6h

Device Status.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:20, F:0] + 6h	0290h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**Detected Parity Error (DPE):** This bit is set by the Intel PCH whenever a parity error is seen on the internal interface to the XHC host controller, regardless of the setting of bit 6 or bit 8 in the Command register or any other conditions. Software clears this bit by writing a 1 to this bit location.
14	0h RW/1C	**Signaled System Error (SSE):** This bit is set by the Intel PCH whenever it signals SERR# (internally). The SERR_EN bit (bit 8 in the Command Register) must be 1 for this bit to be set. Software clears this bit by writing a 1 to this bit location.
13	0h RW/1C	**Received Master-Abort Status (RMA):** This bit is set when XHC, as a master, receives a master-abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location.
12	0h RW/1C	**Received Target Abort Status (RTA):** This bit is set when XHC, as a master, receives a target abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location.
11	0h RW/1C	**Signaled Target-Abort Status (STA):** This bit is used to indicate when the XHC function responds to a cycle with a target abort.
10:9	1h RO	**DEVSEL# Timing Status (DEVT):** This 2-bit field defines the timing for DEVSEL# assertion. Read-Only.
8	0h RW/1C	**Master Data Parity Error Detected (MDPED):** This bit is set by the Intel PCH whenever a data parity error is detected on an XHC read completion packet on the internal interface to the XHC host controller and bit 6 of the Command register is set to 1. Software clears this bit by writing a 1 to this bit location.

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Fast Back-to-Back Capable (FBBC):** Reserved
6	0h RO	**User Definable Features (UDF):** Reserved
5	0h RO	**66 MHz Capable (MC):** Reserved
4	1h RO	**Capabilities List (CL):** Hardwired to 1 indicating that offset 34h contains a valid capabilities pointer.
3	0h RO/V	**Interrupt Status (INTR_STS):** This read-only bit reflects the state of this function's interrupt at the input of the enable/disable logic. This bit is a 1 when the interrupt is asserted. This bit will be 0 when the interrupt is deasserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
2:0	0h RO	**Reserved**

17.1.5 Revision ID (RID) - Offset 8h

Revision ID.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:20, F:0] + 8h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO/V	**Revision ID (RID)**

17.1.6 Programming Interface (PI) - Offset 9h

Programming Interface.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:20, F:0] + 9h	30h

Bit Range	Default & Access	Field Name (ID): Description
7:0	30h RO	**Programming Interface (PI):** A value of 30h indicates that this USB Host Controller conforms to the XHCI specification.

17.1.7 Sub Class Code (SCC) - Offset Ah

Sub Class Code.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:20, F:0] + Ah	03h

Bit Range	Default & Access	Field Name (ID): Description
7:0	03h RO	**Sub Class Code (SCC):** A value of 03h indicates that this is a Universal Serial Bus Host Controller.

17.1.8 Base Class Code (BCC) - Offset Bh

Base Class Code.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:20, F:0] + Bh	0Ch

Bit Range	Default & Access	Field Name (ID): Description
7:0	0Ch RO	**Base Class Code (BCC):** A value of 0Ch indicates that this is a Serial Bus controller.

17.1.9 Master Latency Timer (MLT) - Offset Dh

Master Latency Timer.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:20, F:0] + Dh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Master Latency Timer (MLT):** Because the XHC controller is internally implemented with arbitration on an internal interface, it does not need a master latency timer. The bits will be fixed at 0.

17.1.10 Header Type (HT) - Offset Eh

Header Type.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:20, F:0] + Eh	80h

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Multi-Function Bit (MFB):** Read only indicating single function device.
6:0	00h RO	**Configuration layout (CL):** Hardwired to 0 to indicate a standard PCI configuration layout.

17.1.11 Memory Base Address (MBAR) - Offset 10h

Value in this register will be different after the enumeration process.

Type	Size	Offset	Default
PCI	64 bit	[B:0, D:20, F:0] + 10h	0000000000000004h

Bit Range	Default & Access	Field Name (ID): Description
63:16	0000000000000h RW	**Base Address (BA):** Bits (63:16) correspond to memory address signals (63:16), respectively. This gives 64 KB of relocatable memory space aligned to 64 KB boundaries.
15:4	0h RO	**Reserved**
3	0h RO	**PREFETCHABLE:** This bit is hardwired to 0 indicating that this range should not be prefetched.
2:1	2h RO	**MBAR_TYPE:** If this field is hardwired to 00 it indicates that this range can be mapped anywhere within 32-bit address space. If this field is hardwired to 10 it indicates that this range can be mapped anywhere within 64-bit address space.
0	0h RO	**Resource Type Indicator (RTE):** This bit is hardwired to 0 indicating that the base address field in this register maps to memory space

17.1.12 USB Subsystem Vendor ID (SSVID) - Offset 2Ch

This register is modified and maintained by BIOS.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:20, F:0] + 2Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/L	**USB Subsystem Vendor ID (SSVID):** This register, in combination with the USB Subsystem ID register, enables the operating system to distinguish each subsystem from the others. Writes to this register are controlled by the Access Control bit (ACCTRL). **Locked by:** XHCC1.ACCTRL

17.1.13 USB Subsystem ID (SSID) - Offset 2Eh

This register is modified and maintained by BIOS.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:20, F:0] + 2Eh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/L	**USB Subsystem ID (SSID):** BIOS sets the value in this register to identify the Subsystem ID. This register, in combination with the Subsystem Vendor ID register, enables the operating system to distinguish each subsystem from other(s). Writes to this register are controlled by the Access Control bit (ACCTRL). **Locked by:** XHCC1.ACCTRL

17.1.14 Capabilities Pointer (CAP_PTR) - Offset 34h

Capabilities Pointer.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:20, F:0] + 34h	70h

Bit Range	Default & Access	Field Name (ID): Description
7:0	70h RO	**Capabilities Pointer (CAP_PTR):** This register points to the starting offset of the capabilities ranges.

17.1.15 Interrupt Line (ILINE) - Offset 3Ch

Interrupt Line.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:20, F:0] + 3Ch	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Interrupt Line (ILINE):** This data is not used by the Intel PCH. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to.

17.1.16 Interrupt Pin (IPIN) - Offset 3Dh

This register is modified and maintained by BIOS.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:20, F:0] + 3Dh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/L	**Interrupt pin (IPIN):** Bits 7:0 reflect the Interrupt Pin assigned to the host controller by the platform (and are hardwired). **Locked by:** XHCC1.ACCTRL

17.1.17 Audio Time Synchronization (AUDSYNC) - Offset 58h

This 32 bit register is used for audio stream synchronization across different devices. Global signal sample_now captures a value in AUDSYNC register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:0] + 58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO/V	**Captured Frame List Current Index/Frame Number (CMFI):** The value in this register is updated in response to sample_now signal. Bits (29:16) reflect state of bits (13:0) of FRINDEX
15:13	0h RO	**Reserved**
12:0	0000h RO/V	**Captured Micro-frame BLIF (CMFB):** The value is updated in response to sample_now signal and provides information about offset within micro-frame. Captured value represents number of 8 high-speed bit time units from start of micro-frame. At the beginning of micro-frame captured value will be 0 and increase to maximum value at the end. Default maximum value is 7499 but it may be changed as result of adjustment done in FLA.

17.1.18 Serial Bus Release Number (SBRN) - Offset 60h

Serial Bus Release Number.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:20, F:0] + 60h	31h

Bit Range	Default & Access	Field Name (ID): Description
7:0	31h RO	**Serial Bus Release Number (SBRN):** A value of 30h indicates that this controller follows USB release 3.0.

17.1.19 Frame Length Adjustment (FLADJ) - Offset 61h

This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written into these six bits, the length of the frame is adjusted. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. This register should only be modified when the HChalted bit in the USBSTS register is a one. Changing value of this register while the host controller is operating yields undefined results.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:20, F:0] + 61h	60h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6	1h RO	**No Frame Length Timing Capability (NO_FRAME_LENGTH_TIMING_CAP):** This flag is set to 1 to indicate that the host controller does not support a programmable Frame Length Timing Value field.
5:0	20h RO	**Frame Length Timing Value (FLTV):** SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (number of High Speed bit times) FLADJ Value (decimal) (decimal) 59488 0 (00h) 59504 1 (01h) 59520 2 (02h) ... 59984 31 (1Fh) 60000 32 (20h) ... 60480 62 (3Eh) 60496 63 (3Fh) Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (# High Speed bit times) FLADJ Value

17.1.20 Best Effort Service Latency (BESL) - Offset 62h

Best Effort Service Latency.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:20, F:0] + 62h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RW/L	**Default Best Effort Service Latency Deep (DBESLD):** Default Best Effort Service Latency (DBESLD) If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESLD field. This is programmed by BIOS based on platform parameters. **Locked by:** XHCC1.ACCTRL
3:0	0h RW/L	**Default Best Effort Service Latency (DBESL):** If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESL field. This is programmed by BIOS based on platform parameters. **Locked by:** XHCC1.ACCTRL

17.1.21 PCI Power Management Capability ID (PM_CID) - Offset 70h

PCI Power Management Capability ID.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:20, F:0] + 70h	01h

Bit Range	Default & Access	Field Name (ID): Description
7:0	01h RO	**PCI Power Management Capability ID (PM_CID):** A value of 01h indicates that this is a PCI Power Management capabilities field.

17.1.22 Next Item Pointer 1 (PM_NEXT) - Offset 71h

This register is modified and maintained by BIOS.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:20, F:0] + 71h	80h

Bit Range	Default & Access	Field Name (ID): Description
7:0	80h RW/L	**Next Item Pointer 1 (PM_NEXT):** This register defaults to 80h, which indicates that the next capability registers begin at configuration offset 80h. This register is writable when the Access Control bit is set to '0'. This allows BIOS to effectively hide the next capability registers, if necessary. This register should only be written during system initialization before the plug-and-play software has enabled any master-initiated traffic. Values of: 80h implies next capability is MSI 00h implies that MSI capability is hidden. Note: This value is never expected to be programmed. **Locked by:** XHCC1.ACCTRL

17.1.23 Power Management Capabilities (PM_CAP) - Offset 72h

Normally, this register is read-only to report capabilities to the power management software. In order to report different power management capabilities depending on the system in which the Intel PCH is used, the write access to this register is controlled by the Access Control bit (ACCTRL). The value written to this register does not affect the hardware other than changing the value returned during a read.

This register is modified and maintained by BIOS.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:20, F:0] + 72h	C1C2h

Bit Range	Default & Access	Field Name (ID): Description
15:11	18h RW/L	**PME_SUPPORT:** This 5-bit field indicates the power states in which the function may assert PME#. The Intel PCH XHC does not support the D1 or D2 states. For all other states, the Intel PCH XHC is capable of generating PME#. Software should never need to modify this field. However, the ability to change this field may prove useful for some systems. **Locked by:** XHCC1.ACCTRL
10	0h RW/L	**D2_SUPPORT:** The D2 state is not supported. **Locked by:** XHCC1.ACCTRL
9	0h RW/L	**D1_SUPPORT:** The D1 state is not supported. **Locked by:** XHCC1.ACCTRL
8:6	7h RW/L	**AUX_CURRENT:** The Intel PCH XHC reports 375mA maximum Suspend well current required when in the D3cold state. This value can be written by BIOS when a more accurate value is known. **Locked by:** XHCC1.ACCTRL
5	0h RW/L	**DSI:** The Intel PCH reports 0, indicating that no device-specific initialization is required. **Locked by:** XHCC1.ACCTRL
4	0h RO	**Reserved**
3	0h RW/L	**PME Clock (PMECLOCK):** The Intel PCH reports 0, indicating that no PCI clock is required to generate PME#. **Locked by:** XHCC1.ACCTRL
2:0	2h RW/L	**VERSION:** The Intel PCH reports 010, indicating that it complies with Revision 1.1 of the PCI Power Management Specification. **Locked by:** XHCC1.ACCTRL

17.1.24 Power Management Control/Status (PM_CS) - Offset 74h

Power Management Control/Status.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:20, F:0] + 74h	0008h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**PME_STATUS:** This bit is set when the Intel PCH XHC would normally assert the PME# signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the internal PME to deassert (if enabled). Writing a 0 has no effect. This bit must be explicitly cleared by the operating system each time the operating system is loaded.
14:13	0h RO	**DATA_SCALE:** The Intel PCH hardwires these bits to 00 because it does not support the associated Data register.
12:9	0h RO	**DATA_SELECT:** The Intel PCH hardwires these bits to 0000 because it does not support the associated Data register.
8	0h RW	**PME_EN:** A 1 enables the Intel PCH XHC to generate an internal PME signal when PME_Status is 1. This bit must be explicitly cleared by the operating system each time it is initially loaded.
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset (NSR):** No_Soft_Reset - When set ("1"), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. Transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	**Reserved**
1:0	0h RW	**POWERSTATE:** This 2-bit field is used both to determine the current power state of XHC function and to set a new power state. The definitions of the field values are: 00b - D0 state 11b - D3hot state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3hot state, the Intel PCH must not accept accesses to the XHC memory range, but the configuration space must still be accessible. Software should wait for 100ms before requesting the xHCI controller to re-enter D3 after a D3 exit.

17.1.25 Message Signaled Interrupt CID (MSI_CID) - Offset 80h

Message Signaled Interrupt CID.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:20, F:0] + 80h	05h

Bit Range	Default & Access	Field Name (ID): Description
7:0	05h RO	**Capability ID (CID):** Indicates that this is an MSI capability

17.1.26 Next Item Pointer (MSI_NEXT) - Offset 81h

Next Item Pointer.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:20, F:0] + 81h	90h

Bit Range	Default & Access	Field Name (ID): Description
7:0	90h RW/L	**Next Pointer (NEXT_POINTER):** Indicates that this is the last item on the capability list **Locked by:** XHCC1.ACCTRL

17.1.27 Message Signaled Interrupt Message Control (MSI_MCTL) - Offset 82h

Message Signaled Interrupt Message Control.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:20, F:0] + 82h	0086h

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	**Reserved**
8	0h RO	**Per-Vector Masking Capable (PVM):** Specifies whether controller supports MSI per vector masking. Not supported
7	1h RO	**64 Bit Address Capable (C64):** Specifies whether capable of generating 64-bit messages. This device is 64-bit capable.

Bit Range	Default & Access	Field Name (ID): Description
6:4	0h RW	**Multiple Message Enable (MME):** Indicates the number of messages the controller should assert. This device supports multiple message MSI.
3:1	3h RO	**Multiple Message Capable (MMC):** Indicates the number of messages the controller wishes to assert. This field must be set by HW to reflect the number of Interrupters supported. Encoding number of Vectors requested (number of Interrupters) 000 1 001 2 010 4 011 8 100 16 101 32 110-111 Reserved
0	0h RW	**MSI Enable (MSIE):** If set to 1, MSI is enabled and the traditional interrupt pins are not used to generate interrupts. If cleared to 0, MSI operation is disabled and the traditional interrupt pins are used.

17.1.28 Message Signaled Interrupt Message Address (MSI_MAD) - Offset 84h

Message Signaled Interrupt Message Address.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:0] + 84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**ADDR:** Lower DW of system specified message address, always DWORD aligned
1:0	0h RO	**Reserved**

17.1.29 Message Signaled Interrupt Upper Address (MSI_MUAD) - Offset 88h

Message Signaled Interrupt Upper Address.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:0] + 88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Upper Addr (UPPERADDR):** Upper DW of system specified message address.

17.1.30 Message Signaled Interrupt Message Data (MSI_MD) - Offset 8Ch

Message Signaled Interrupt Message Data.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:20, F:0] + 8Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**DATA:** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD(15:0)) during the data phase of the MSI memory write transaction. The Multiple Message Enable field (bits 6-4 of the Message Control register) defines the number of low order message data bits the function is permitted to modify to generate its system software allocated vectors. For example, a Multiple Message Enable encoding of 010 indicates the function has been allocated four vectors and is permitted to modify message data bits 1 and 0 (a function modifies the lower message data bits to generate the allocated number of vectors). If the Multiple Message Enable field is 000, the function is not permitted to modify the message data.

17.1.31 High Speed Configuration 2 (HSCFG2) - Offset A4h

High Speed Configuration 2.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:0] + A4h	00003800h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW	**PORT1_HOST_MODE_OVERRIDE:** When set, this bit causes the Host_Device mux on port 1 to be forced into the Host mode.
17:16	0h RW	**EUSB2SEL:** The two bits are associate with USB2 ports 1 - bit 16 and 2 - bit 2 0: Port is mapped to USB2 1: Port is mapped to eUSB2

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**HS ASYNC Active IN Mask (HSAAIM):** Determines if the Async Active will mask/ignore IN EP s. 0 HS ASYNC Active will include IN EP s. 1 HS ASYNC Active will mask/ignore IN EP s.
14	0h RW	**HS OUT ASYNC Active Polling EP Mask (HSOAAPEPM):** Determines if the Async Active for OUT HS/FS/LS masks/ignores EP s that are polling/PINGing (HS) due to NAK. 0 HS OUT ASYNC Active will include EP s that are polling. 1 HS OUT ASYNC Active will mask/ignore EP s that are polling.
13	1h RW	**HS IN ASYNC Active Polling EP Mask (HSIAAPEPM):** Determines if the Async Active for IN HS/FS/LS masks/ignores EP s that are polling due to NAK. 0 HS IN ASYNC Active will include EP s that are polling. 1 HS IN ASYNC Active will mask/ignore EP s that are polling.
12:11	3h RW	**HS INTR IN Periodic Active Policy Control (HSIIPAPC):** Controls how the HS INTR IN periodic active is used to generate the global periodic active. This will determine how the smallest service interval among active EP s and number of active EP s are used. 0 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold OR Numb of EP Threshold values meet the requirement. 1 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold AND Numb of EP Threshold values meet the requirement. 2 Always allow HS INTR EP s to be used in the generation of the global Periodic Active indication. 3 Never allow HS INTR EP s to be used in the generation of the global Periodic Active indication.
10:4	00h RW	**HS INTR IN Periodic Active Num of EP Threshold (HSIIPANEPT):** Defines the threshold used to determine if Periodic Active may include HS/FS/LS INTR IN EP active indication. If there are more than NumEPThreshold active HS/FS/LS INTR EP s then they may be included as part of the periodic active generation.
3:0	0h RW	**HS INTR IN Periodic Active Service Interval Threshold (HSIIPASIT):** Defines the Service Interval threshold used to determine if Periodic Active will include HS/FS/LS INTR IN EP active indication. If there are any active HS/FS/LS INTR EP s with a service interval less than or equal to this threshold then they may be included as part of the periodic active generation.

17.2 xHCI Memory Mapped Registers Summary

Table 17-2. Summary of xHCI Memory Mapped Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	1	Capability Registers Length (CAPLENGTH)	80h
2h	2	Host Controller Interface Version Number (HCIVERSION)	0110h
4h	4	Structural Parameters 1 (HCSPARAMS1)	10000840h
8h	4	Structural Parameters 2 (HCSPARAMS2)	14200054h
Ch	4	Structural Parameters 3 (HCSPARAMS3)	00A0000Ah
10h	4	Capability Parameters (HCCPARAMS)	20007FC1h
14h	4	Doorbell Offset (DBOFF)	00003000h
18h	4	Runtime Register Space Offset (RTSOFF)	00002000h
80h	4	USB Command (USBCMD)	00000000h
84h	4	USB Status (USBSTS)	00000001h
88h	4	Page Size (PAGESIZE)	00000001h
94h	4	Device Notification Control (DNCTRL)	00000000h
98h	4	Command Ring Low (CRCR_LO)	00000000h
9Ch	4	Command Ring High (CRCR_HI)	00000000h
B0h	4	Device Context Base Address Array Pointer Low (DCBAAP_LO)	00000000h
B4h	4	Device Context Base Address Array Pointer High (DCBAAP_HI)	00000000h
B8h	4	Configure Reg (CONFIG)	00000000h
480h	4	Port Status AndControl USB2 (PORTSC1)	000002A0h
484h	4	Port Power Management Status Aand Control USB2 (PORTPMSC1)	00000000h
48Ch	4	Port X Hardware LPM Control Register (PORTHLPMC1)	00000000h
2000h	4	Microframe Index (RTMFINDEX)	00000000h
2020h	4	Interrupter Management (IMAN0)	00000000h
2024h	4	Interrupter Moderation (IMOD0)	00000FA0h
2028h	4	Event Ring Segment Table Size (ERSTSZ0)	00000000h
2030h	4	Event Ring Segment Table Base Address Low (ERSTBA_LO0)	00000000h
2034h	4	Event Ring Segment Table Base Address High (ERSTBA_HI0)	00000000h
2038h	4	Event Ring Dequeue Pointer Low (ERDP_LO0)	00000000h
203Ch	4	Event Ring Dequeue Pointer High (ERDP_HI0)	00000000h
2040h	4	Interrupter Management (IMAN1)	00000000h
2044h	4	Interrupter Moderation (IMOD1)	00000FA0h
2048h	4	Event Ring Segment Table Size (ERSTSZ1)	00000000h
2050h	4	Event Ring Segment Table Base Address Low (ERSTBA_LO1)	00000000h
2054h	4	Event Ring Segment Table Base Address High (ERSTBA_HI1)	00000000h
2058h	4	Event Ring Dequeue Pointer Low (ERDP_LO1)	00000000h
205Ch	4	Event Ring Dequeue Pointer High (ERDP_HI1)	00000000h
2060h	4	Interrupter Management (IMAN2)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2064h	4	Interrupter Moderation (IMOD2)	00000FA0h
2068h	4	Event Ring Segment Table Size (ERSTSZ2)	00000000h
2070h	4	Event Ring Segment Table Base Address Low (ERSTBA_LO2)	00000000h
2074h	4	Event Ring Segment Table Base Address High (ERSTBA_HI2)	00000000h
2078h	4	Event Ring Dequeue Pointer Low (ERDP_LO2)	00000000h
207Ch	4	Event Ring Dequeue Pointer High (ERDP_HI2)	00000000h
2080h	4	Interrupter Management (IMAN3)	00000000h
2084h	4	Interrupter Moderation (IMOD3)	00000FA0h
2088h	4	Event Ring Segment Table Size (ERSTSZ3)	00000000h
2090h	4	Event Ring Segment Table Base Address Low (ERSTBA_LO3)	00000000h
2094h	4	Event Ring Segment Table Base Address High (ERSTBA_HI3)	00000000h
2098h	4	Event Ring Dequeue Pointer Low (ERDP_LO3)	00000000h
209Ch	4	Event Ring Dequeue Pointer High (ERDP_HI3)	00000000h
20A0h	4	Interrupter Management (IMAN4)	00000000h
20A4h	4	Interrupter Moderation (IMOD4)	00000FA0h
20A8h	4	Event Ring Segment Table Size (ERSTSZ4)	00000000h
20B0h	4	Event Ring Segment Table Base Address Low (ERSTBA_LO4)	00000000h
20B4h	4	Event Ring Segment Table Base Address High (ERSTBA_HI4)	00000000h
20B8h	4	Event Ring Dequeue Pointer Low (ERDP_LO4)	00000000h
20BCh	4	Event Ring Dequeue Pointer High (ERDP_HI4)	00000000h
20C0h	4	Interrupter Management (IMAN5)	00000000h
20C4h	4	Interrupter Moderation (IMOD5)	00000FA0h
20C8h	4	Event Ring Segment Table Size (ERSTSZ5)	00000000h
20D0h	4	Event Ring Segment Table Base Address Low (ERSTBA_LO5)	00000000h
20D4h	4	Event Ring Segment Table Base Address High (ERSTBA_HI5)	00000000h
20D8h	4	Event Ring Dequeue Pointer Low (ERDP_LO5)	00000000h
20DCh	4	Event Ring Dequeue Pointer High (ERDP_HI5)	00000000h
20E0h	4	Interrupter Management (IMAN6)	00000000h
20E4h	4	Interrupter Moderation (IMOD6)	00000FA0h
20E8h	4	Event Ring Segment Table Size (ERSTSZ6)	00000000h
20F0h	4	Event Ring Segment Table Base Address Low (ERSTBA_LO6)	00000000h
20F4h	4	Event Ring Segment Table Base Address High (ERSTBA_HI6)	00000000h
20F8h	4	Event Ring Dequeue Pointer Low (ERDP_LO6)	00000000h
20FCh	4	Event Ring Dequeue Pointer High (ERDP_HI6)	00000000h
2100h	4	Interrupter Management (IMAN7)	00000000h
2104h	4	Interrupter Moderation (IMOD7)	00000FA0h
2108h	4	Event Ring Segment Table Size (ERSTSZ7)	00000000h
2110h	4	Event Ring Segment Table Base Address Low (ERSTBA_LO7)	00000000h
2114h	4	Event Ring Segment Table Base Address High (ERSTBA_HI7)	00000000h
2118h	4	Event Ring Dequeue Pointer Low (ERDP_LO7)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
211Ch	4	Event Ring Dequeue Pointer High (ERDP_HI7)	00000000h
3000h	4	Door Bell (DB0)	00000000h
3004h	4	Door Bell (DB1)	00000000h
3008h	4	Door Bell (DB2)	00000000h
300Ch	4	Door Bell (DB3)	00000000h
3010h	4	Door Bell (DB4)	00000000h
3014h	4	Door Bell (DB5)	00000000h
3018h	4	Door Bell (DB6)	00000000h
301Ch	4	Door Bell (DB7)	00000000h
3020h	4	Door Bell (DB8)	00000000h
3024h	4	Door Bell (DB9)	00000000h
3028h	4	Door Bell (DB10)	00000000h
302Ch	4	Door Bell (DB11)	00000000h
3030h	4	Door Bell (DB12)	00000000h
3034h	4	Door Bell (DB13)	00000000h
3038h	4	Door Bell (DB14)	00000000h
303Ch	4	Door Bell (DB15)	00000000h
3040h	4	Door Bell (DB16)	00000000h
3044h	4	Door Bell (DB17)	00000000h
3048h	4	Door Bell (DB18)	00000000h
304Ch	4	Door Bell (DB19)	00000000h
3050h	4	Door Bell (DB20)	00000000h
3054h	4	Door Bell (DB21)	00000000h
3058h	4	Door Bell (DB22)	00000000h
305Ch	4	Door Bell (DB23)	00000000h
3060h	4	Door Bell (DB24)	00000000h
3064h	4	Door Bell (DB25)	00000000h
3068h	4	Door Bell (DB26)	00000000h
306Ch	4	Door Bell (DB27)	00000000h
3070h	4	Door Bell (DB28)	00000000h
3074h	4	Door Bell (DB29)	00000000h
3078h	4	Door Bell (DB30)	00000000h
307Ch	4	Door Bell (DB31)	00000000h
3080h	4	Door Bell (DB32)	00000000h
3084h	4	Door Bell (DB33)	00000000h
3088h	4	Door Bell (DB34)	00000000h
308Ch	4	Door Bell (DB35)	00000000h
3090h	4	Door Bell (DB36)	00000000h
3094h	4	Door Bell (DB37)	00000000h
3098h	4	Door Bell (DB38)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
309Ch	4	Door Bell (DB39)	00000000h
30A0h	4	Door Bell (DB40)	00000000h
30A4h	4	Door Bell (DB41)	00000000h
30A8h	4	Door Bell (DB42)	00000000h
30ACh	4	Door Bell (DB43)	00000000h
30B0h	4	Door Bell (DB44)	00000000h
30B4h	4	Door Bell (DB45)	00000000h
30B8h	4	Door Bell (DB46)	00000000h
30BCh	4	Door Bell (DB47)	00000000h
30C0h	4	Door Bell (DB48)	00000000h
30C4h	4	Door Bell (DB49)	00000000h
30C8h	4	Door Bell (DB50)	00000000h
30CCh	4	Door Bell (DB51)	00000000h
30D0h	4	Door Bell (DB52)	00000000h
30D4h	4	Door Bell (DB53)	00000000h
30D8h	4	Door Bell (DB54)	00000000h
30DCh	4	Door Bell (DB55)	00000000h
30E0h	4	Door Bell (DB56)	00000000h
30E4h	4	Door Bell (DB57)	00000000h
30E8h	4	Door Bell (DB58)	00000000h
30ECh	4	Door Bell (DB59)	00000000h
30F0h	4	Door Bell (DB60)	00000000h
30F4h	4	Door Bell (DB61)	00000000h
30F8h	4	Door Bell (DB62)	00000000h
30FCh	4	Door Bell (DB63)	00000000h
3100h	4	Door Bell (DB64)	00000000h
8004h	4	XECP SUPP USB2_1 (XECP_SUPP_USB2_1)	20425355h
800Ch	4	XECP SUPP USB3_3 (XECP_SUPP_USB2_3)	00000000h
8010h	4	XECP SUPP USB2_4 Full Speed (XECP_SUPP_USB2_4)	000C0021h
8014h	4	XECP_SUPP USB2_5 Low Speed (XECP_SUPP_USB2_5)	05DC0012h
8018h	4	XECP SUPP USB2_6 High Speed (XECP_SUPP_USB2_6)	01E00023h
8020h	4	XECP SUPP USB3_0 (XECP_SUPP_USB3_0)	03101402h
8024h	4	XECP SUPP USB3_1 (XECP_SUPP_USB3_1)	20425355h
8028h	4	XECP SUPP USB3_2 (XECP_SUPP_USB3_2)	8000040Dh
802Ch	4	XECP SUPP USB3_3 (XECP_SUPP_USB3_3)	00000000h
8030h	4	XECP SUPP USB3_4 (XECP_SUPP_USB3_4)	00050134h
8034h	4	XECP SUPP USB3_5 (XECP_SUPP_USB3_5)	000A4135h
8038h	4	XECP SUPP USB3_6 (XECP_SUPP_USB3_6)	04E00126h
803Ch	4	XECP SUPP USB3_7 (XECP_SUPP_USB3_7)	09C00127h
8040h	4	XECP SUPP USB3_8 (XECP_SUPP_USB3_8)	13800128h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8044h	4	XECP SUPP USB3_9 (XECP_SUPP_USB3_9)	05B10129h
8048h	4	XECP SUPP USB3_10 (XECP_SUPP_USB3_10)	0B63012Ah
804Ch	4	XECP SUPP USB3_11 (XECP_SUPP_USB3_11)	16C6012Bh
8094h	4	Host Control Scheduler (HOST_CTRL_SCH_REG)	00C08140h
80A4h	4	Power Management Control (PMCTRL_REG)	492D5094h
80B0h	4	Host Controller Misc Reg (HOST_CTRL_MISC_REG)	0080037Fh
80B4h	4	Host Controller Misc Reg2 (HOST_CTRL_MISC_REG2)	10000184h
80B8h	4	Super Speed Port Enable (SSPE_REG)	C0000000h
80E0h	4	AUX Power Management Control (AUX_CTRL_REG1)	8080BCE0h
80ECh	4	SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG)	18020C00h
80F0h	4	USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1)	314803A0h
80F4h	4	USB2 Port Link Control 2 (USB2_LINK_MGR_CTRL_REG2)	80C40620h
80F8h	4	USB2 Port Link Control 3 (USB2_LINK_MGR_CTRL_REG3)	F865EB6Bh
80FCh	4	USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4)	02008003h
8140h	4	Power Scheduler Control-0 (PWR_SCHED_CTRL0)	0A019132h
8144h	4	Power Scheduler Control-1 (PWR_SCHED_CTRL2)	0000023Fh
8154h	4	AUX Power Management Control (AUX_CTRL_REG2)	81192206h
8164h	4	USB2 PHY Power Management Control (USB2_PHY_PMC)	000000FCh
816Ch	4	XHCI Aux Clock Control Register (XHCI_AUX_CCR)	000F403Ch
8174h	4	XHC Latency Tolerance Parameters LTV Control (XLTP_LTV1)	01400C01h
8178h	4	XHC Latency Tolerance Parameters LTV Control 2 (XLTP_LTV2)	000017FFh
817Ch	4	XHC Latency Tolerance Parameters High Idle Time Control (XLTP_HITC)	00050002h
8180h	4	XHC Latency Tolerance Parameters Medium Idle Time Control (XLTP_MITC)	00050002h
8184h	4	XHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC)	00050002h
81B8h	4	LFPS On Count (LFPSONCOUNT_REG)	000420C8h
81C4h	4	USB2 Power Management Control (USB2PMCTRL_REG)	00020908h
846Ch	4	USB Legacy Support Capability (USBLEGSUP)	00002201h
8470h	4	USB Legacy Support Control Status (USBLEGCTLSTS)	00000000h
84F4h	4	Port Disable Override Capability Register (PDO_CAPABILITY)	000003C6h
8700h	4	Debug Capability ID Register (DCID)	0005100Ah
8704h	4	Debug Capability Doorbell Register (DCDB)	00000000h
8708h	4	Debug Capability Event Ring Segment Table Size Register (DCERSTSZ)	00000000h
8710h	8	Debug Capability Event Ring Segment Table Base Address Register (DCERSTBA)	0000000000000000h
8718h	8	Debug Capability Event Ring Dequeue Pointer Register (DCERDP)	0000000000000000h
8720h	4	Debug Capability Control Register (DCCTRL)	00000000h
8724h	4	Debug Capability Status Register (DCST)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8728h	4	Debug Capability Port Status And Control Register (DCPORTSC)	00000080h
8730h	8	Debug Capability Context Pointer Register (DCCP)	0000000000000000h
8E10h	4	GLOBAL TIME SYNC CAP REG (GLOBAL_TIME_SYNC_CAP_REG)	000012C9h
8E14h	4	GLOBAL TIME SYNC CTRL REG (GLOBAL_TIME_SYNC_CTRL_REG)	00000000h
8E18h	4	MICROFRAME TIME REG (MICROFRAME_TIME_REG)	00000000h
8E20h	4	GLOBAL TIME LOW REG (GLOBAL_TIME_LOW_REG)	00000000h
8E24h	4	GLOBAL TIME HI REG (GLOBAL_TIME_HI_REG)	00000000h
90A4h	4	XHCI USB2 Overcurrent Pin Mapping (U2OCM1)	00000000h
90A8h	4	XHCI USB2 Overcurrent Pin Mapping (U2OCM2)	00000000h
90ACh	4	XHCI USB2 Overcurrent Pin Mapping (U2OCM3)	00000000h
90B0h	4	XHCI USB2 Overcurrent Pin Mapping (U2OCM4)	00000000h
90B4h	4	XHCI USB2 Overcurrent Pin Mapping (U2OCM5)	00000000h
90B8h	4	XHCI USB2 Overcurrent Pin Mapping (U2OCM6)	00000000h
90BCh	4	XHCI USB2 Overcurrent Pin Mapping (U2OCM7)	00000000h
90C0h	4	XHCI USB2 Overcurrent Pin Mapping (U2OCM8)	00000000h
9124h	4	XHCI USB3 Overcurrent Pin Mapping (U3OCM1)	00000000h
9128h	4	XHCI USB3 Overcurrent Pin Mapping (U3OCM2)	00000000h
912Ch	4	XHCI USB3 Overcurrent Pin Mapping (U3OCM3)	00000000h
9130h	4	XHCI USB3 Overcurrent Pin Mapping (U3OCM4)	00000000h
9134h	4	XHCI USB3 Overcurrent Pin Mapping (U3OCM5)	00000000h
9138h	4	XHCI USB3 Overcurrent Pin Mapping (U3OCM6)	00000000h
913Ch	4	XHCI USB3 Overcurrent Pin Mapping (U3OCM7)	00000000h
9140h	4	XHCI USB3 Overcurrent Pin Mapping (U3OCM8)	00000000h

17.2.1 Capability Registers Length (CAPLENGTH) - Offset 0h

This register is modified and maintained by BIOS.

Type	Size	Offset	Default
MMIO	8 bit	MBAR + 0h	80h

Bit Range	Default & Access	Field Name (ID): Description
7:0	80h RW/L	**Capability Registers Length (CAPLENGTH):** Capability Registers Length (CAPLENGTH) **Locked by:** XHCC1.ACCTRL

17.2.2 Host Controller Interface Version Number (HCIVERSION) - Offset 2h

This register is modified and maintained by BIOS.

Type	Size	Offset	Default
MMIO	16 bit	MBAR + 2h	0110h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0110h RW/L	**Host Controller Interface Version Number (HCIVERSION):** Host Controller Interface Version Number (HCIVERSION) **Locked by:** XHCC1.ACCTRL

17.2.3 Structural Parameters 1 (HCSPARAMS1) - Offset 4h

This register is modified and maintained by BIOS.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 4h	10000840h

Bit Range	Default & Access	Field Name (ID): Description
31:24	10h RW/L	**Number of Ports (MAXPORTS):** Number of Ports (MaxPorts): The value in this field reflects the highest numbered port in the controller, not the actual count of the number of ports. This allows for gaps in the port numbering, between USB2 and USB3 protocol capabilities. **Locked by:** XHCC1.ACCTRL
23:19	0h RO	**Reserved**
18:8	008h RW/L	**Number of Interrupters (MAXINTRS):** Number of Interrupters (MaxInt) **Locked by:** XHCC1.ACCTRL
7:0	40h RW/L	**Number of Device Slots (MAXSLOTS):** Number of Device Slots (MaxSlots) **Locked by:** XHCC1.ACCTRL

17.2.4 Structural Parameters 2 (HCSPARAMS2) - Offset 8h

This register is modified and maintained by BIOS.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8h	14200054h

Bit Range	Default & Access	Field Name (ID): Description
31:27	02h RW/L	**Max Scratchpad Buffers LO (MAXSCRATCHPADBUFS):** Max Scratchpad Buffers Lo (MaxScratchpadBufs) **Locked by:** XHCC1.ACCTRL
26	1h RW/L	**Scratchpad Restore (SPR):** Scratchpad Restore (SPR) **Locked by:** XHCC1.ACCTRL
25:21	01h RW/L	**Max Scratchpad Buffers HI (MAXSCRATCHPADBUFS_HI):** Max Scratchpad Buffers Hi (MaxScratchpadBufs) **Locked by:** XHCC1.ACCTRL
20:8	0h RO	**Reserved**
7:4	5h RW/L	**Event Ring Segment Table Max (ERSTMAX):** Event Ring Segment Table Max (ERSTMax) **Locked by:** XHCC1.ACCTRL
3:0	4h RW/L	**Isochronous Scheduling Threshold (IST):** Isochronous Scheduling Threshold (IST) **Locked by:** XHCC1.ACCTRL

17.2.5 Structural Parameters 3 (HCSPARAMS3) - Offset Ch

This register is modified and maintained by BIOS.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + Ch	00A0000Ah

Bit Range	Default & Access	Field Name (ID): Description
31:16	00A0h RW/L	**U2 Device Exit Latency (U2DEL):** U2 Device Exit Latency (U2DEL) **Locked by:** XHCC1.ACCTRL
15:8	0h RO	**Reserved**
7:0	0Ah RW/L	**U1 Device Exit Latency (U1DEL):** U1 Device Exit Latency (U1DEL) **Locked by:** XHCC1.ACCTRL

17.2.6 Capability Parameters (HCCPARAMS) - Offset 10h

This register is modified and maintained by BIOS.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 10h	20007FC1h

Bit Range	Default & Access	Field Name (ID): Description
31:16	2000h RW/L	**xHCI Extended Capabilities Pointer (XECP):** xHCI Extended Capabilities Pointer (xECP): The Default value should be 2008h if NumUSB2 = 0 **Locked by:** XHCC1.ACCTRL
15:12	7h RW/L	**Maximum Primary Stream Array Size (MAXPSASIZE):** Maximum Primary Stream Array Size (MaxPSASize) **Locked by:** XHCC1.ACCTRL
11	1h RW/L	**Contiguous Frame ID Capability (CFC):** Contiguous Frame ID Capability (CFC) **Locked by:** XHCC1.ACCTRL
10	1h RW/L	**Stopped EDLTA Capability (SEC):** Stopped EDLTA Capability (SEC) **Locked by:** XHCC1.ACCTRL
9	1h RW/L	**Stopped - Short Packet Capability (SPC):** Stopped - Short Packet Capability (SPC) **Locked by:** XHCC1.ACCTRL
8	1h RW/L	**Parse All Event Data (PAE):** Parse All Event Data (PAE) **Locked by:** XHCC1.ACCTRL
7	1h RW/L	**No Secondary SID Support (NSS):** No Secondary SID Support (NSS) **Locked by:** XHCC1.ACCTRL
6	1h RW/L	**Latency Tolerance Messaging Capability (LTC):** Latency Tolerance Messaging Capability (LTC) **Locked by:** XHCC1.ACCTRL
5	0h RW/L	**Light HC Reset Capability (LHRC):** Light HC Reset Capability (LHRC) **Locked by:** XHCC1.ACCTRL
4	0h RW/L	**Port Indicators (PIND):** Port Indicators (PIND) **Locked by:** XHCC1.ACCTRL
3	0h RW/L	**Port Power Control (PPC):** Port Power Control (PPC) **Locked by:** XHCC1.ACCTRL
2	0h RW/L	**Context Size (CSZ):** Context Size (CSZ) **Locked by:** XHCC1.ACCTRL
1	0h RW/L	**BW Negotiation Capability (BNC):** BW Negotiation Capability (BNC) **Locked by:** XHCC1.ACCTRL
0	1h RW/L	**64-bit Addressing Capability (AC64):** 64-bit Addressing Capability (AC64) **Locked by:** XHCC1.ACCTRL

17.2.7 Doorbell Offset (DBOFF) - Offset 14h

Doorbell Offset.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 14h	00003000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000C00h RO	**Doorbell Array Offset (DBAO):** Doorbell Array Offset (DBAO)
1:0	0h RO	**Reserved**

17.2.8 Runtime Register Space Offset (RTSOFF) - Offset 18h

Runtime Register Space Offset.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 18h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0000100h RO	**Runtime Register Space Offset (RTRSO):** Runtime Register Space Offset (RTRSO)
4:0	0h RO	**Reserved**

17.2.9 USB Command (USBCMD) - Offset 80h

USB Command.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14	0h RW	**Extended TCB Enable (ETE):** This flag indicates that the host controller implementation is enabled to support Transfer Burst Count values greater than 4 in Isoch TDs. This bit may be set only if ETC = 1.
13	0h RW	**CEM Enable (CEM):** Default = '0'. when set to '1', a Max Exit Latency Too Large Capability Error may be returned by a Configure Endpoint Command. When Cleared to '0', a Max Exit latency Too Large Capability Error shall not be returned by a Configure Endpoint Command. This bit is Reserved if CMC='0'.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	**Reserved**
11	0h RW	**Enable U3 MFINDEX Stop (EU3S):** Enable U3 MFINDEX Stop
10	0h RW	**Enable Wrap Event (EWE):** Enable Wrap Event
9	0h RW	**Controller Restore State (CRS):** Controller Restore State
8	0h RW	**Controller Save State (CSS):** Controller Save State
7	0h RW	**Light Host Controller Reset (LHCRST):** Light Host Controller Reset
6:4	0h RO	**Reserved**
3	0h RW	**Host System Error Enable (HSEE):** Host System Error Enable
2	0h RW	**Interrupter Enable (INTE):** Interrupter Enable
1	0h RW	**Host Controller Reset (HCRST):** Host Controller Reset
0	0h RW	**RS:** Run/Stop

17.2.10 USB Status (USBSTS) - Offset 84h

USB Status.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 84h	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RO	**Host Controller Error (HCE):** This bit is not preset in HC, this is deviation from XHCI 1.0 spec.
11	0h RO	**Controller Not Ready (CNR):** This is deviation from XHCI 1.0 spec.
10	0h RW/1C	**Save/Restore Error (SRE):** Save/Restore Error
9	0h RO	**Restore State Status (RSS):** Restore State Status
8	0h RO	**Save State Status (SSS):** Save State Status

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Reserved**
4	0h RW/1C	**Port Change Detect (PCD):** Port Change Detect
3	0h RW/1C	**Event Interrupt (EINT):** Event Interrupt
2	0h RW/1C	**Host System Error (HSE):** Host System Error
1	0h RO	**Reserved**
0	1h RO	**HCH:** HCHalted

17.2.11 Page Size (PAGESIZE) - Offset 88h

Page Size.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 88h	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0001h RO	**Page Size (PAGESIZE):** Page Size

17.2.12 Device Notification Control (DNCTRL) - Offset 94h

Device Notification Control.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Notification Enable (N0_N15):** Notification Enable

17.2.13 Command Ring Low (CRCR_LO) - Offset 98h

Command Ring Low.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h WO	**Command Ring Pointer (CRP):** Command Ring Pointer
5:4	0h RO	**Reserved**
3	0h RO	**Command Ring Running (CRR):** Command Ring Running
2	0h WO	**Command Abort (CA):** Command Abort
1	0h WO	**Command Stop (CS):** Command Stop
0	0h WO	**Ring Cycle State (RCS):** Ring Cycle State

17.2.14 Command Ring High (CRCR_HI) - Offset 9Ch

Command Ring High.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**Command Ring Pointer (CRP):** Command Ring Pointer

17.2.15 Device Context Base Address Array Pointer Low (DCBAAP_LO) - Offset B0h

Device Context Base Address Array Pointer Low.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RW	**Device Context Base Address Array Pointer (DCBAAP):** Device Context Base Address Array Pointer
5:0	0h RO	**Reserved**

17.2.16 Device Context Base Address Array Pointer High (DCBAAP_HI) - Offset B4h

Device Context Base Address Array Pointer High.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Device Context Base Address Array Pointer (DCBAAP):** Device Context Base Address Array Pointer High

17.2.17 Configure Reg (CONFIG) - Offset B8h

Configure Reg.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9	0h RW	**Configuration Information Enable (CIE):** Configuration Information Enable
8	0h RW	**U3 Entry Enable (U3E):** U3 Entry Enable
7:0	00h RW	**Max Device Slots Enabled (MAXSLOTSEN):** Max Device Slots Enabled

17.2.18 Port Status And Control USB2 (PORTSC1) - Offset 480h

The USB PORTSC registers should be accessed via DW writes for any modification.

Byte Writes have unintended behavior.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 480h	000002A0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR):** Warm Port Reset
30	0h RW/L	**Device Removable (DR):** Device Removable **Locked by:** XHCC1.ACCTRL
29:28	0h RO	**Reserved**
27	0h RW/P	**Wake on Over-current Enable (WOE):** Note: This register is sticky.
26	0h RW/P	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0h RW/P	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0h RO	**Cold Attach Status (CAS):** Cold Attach Status
23	0h RW/1C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0h RW/1C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0h RW/1C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0h RW/1C	**Over-current Change (OCC):** Note: This register is sticky.
19	0h RW/1C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0h RW/1C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0h RW/1C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0h RW	**Port Link State Write Strobe (LWS):** Port Link State Write Strobe
15:14	0h RW/P	**Port Indicator Control (PIC):** Note: This register is sticky.
13:10	0h RW	**Port Speed (PORTSPEED):** Note: This register is sticky.
9	1h RW/P	**Port Power (PP):** Note: This register is sticky.
8:5	5h RW/P	**Port Link State (PLS):** Note: This register is sticky.
4	0h RW/1S	**Port Reset (PR):** Port Reset
3	0h RW	**Over-current Active (OCA):** Note: This register is sticky.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Reserved**
1	0h RW/1C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0h RW	**Current Connect Status (CCS):** Note: This register is sticky.

17.2.19 Port Power Management Status And Control USB2 (PORTPMSC1) - Offset 484h

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 484h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW/P	**Port Test Control (PTC):** Note: This register is sticky.
27:17	0h RO	**Reserved**
16	0h RW	**Hardware LPM Enable (HLE):** Hardware LPM Enable
15:8	00h RW/P	**Device Address (DA):** Note: This register is sticky.
7:4	0h RW/P	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky.
3	0h RW/P	**Remote Wake Enable (RWE):** Note: This register is sticky.
2:0	0h RW	**L1 Status (L1S):** Note: This register is sticky.

17.2.20 Port X Hardware LPM Control Register (PORTHLPMC1) - Offset 48Ch

This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST).

The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters necessary for xHC to automatically generate an LPM Token to the downstream device.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 48Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value.
9:2	00h RW/P	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky.
1:0	0h RW/P	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky.

17.2.21 Microframe Index (RTMFINDEX) - Offset 2000h

Microframe Index.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2000h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:0	0000h RO	**Microframe Index (IMAN0):** Microframe Index

17.2.22 Interrupter Management (IMAN0) - Offset 2020h

There are 8 IMAN registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2020h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**Interrupt Enable (IE):** Interrupt Enable
0	0h RW/1C	**Interrupt Pending (IP):** Interrupt Pending

17.2.23 Interrupter Moderation (IMOD0) - Offset 2024h

There are 8 IMOD registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2024h	00000FA0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Interrupt Moderation Counter (IMODC):** Interrupt Moderation Counter
15:0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Interrupt Moderation Interval

17.2.24 Event Ring Segment Table Size (ERSTSZ0) - Offset 2028h

There are 8 ERSTSZ register.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2028h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Event Ring Segment Table Size (ERSTS):** Event Ring Segment Table Size

17.2.25 Event Ring Segment Table Base Address Low (ERSTBA_LO0) - Offset 2030h

There are 8 ERSTBA_LO registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2030h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Event Ring Segment Table Base Address Register
5:0	0h RO	**Reserved**

17.2.26 Event Ring Segment Table Base Address High (ERSTBA_HI0) - Offset 2034h

Event Ring Segment Table Base Address High.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2034h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA):** Event Ring Segment Table Base Address

17.2.27 Event Ring Dequeue Pointer Low (ERDP_LO0) - Offset 2038h

There are 8 ERDP_LO registers.

x = 1, 2, ...,8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2038h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** Event Ring Dequeue Pointer
3	0h RW/1C	**Event Handler Busy (EHB):** Event Handler Busy
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** Dequeue ERST Segment Index

17.2.28 Event Ring Dequeue Pointer High (ERDP_HI0) - Offset 203Ch

There are 8 ERDP_HI registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 203Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** Event Ring Dequeue Pointer

17.2.29 Interrupter Management (IMAN1) - Offset 2040h

There are 8 IMAN registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2040h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**Interrupt Enable (IE):** Interrupt Enable
0	0h RW/1C	**Interrupt Pending (IP):** Interrupt Pending

17.2.30 Interrupter Moderation (IMOD1) - Offset 2044h

There are 8 IMOD registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2044h	00000FA0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Interrupt Moderation Counter (IMODC):** Interrupt Moderation Counter
15:0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Interrupt Moderation Interval

17.2.31 Event Ring Segment Table Size (ERSTSZ1) - Offset 2048h

There are 8 ERSTSZ register.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2048h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Event Ring Segment Table Size (ERSTS):** Event Ring Segment Table Size

17.2.32 Event Ring Segment Table Base Address Low (ERSTBA_LO1) - Offset 2050h

There are 8 ERSTBA_LO registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2050h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Event Ring Segment Table Base Address Register
5:0	0h RO	**Reserved**

17.2.33 Event Ring Segment Table Base Address High (ERSTBA_HI1) - Offset 2054h

Event Ring Segment Table Base Address High.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2054h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA):** Event Ring Segment Table Base Address

17.2.34 Event Ring Dequeue Pointer Low (ERDP_LO1) - Offset 2058h

There are 8 ERDP_LO registers.

x = 1, 2, ...,8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2058h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** Event Ring Dequeue Pointer
3	0h RW/1C	**Event Handler Busy (EHB):** Event Handler Busy
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** Dequeue ERST Segment Index

17.2.35 Event Ring Dequeue Pointer High (ERDP_HI1) - Offset 205Ch

There are 8 ERDP_HI registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 205Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** Event Ring Dequeue Pointer

17.2.36 Interrupter Management (IMAN2) - Offset 2060h

There are 8 IMAN registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2060h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**Interrupt Enable (IE):** Interrupt Enable
0	0h RW/1C	**Interrupt Pending (IP):** Interrupt Pending

17.2.37 Interrupter Moderation (IMOD2) - Offset 2064h

There are 8 IMOD registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2064h	00000FA0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Interrupt Moderation Counter (IMODC):** Interrupt Moderation Counter
15:0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Interrupt Moderation Interval

17.2.38 Event Ring Segment Table Size (ERSTSZ2) - Offset 2068h

There are 8 ERSTSZ register.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2068h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Event Ring Segment Table Size (ERSTS):** Event Ring Segment Table Size

17.2.39 Event Ring Segment Table Base Address Low (ERSTBA_LO2) - Offset 2070h

There are 8 ERSTBA_LO registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2070h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Event Ring Segment Table Base Address Register
5:0	0h RO	**Reserved**

17.2.40 Event Ring Segment Table Base Address High (ERSTBA_HI2) - Offset 2074h

Event Ring Segment Table Base Address High.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2074h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA):** Event Ring Segment Table Base Address

17.2.41 Event Ring Dequeue Pointer Low (ERDP_LO2) - Offset 2078h

There are 8 ERDP_LO registers.

x = 1, 2, ...,8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2078h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** Event Ring Dequeue Pointer
3	0h RW/1C	**Event Handler Busy (EHB):** Event Handler Busy
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** Dequeue ERST Segment Index

17.2.42 Event Ring Dequeue Pointer High (ERDP_HI2) - Offset 207Ch

There are 8 ERDP_HI registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 207Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** Event Ring Dequeue Pointer

17.2.43 Interrupter Management (IMAN3) - Offset 2080h

There are 8 IMAN registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2080h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**Interrupt Enable (IE):** Interrupt Enable
0	0h RW/1C	**Interrupt Pending (IP):** Interrupt Pending

17.2.44 Interrupter Moderation (IMOD3) - Offset 2084h

There are 8 IMOD registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2084h	00000FA0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Interrupt Moderation Counter (IMODC):** Interrupt Moderation Counter
15:0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Interrupt Moderation Interval

17.2.45 Event Ring Segment Table Size (ERSTSZ3) - Offset 2088h

There are 8 ERSTSZ register.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2088h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Event Ring Segment Table Size (ERSTS):** Event Ring Segment Table Size

17.2.46 Event Ring Segment Table Base Address Low (ERSTBA_LO3) - Offset 2090h

There are 8 ERSTBA_LO registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2090h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Event Ring Segment Table Base Address Register
5:0	0h RO	**Reserved**

17.2.47 Event Ring Segment Table Base Address High (ERSTBA_HI3) - Offset 2094h

Event Ring Segment Table Base Address High.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2094h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA):** Event Ring Segment Table Base Address

17.2.48 Event Ring Dequeue Pointer Low (ERDP_LO3) - Offset 2098h

There are 8 ERDP_LO registers.

x = 1, 2, ...,8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2098h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** Event Ring Dequeue Pointer
3	0h RW/1C	**Event Handler Busy (EHB):** Event Handler Busy
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** Dequeue ERST Segment Index

17.2.49 Event Ring Dequeue Pointer High (ERDP_HI3) - Offset 209Ch

There are 8 ERDP_HI registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 209Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** Event Ring Dequeue Pointer

17.2.50 Interrupter Management (IMAN4) - Offset 20A0h

There are 8 IMAN registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 20A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**Interrupt Enable (IE):** Interrupt Enable
0	0h RW/1C	**Interrupt Pending (IP):** Interrupt Pending

17.2.51 Interrupter Moderation (IMOD4) - Offset 20A4h

There are 8 IMOD registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 20A4h	00000FA0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Interrupt Moderation Counter (IMODC):** Interrupt Moderation Counter
15:0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Interrupt Moderation Interval

17.2.52 Event Ring Segment Table Size (ERSTSZ4) - Offset 20A8h

There are 8 ERSTSZ register.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 20A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Event Ring Segment Table Size (ERSTS):** Event Ring Segment Table Size

17.2.53 Event Ring Segment Table Base Address Low (ERSTBA_LO4) - Offset 20B0h

There are 8 ERSTBA_LO registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 20B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Event Ring Segment Table Base Address Register
5:0	0h RO	**Reserved**

17.2.54 Event Ring Segment Table Base Address High (ERSTBA_HI4) - Offset 20B4h

Event Ring Segment Table Base Address High.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 20B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA):** Event Ring Segment Table Base Address

17.2.55 Event Ring Dequeue Pointer Low (ERDP_LO4) - Offset 20B8h

There are 8 ERDP_LO registers.

x = 1, 2, ...,8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 20B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** Event Ring Dequeue Pointer
3	0h RW/1C	**Event Handler Busy (EHB):** Event Handler Busy
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** Dequeue ERST Segment Index

17.2.56 Event Ring Dequeue Pointer High (ERDP_HI4) - Offset 20BCh

There are 8 ERDP_HI registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 20BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** Event Ring Dequeue Pointer

17.2.57 Interrupter Management (IMAN5) - Offset 20C0h

There are 8 IMAN registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 20C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**Interrupt Enable (IE):** Interrupt Enable
0	0h RW/1C	**Interrupt Pending (IP):** Interrupt Pending

17.2.58 Interrupter Moderation (IMOD5) - Offset 20C4h

There are 8 IMOD registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 20C4h	00000FA0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Interrupt Moderation Counter (IMODC):** Interrupt Moderation Counter
15:0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Interrupt Moderation Interval

17.2.59 Event Ring Segment Table Size (ERSTSZ5) - Offset 20C8h

There are 8 ERSTSZ register.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 20C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Event Ring Segment Table Size (ERSTS):** Event Ring Segment Table Size

17.2.60 Event Ring Segment Table Base Address Low (ERSTBA_LO5) - Offset 20D0h

There are 8 ERSTBA_LO registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 20D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Event Ring Segment Table Base Address Register
5:0	0h RO	**Reserved**

17.2.61 Event Ring Segment Table Base Address High (ERSTBA_HI5) - Offset 20D4h

Event Ring Segment Table Base Address High.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 20D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA):** Event Ring Segment Table Base Address

17.2.62 Event Ring Dequeue Pointer Low (ERDP_LO5) - Offset 20D8h

There are 8 ERDP_LO registers.

x = 1, 2, ...,8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 20D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** Event Ring Dequeue Pointer
3	0h RW/1C	**Event Handler Busy (EHB):** Event Handler Busy
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** Dequeue ERST Segment Index

17.2.63 Event Ring Dequeue Pointer High (ERDP_HI5) - Offset 20DCh

There are 8 ERDP_HI registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 20DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** Event Ring Dequeue Pointer

17.2.64 Interrupter Management (IMAN6) - Offset 20E0h

There are 8 IMAN registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 20E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**Interrupt Enable (IE):** Interrupt Enable
0	0h RW/1C	**Interrupt Pending (IP):** Interrupt Pending

17.2.65 Interrupter Moderation (IMOD6) - Offset 20E4h

There are 8 IMOD registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 20E4h	00000FA0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Interrupt Moderation Counter (IMODC):** Interrupt Moderation Counter
15:0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Interrupt Moderation Interval

17.2.66 Event Ring Segment Table Size (ERSTSZ6) - Offset 20E8h

There are 8 ERSTSZ register.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 20E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Event Ring Segment Table Size (ERSTS):** Event Ring Segment Table Size

17.2.67 Event Ring Segment Table Base Address Low (ERSTBA_LO6) - Offset 20F0h

There are 8 ERSTBA_LO registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 20F0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Event Ring Segment Table Base Address Register
5:0	0h RO	**Reserved**

17.2.68 Event Ring Segment Table Base Address High (ERSTBA_HI6) - Offset 20F4h

Event Ring Segment Table Base Address High.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 20F4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA):** Event Ring Segment Table Base Address

17.2.69 Event Ring Dequeue Pointer Low (ERDP_LO6) - Offset 20F8h

There are 8 ERDP_LO registers.

x = 1, 2, ...,8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 20F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** Event Ring Dequeue Pointer
3	0h RW/1C	**Event Handler Busy (EHB):** Event Handler Busy
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** Dequeue ERST Segment Index

17.2.70 Event Ring Dequeue Pointer High (ERDP_HI6) - Offset 20FCh

There are 8 ERDP_HI registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 20FCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** Event Ring Dequeue Pointer

17.2.71 Interrupter Management (IMAN7) - Offset 2100h

There are 8 IMAN registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2100h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**Interrupt Enable (IE):** Interrupt Enable
0	0h RW/1C	**Interrupt Pending (IP):** Interrupt Pending

17.2.72 Interrupter Moderation (IMOD7) - Offset 2104h

There are 8 IMOD registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2104h	00000FA0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Interrupt Moderation Counter (IMODC):** Interrupt Moderation Counter
15:0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Interrupt Moderation Interval

17.2.73 Event Ring Segment Table Size (ERSTSZ7) - Offset 2108h

There are 8 ERSTSZ register.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2108h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Event Ring Segment Table Size (ERSTS):** Event Ring Segment Table Size

17.2.74 Event Ring Segment Table Base Address Low (ERSTBA_LO7) - Offset 2110h

There are 8 ERSTBA_LO registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2110h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Event Ring Segment Table Base Address Register
5:0	0h RO	**Reserved**

17.2.75 Event Ring Segment Table Base Address High (ERSTBA_HI7) - Offset 2114h

Event Ring Segment Table Base Address High.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2114h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA):** Event Ring Segment Table Base Address

17.2.76 Event Ring Dequeue Pointer Low (ERDP_LO7) - Offset 2118h

There are 8 ERDP_LO registers.

x = 1, 2, ...,8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2118h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** Event Ring Dequeue Pointer
3	0h RW/1C	**Event Handler Busy (EHB):** Event Handler Busy
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** Dequeue ERST Segment Index

17.2.77 Event Ring Dequeue Pointer High (ERDP_HI7) - Offset 211Ch

There are 8 ERDP_HI registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 211Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** Event Ring Dequeue Pointer

17.2.78 Door Bell (DB0) - Offset 3000h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3000h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.79 Door Bell (DB1) - Offset 3004h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3004h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.80 Door Bell (DB2) - Offset 3008h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3008h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.81 Door Bell (DB3) - Offset 300Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 300Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.82 Door Bell (DB4) - Offset 3010h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3010h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.83 Door Bell (DB5) - Offset 3014h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3014h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.84 Door Bell (DB6) - Offset 3018h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3018h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.85 Door Bell (DB7) - Offset 301Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 301Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.86 Door Bell (DB8) - Offset 3020h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3020h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.87 Door Bell (DB9) - Offset 3024h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3024h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.88 Door Bell (DB10) - Offset 3028h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3028h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.89 Door Bell (DB11) - Offset 302Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 302Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.90 Door Bell (DB12) - Offset 3030h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3030h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.91 Door Bell (DB13) - Offset 3034h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3034h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.92 Door Bell (DB14) - Offset 3038h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3038h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.93 Door Bell (DB15) - Offset 303Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 303Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.94 Door Bell (DB16) - Offset 3040h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3040h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.95 Door Bell (DB17) - Offset 3044h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3044h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.96 Door Bell (DB18) - Offset 3048h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3048h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.97 Door Bell (DB19) - Offset 304Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 304Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.98 Door Bell (DB20) - Offset 3050h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3050h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.99 Door Bell (DB21) - Offset 3054h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3054h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.100 Door Bell (DB22) - Offset 3058h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3058h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.101 Door Bell (DB23) - Offset 305Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 305Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.102 Door Bell (DB24) - Offset 3060h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3060h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.103 Door Bell (DB25) - Offset 3064h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3064h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.104 Door Bell (DB26) - Offset 3068h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3068h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.105 Door Bell (DB27) - Offset 306Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 306Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.106 Door Bell (DB28) - Offset 3070h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3070h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.107 Door Bell (DB29) - Offset 3074h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3074h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.108 Door Bell (DB30) - Offset 3078h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3078h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.109 Door Bell (DB31) - Offset 307Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 307Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.110 Door Bell (DB32) - Offset 3080h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3080h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.111 Door Bell (DB33) - Offset 3084h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3084h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.112 Door Bell (DB34) - Offset 3088h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3088h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.113 Door Bell (DB35) - Offset 308Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 308Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.114 Door Bell (DB36) - Offset 3090h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3090h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.115 Door Bell (DB37) - Offset 3094h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3094h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.116 Door Bell (DB38) - Offset 3098h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3098h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.117 Door Bell (DB39) - Offset 309Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 309Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.118 Door Bell (DB40) - Offset 30A0h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.119 Door Bell (DB41) - Offset 30A4h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.120 Door Bell (DB42) - Offset 30A8h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.121 Door Bell (DB43) - Offset 30ACh

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.122 Door Bell (DB44) - Offset 30B0h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.123 Door Bell (DB45) - Offset 30B4h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.124 Door Bell (DB46) - Offset 30B8h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.125 Door Bell (DB47) - Offset 30BCh

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.126 Door Bell (DB48) - Offset 30C0h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.127 Door Bell (DB49) - Offset 30C4h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.128 Door Bell (DB50) - Offset 30C8h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.129 Door Bell (DB51) - Offset 30CCh

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.130 Door Bell (DB52) - Offset 30D0h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.131 Door Bell (DB53) - Offset 30D4h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.132 Door Bell (DB54) - Offset 30D8h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.133 Door Bell (DB55) - Offset 30DCh

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.134 Door Bell (DB56) - Offset 30E0h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.135 Door Bell (DB57) - Offset 30E4h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.136 Door Bell (DB58) - Offset 30E8h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.137 Door Bell (DB59) - Offset 30ECh

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.138 Door Bell (DB60) - Offset 30F0h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30F0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.139 Door Bell (DB61) - Offset 30F4h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30F4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.140 Door Bell (DB62) - Offset 30F8h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.141 Door Bell (DB63) - Offset 30FCh

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 30FCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.142 Door Bell (DB64) - Offset 3100h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3100h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

17.2.143 XECP SUPP USB2_1 (XECP_SUPP_USB2_1) - Offset 8004h

XECP SUPP USB2_1.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8004h	20425355h

Bit Range	Default & Access	Field Name (ID): Description
31:0	20425355h RO	**XECP_SUPP_USB2_1:** Namestring USB

17.2.144 XECP SUPP USB3_3 (XECP_SUPP_USB2_3) - Offset 800Ch

XECP SUPP USB3_3.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 800Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RO	**PROTOCOL_SLOT_TYPE:** Protocol Slot Type

17.2.145 XECP SUPP USB2_4 Full Speed (XECP_SUPP_USB2_4) - Offset 8010h

XECP SUPP USB2_4 Full Speed.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8010h	000C0021h

Bit Range	Default & Access	Field Name (ID): Description
31:16	000Ch RO	**Protocol Speed ID Mantissa (PSIM):** Protocol Speed ID Mantissa
15:9	0h RO	**Reserved**
8	0h RO	**PSI Full Duplex (PFD):** PSI Full Duplex
7:6	0h RO	**PSI Type (PLT):** PSI Type
5:4	2h RO	**Protocol Speed ID Exponent (PSIE):** Protocol Speed ID Exponent
3:0	1h RO	**Protocol Speed ID Value (PSIV):** Protocol Speed ID Value

17.2.146 XECP_SUPP USB2_5 Low Speed (XECP_SUPP_USB2_5) - Offset 8014h

XECP_SUPP USB2_5 Low Speed.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8014h	05DC0012h

Bit Range	Default & Access	Field Name (ID): Description
31:16	05DCh RO	**Protocol Speed ID Mantissa (PSIM):** Protocol Speed ID Mantissa
15:9	0h RO	**Reserved**
8	0h RO	**PSI Full Duplex (PFD):** PSI Full Duplex
7:6	0h RO	**PSI Type (PLT):** PSI Type
5:4	1h RO	**Protocol Speed ID Exponent (PSIE):** Protocol Speed ID Exponent
3:0	2h RO	**Protocol Speed ID Value (PSIV):** Protocol Speed ID Value

17.2.147 XECP SUPP USB2_6 High Speed (XECP_SUPP_USB2_6) - Offset 8018h

XECP SUPP USB2_6 High Speed.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8018h	01E00023h

Bit Range	Default & Access	Field Name (ID): Description
31:16	01E0h RO	**Protocol Speed ID Mantissa (PSIM):** Protocol Speed ID Mantissa
15:9	0h RO	**Reserved**
8	0h RO	**PSI Full Duplex (PFD):** PSI Full Duplex
7:6	0h RO	**PSI Type (PLT):** PSI Type
5:4	2h RO	**Protocol Speed ID Exponent (PSIE):** Protocol Speed ID Exponent
3:0	3h RO	**Protocol Speed ID Value (PSIV):** Protocol Speed ID Value

17.2.148 XECP SUPP USB3_0 (XECP_SUPP_USB3_0) - Offset 8020h

XECP SUPP USB3_0.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8020h	03101402h

Bit Range	Default & Access	Field Name (ID): Description
31:24	03h RO	**USB Major Revision: 3.0 (USB3_MAJ_REV):** USB Major Revision: 3.0
23:16	10h RW/L	**USB Minor Revision (USB3_MIN_REV):** USB Minor Revision: 0.1 **Locked by:** XHCC1.ACCTRL
15:8	14h RW/L	**Next Capability Pointer (NCP):** Next Capability Pointer **Locked by:** XHCC1.ACCTRL
7:0	02h RO	**Supported Protocol ID (SPID):** Supported Protocol ID

17.2.149 XECP SUPP USB3_1 (XECP_SUPP_USB3_1) - Offset 8024h

XECP SUPP USB3_1.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8024h	20425355h

Bit Range	Default & Access	Field Name (ID): Description
31:0	20425355h RO	**XECP_SUPP_USB3_1:** Namestring USB

17.2.150 XECP SUPP USB3_2 (XECP_SUPP_USB3_2) - Offset 8028h

XECP SUPP USB3_2.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8028h	8000040Dh

Bit Range	Default & Access	Field Name (ID): Description
31:28	8h RO	**Protocol Speed ID Count (PROT_SPD_ID_CNT):** 1 USB 3.0 Speed (Supper Speed)
27:16	0h RO	**Reserved**
15:8	04h RO	**Compatible Port Count (CPC):** The compatible port count varies based on SKU - controlled by the USB3 Port config fuses
7:0	0Dh RO	**Compatible Port Offset (CPO):** Compatible Port Offset

17.2.151 XECP SUPP USB3_3 (XECP_SUPP_USB3_3) - Offset 802Ch

XECP SUPP USB3_3.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 802Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RO	**PROTOCOL_SLOT_TYPE:** Protocol Slot Type

17.2.152 XECP SUPP USB3_4 (XECP_SUPP_USB3_4) - Offset 8030h

XECP SUPP USB3_4.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8030h	00050134h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0005h RO	**Protocol Speed ID Mantissa (PSIM):** Protocol Speed ID Mantissa
15:9	0h RO	**Reserved**
8	1h RO	**PSI Full Duplex (PFD):** PSI Full Duplex
7:6	0h RO	**PSI Type (PLT):** PSI Type
5:4	3h RO	**Protocol Speed ID Exponent (PSIE):** Protocol Speed ID Exponent
3:0	4h RO	**Protocol Speed ID Value (PSIV):** Protocol Speed ID Value

17.2.153 XECP SUPP USB3_5 (XECP_SUPP_USB3_5) - Offset 8034h

XECP SUPP USB3_5.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8034h	000A4135h

Bit Range	Default & Access	Field Name (ID): Description
31:16	000Ah RO	**Protocol Speed ID Mantissa (PSIM):** Protocol Speed ID Mantissa
15:14	1h RO	**link Protocol (LP):** link Protocol
13:9	0h RO	**Reserved**
8	1h RO	**PSI Full Duplex (PFD):** PSI Full Duplex
7:6	0h RO	**PSI Type (PLT):** PSI Type
5:4	3h RO	**Protocol Speed ID Exponent (PSIE):** Protocol Speed ID Exponent
3:0	5h RO	**Protocol Speed ID Value (PSIV):** Protocol Speed ID Value

17.2.154 XECP SUPP USB3_6 (XECP_SUPP_USB3_6) - Offset 8038h

XECP SUPP USB3_6.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8038h	04E00126h

Bit Range	Default & Access	Field Name (ID): Description
31:16	04E0h RO	**Protocol Speed ID Mantissa (PSIM):** Protocol Speed ID Mantissa
15:9	0h RO	**Reserved**
8	1h RO	**PSI Full Duplex (PFD):** PSI Full Duplex
7:6	0h RO	**PSI Type (PLT):** PSI Type
5:4	2h RO	**Protocol Speed ID Exponent (PSIE):** Protocol Speed ID Exponent
3:0	6h RO	**Protocol Speed ID Value (PSIV):** Protocol Speed ID Value

17.2.155 XECP SUPP USB3_7 (XECP_SUPP_USB3_7) - Offset 803Ch

XECP SUPP USB3_7.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 803Ch	09C00127h

Bit Range	Default & Access	Field Name (ID): Description
31:16	09C0h RO	**Protocol Speed ID Mantissa (PSIM):** Protocol Speed ID Mantissa
15:9	0h RO	**Reserved**
8	1h RO	**PSI Full Duplex (PFD):** PSI Full Duplex
7:6	0h RO	**PSI Type (PLT):** PSI Type
5:4	2h RO	**Protocol Speed ID Exponent (PSIE):** Protocol Speed ID Exponent
3:0	7h RO	**Protocol Speed ID Value (PSIV):** Protocol Speed ID Value

17.2.156 XECP SUPP USB3_8 (XECP_SUPP_USB3_8) - Offset 8040h

XECP SUPP USB3_8.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8040h	13800128h

Bit Range	Default & Access	Field Name (ID): Description
31:16	1380h RO	**Protocol Speed ID Mantissa (PSIM):** Protocol Speed ID Mantissa
15:9	0h RO	**Reserved**
8	1h RO	**PSI Full Duplex (PFD):** PSI Full Duplex
7:6	0h RO	**PSI Type (PLT):** PSI Type
5:4	2h RO	**Protocol Speed ID Exponent (PSIE):** Protocol Speed ID Exponent
3:0	8h RO	**Protocol Speed ID Value (PSIV):** Protocol Speed ID Value

17.2.157 XECP SUPP USB3_9 (XECP_SUPP_USB3_9) - Offset 8044h

XECP SUPP USB3_9.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8044h	05B10129h

Bit Range	Default & Access	Field Name (ID): Description
31:16	05B1h RO	**Protocol Speed ID Mantissa (PSIM):** Protocol Speed ID Mantissa
15:9	0h RO	**Reserved**
8	1h RO	**PSI Full Duplex (PFD):** PSI Full Duplex
7:6	0h RO	**PSI Type (PLT):** PSI Type
5:4	2h RO	**Protocol Speed ID Exponent (PSIE):** Protocol Speed ID Exponent
3:0	9h RO	**Protocol Speed ID Value (PSIV):** Protocol Speed ID Value

17.2.158 XECP SUPP USB3_10 (XECP_SUPP_USB3_10) - Offset 8048h

XECP SUPP USB3_10.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8048h	0B63012Ah

Bit Range	Default & Access	Field Name (ID): Description
31:16	0B63h RO	**Protocol Speed ID Mantissa (PSIM):** Protocol Speed ID Mantissa
15:9	0h RO	**Reserved**
8	1h RO	**PSI Full Duplex (PFD):** PSI Full Duplex
7:6	0h RO	**PSI Type (PLT):** PSI Type
5:4	2h RO	**Protocol Speed ID Exponent (PSIE):** Protocol Speed ID Exponent
3:0	Ah RO	**Protocol Speed ID Value (PSIV):** Protocol Speed ID Value

17.2.159 XECP SUPP USB3_11 (XECP_SUPP_USB3_11) - Offset 804Ch

XECP SUPP USB3_11.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 804Ch	16C6012Bh

Bit Range	Default & Access	Field Name (ID): Description
31:16	16C6h RO	**Protocol Speed ID Mantissa (PSIM):** Protocol Speed ID Mantissa
15:9	0h RO	**Reserved**
8	1h RO	**PSI Full Duplex (PFD):** PSI Full Duplex
7:6	0h RO	**PSI Type (PLT):** PSI Type
5:4	2h RO	**Protocol Speed ID Exponent (PSIE):** Protocol Speed ID Exponent
3:0	Bh RO	**Protocol Speed ID Value (PSIV):** Protocol Speed ID Value

17.2.160 Host Control Scheduler (HOST_CTRL_SCH_REG) - Offset 8094h

Host Control Scheduler.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8094h	00C08140h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Disable repeat scheduler service of usb2 periodic (SCH_USB2_PRDC):** Disable repeat scheduler service of usb2 periodic
30:27	0h RW	**Enable scheduler limiter functions to block async. traffic types across ports while periodic pending (SCH_BLOCK_ASYNC):** Enable scheduler limiter functions to block async. traffic types across ports while periodic pending
26	0h RW	**Enable pkt pending notification to usb3 ports (EN_PP_NTFC_USB3):** Enable pkt pending notification to usb3 ports
25	0h RW	**disable async. burst limitation while periodic in progress (DIS_ASYNC_BURST):** disable async. burst limitation while periodic in progress
24	0h RW	**Disable marking overlap flag on all TT periodic INs. (DIS_OVERLAP_TT_PERIODIC):** Disable marking overlap flag on all TT periodic INs.
23	1h RW	**disable blocking of async. scheduling while periodic active to same port (DIS_BLOCK_ASYNC_PER_ACT):** disable blocking of async. scheduling while periodic active to same port
22	1h RW	**Setting this bit enables pipelining of multiple OUT EPs (EN_PIPELINE_MULTIPLE_OUT):** Setting this bit enables pipelining of multiple OUT EPs (across diff ports). This will help boost the performance for multiple ports OUT test case
21	0h RW	**Enable stop serving packets to disabled port (EN_STOP_SERVE_DIS_PORT):** Enable stop serving packets to disabled port

Bit Range	Default & Access	Field Name (ID): Description
20:17	0h RW	**TTE Host Control (TTE_HOST_CTRL):** (0): disable interrupt complete split limit to 3 microframes (1): disable checking of missed microframes (2): disable split error request w/NULL pointer on speculative INs with data payload and no TRB. (3): disable deferred split error request on speculative IN with data payload and no TRB. (7:4): reserved
16	0h RW	**disable deferred split error request on speculative IN with data payload and no TRB. (DIS_DEFFER_SPLIT_ERR):** disable deferred split error request on speculative IN with data payload and no TRB.
15	1h RW	**TTE: disable split error request w/NULL pointer on speculative INs with data payload and no TRB. (TTE_DIS_SPLIT_ERR_IN_DATA_NO_TRB):** TTE: disable split error request w/NULL pointer on speculative INs with data payload and no TRB.
14	0h RW	**TTE: Disable checking of missed microframes (DIS_MISSED_UFRAME_CHECK):** TTE: Disable checking of missed microframes
13	0h RW	**TTE: Disable interrupt complete split limit to 3 micro frames (DIS_INTER_SPLIT_LIMIT):** TTE: Disable interrupt complete split limit to 3 micro frames
12:11	0h RW	**Cache Size Control Reg (CACHE_SZ_CTRL):** 0: 64 1: 32 2,3: 16
10:9	0h RW	**Maximum EP Per Slot (MAX_EP_SLOT):** 0: 32 1: 16 2: 8 3: 4
8	1h RW	**Turn on scratch_pad_en (TO_SCRATCH_PAD_EN):** Cmd Mgr: Enables scratch pad function
7	0h RW	**Scheduler Host Control Reg (STOP_SCH_UNCON):** Enable check to stop scheduling on port that is not connected
6	1h RW	**Disable 1 pack scheduling limit when ISO pending in present microframe (DIS_SCH_LIMIT):** Disable 1 pack scheduling limit when ISO pending in present microframe
5:4	0h RW	**scheduler sort pattern (SCH_SORT_PATTERN):** 00 (default) search ISO ahead of interrupt within each service interval 01 - search USB2-ISO, USB3-ISO, USB2-Interrupt, USB3-Interrupt within each service interval 10 - search strictly by interval 11 - search all ISO intervals ahead interrupt intervals and within each interval, USB2 ahead of USB3
3	0h RW	**Enable TTE overlap prevention on interrupt OUT EPs (at cost of possible service interval slip (EN_TTE_OVERLAP_PREV_OUT):** Enable TTE overlap prevention on interrupt OUT EPs (at cost of possible service interval slip

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Enable TTE overlap prevention on interrupt IN EPs (at cost of possible service interval slip (EN_TTE_OVERLAP_PREV_IN):** Enable TTE overlap prevention on interrupt IN EPs (at cost of possible service interval slip
1	0h RW	**Disable TRM active IN EP valid check function (DIS_TRM_ACT_IN_VALID):** Disable TRM active IN EP valid check function
0	0h RW	**Disable poll delay function (DIS_POLL_DELAY):** Scheduler: Disable poll delay function

17.2.161 Power Management Control (PMCTRL_REG) - Offset 80A4h

Power Management Control.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 80A4h	492D5094h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Async PME Source Enable (ASYNC_PME_SRC_EN):** This field allows the async PME source to be allowed to generate PME. This is specifically required for SOCs that do not allow for any clock other than RTC to be available during RTD3.
30	1h RW	**Legacy PME Source Enable (LEGACY_PME_SRC_EN):** This field allows the legacy PME source to be used in PME generation. The legacy source in reference to the source prior to the RTD3 changes.
29	0h RW	**Reset Warn Power Gate Trigger Disable (RESET_WARN_PWR_GATE_TRIGGER_DISABLE):** This field controls the actions taken for due to reset warn. 0 - Reset Warn will trigger a HW autonomous Power Gate 1 - Reset Warn will not trigger a HW autonomous Power Gate
28	0h RW	**CLR_PME_FLAG_PULSE_AUX_CCLK:** Internal PME flag Clear This Write-Only bit can be used to clear the internal PME flag. SW writes to 1 will clear the PME flag. SW writes to 0 will have no effect and be ignored by the controller. Read always return 0
27	1h RW	**Disable RTD3 power gating when in D3 (DIS_D3_PG):** Disable RTD3 power gating when in D3 and context save operation is not performed
26	0h RW	**XLFPSCOUNTSRC:** XLFPSCOUNTSRC (Source for LFPS OFF Counter) 0: Central RTC Counter for LFPS detection 1: Local Counter for LFPS detection
25	0h RW	**XELFPSRTC:** XELFPSRTC (Enable LFPS Filtering on RTC) 0: Use Oscillator clock for LFPS Filtering during P3 1: Use RTC Clock for LFPS Filtering during P3

Bit Range	Default & Access	Field Name (ID): Description
24	1h RW	**XMPHYSPGDD0I2:** XMPHYSPGDD0I2 (ModPhy Sus Well Power Gate Disable for D0I2) 0: Modphy sus well power gating enabled 1: Modphy sus well power gating disabled
23	0h RW	**XMPHYSPGDD0I3:** XMPHYSPGDD0I3 (ModPhy Sus Well Power Gate Disable for D0I3) 0: Modphy sus well power gating enabled 1: Modphy sus well power gating disabled
22	0h RW	**XMPHYSPGDRTD3:** XMPHYSPGDRTD3 (ModPhy Sus Well Power Gate Disable for RTD3) 0: Modphy sus well power gating enabled 1: Modphy sus well power gating disabled
21:18	Bh RW	**XD3RTCPTTM:** XD3RTCPTTM (D3 RTC Port Timer Tick Multiplier) This register will be the multiplication factor for determining Wake Detection Frequency and RXDET based on the XD3RTCPTTC value. If XD3RTCPTTC is 9h and this register is Bh, frequency for RXDET and H8EXIT detection while MODPHY SUS Power gating is enabled would be 99ms.
17	0h RW	**U3 LFPS Periodic Sampling ON Time Control (U3_LFPS_PRDC_SAMPLING_ON_TIME_CTRL):** This field controls the ON time for the LFPS periodic sampling for USB3 ports. 0 ON time is 2 rtc clocks 1 ON time is 3 rtc clocks Note: This field is ignored if USB3 PHY SUS Well Power Gating is enabled.
16	1h RW	**AON LFPS Detector Enable Mode (AON_LFPS_DETECTOR_EN_MODE):** 1 - Allow the LFSP Detector in AON to own LFPS detection when the port is in PS3 for U2/U3 - not RxD regardless of port ownership. 0 - Allow the LFPS Detector in AON to own the LFPS detection only when the AON owns the port and in U2/U3 - not RxD
15:8	50h RW	**SS U3 LFPS Detection Threshold (SS_U3_LFPS_DETECTION_THRESHOLD):** This field controls the threshold used to determine when a valid U3 Wake is detected through when using the unfiltered LFPS source. The value on this field will reflect the binary count required to have been detected on the counter being clocked by the unfiltered lfps source to result in a valid U3 wake detection.
7:4	9h RW	**SS_U3_LFPS_PRDC_SAMPLING_OFFTIME_CTRL:** This field controls the OFF time for the LFPS periodic sampling for USB3 Ports 0x0 periodic sampling is disabled. 0x1 OFF time is 1ms 0x2 OFF time is 2ms 0xF OFF time is 15ms The ON Time is determined by the amount of time required to reliably determine if there is a valid LFPS and is HW implementation specific. A speed up mode shall be implemented where this field is in units of us. i.e. 0x1 = 1 us OFF time, 0x2 = 2 us OFF time, etc.
3	0h RW	**PS3 LFPS Source Select (PS3_LFPS_SRC_SEL):** 0 LFPS Source is unfiltered 1 LFPS Source is filtered (Rx-Elec-Idle) LFPS Source is Rx-Elec-Idle for any non PS3 state.

Bit Range	Default & Access	Field Name (ID): Description
2	1h RW	**XHCI Engine Autonomous Power Gate Exit Reset Policy (XHC_AUTO_PWRGATE_EXITRST_POLICY):** Controls when the xHCI engine is brought out of reset due to a power ungate. 0 Engine is brought out of reset when D3 to D0 is triggered. This allows for a quick power up sequence while leaving the virtual PCIe LTSSM in L23 is power ungate is not due to D3 to D0. 1 Engine is brought out of reset along with the rest of the IP. This is required for PMC save/restore flow.
1	0h RW	**USB2 Port Wake Unit Coupling Policy (USB2_PORT_WAKE_COUPLING_POLICY):** Controls the trigger for USB2 Port Wake Units to initiate Port Level Power Off Preparation. 0 RTD3 triggered 1 - Port Triggered when in L1, L2 or Disabled, Disconnected
0	0h RW	**USB3 Port Wake Unit Coupling Policy (USB3_PORT_WAKE_COUPLING_POLICY):** Controls the trigger for USB3 Port Wake Units to initiate Port Level Power Off Preparation. 0 - RTD3 Triggered 1 - Port Triggered when in PS3 due to RxDetect, U3, U2 or Disabled

17.2.162 Host Controller Misc Reg (HOST_CTRL_MISC_REG) - Offset 80B0h

Host Controller Misc Reg.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 80B0h	0080037Fh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**USB2_LTRUPDT_DIS:** This controls the inclusion of the USB2 LTR based on link state. Setting this bit will disable USB2 LTR and will expose a NO Requirement from USB2 thus not impacting the aggregated LTR value for the controller.
30	0h RW	**USB2 Line State Debounce During Port Reset Policy (USB2_LINE_STATE_DEBOUNCE_DURING_PORT_RESET_POLICY):** This register controls how the debounce is enforced during the Port Reset phase. 0 do not enable the line state debounce during port reset. 1 enable the line state debounce during port reset.
29	0h RW	**TTE PEXE Credit Fix Disable (TTE_PEXE_CREDIT_FIX_DISABLE):** When set, it disables a fix implemented to re-deem PEXE credits when a port is disconnected
28	0h RW	**TTE Scheduling policy (TTE_SCHEDULING_POLICY):** This register controls a fix made to prevent over-scheduling by not account for 188B in each uFrame. Setting this bit will disable the fix and allow for over-scheduling.

Bit Range	Default & Access	Field Name (ID): Description
27	0h RW	**USB3 ITP Delta Timer Source Select (USB3_ITP_DELTA_TIMER_SOURCE_SELECT):** This register selects the source for the delta timer tracking used for ITP generation. 0 the source is a 16.666 ns tick generated from a crystal reference clock 1 - the source is a 16.666 ns tick generated from the aux_cclk. This field needs to remain in sync with Frame Timer Source Select to ensure the are both set or both cleared. There is no support for any other combination.
26	0h RW	**Frame Timer Source Select (FRAME_TIMER_SOURCE_SELECT):** This register controls the source for the frame timer. 0 the source for the frame timer is a crystal reference clock 1 the source for the frame timer is the aux_cclk.
25	0h RW	**uFrame Masking Enable (UFRAME_MASKING_ENABLE):** If set, enables the uFrame tick to be masked due to ports being in U3/NC. This controls a fix made to disable the auto masking of uFrame tick due to port state w/o any pipeline idle condition. When cleared, it rely on gating of frame timer due to proper port state and idleness tracking from the pipeline.
24	0h RW	**Late FID Check Disable (LATE_FID_CHECK_DISABLE):** This register disables the Late FID Check performed when starting an ISOCH stream.
23	1h RW	**Late FID TTE count adjust Disable (DIS_LATE_FID_TTE_CNT_ADJ):** 0 the value of frame late skip count starts at 1 for TTE eps and 0 for non tte eps. this represents an adjustment for the number of SI missed 1 the value of frame late skip count starts at 0 for both TTE eps and non tte eps
22	0h RW	**Late FID difference calculation legacy (DIS_DIF_CAL_LEGACY):** 0 late uframeid uses the new difference calculation to compute how may SI the TD is late 1 late uframeid uses the legacy difference calculation to compute how may SI the TD is late
21	0h RW	Reserved
20	0h RW	Reserved
19	0h RW	**USB2 Resume Cx Inhibit Disable (USB2_RESUME_CX_INHIBIT_DISABLE):** Controls if USB2 L1 Resume is allowed to contribute to DMA Active which will inhibit Cx state. 0 USB2 L1 Resume is allowed to inhibit Cx via DMA Active 1 USB2 L1 Resume is NOT allowed to inhibit Cx via DMA Active When cleared, Cx will only be inhibited when the DMA traffic for the port begins.
18	0h RW	**LATE_FID_TTE_DIS:** Late FID TTE Disable 0: Late Frame ID Check is enabled for TTE Endpoints 1: Late Frame ID Check is disabled for TTE Endpoints

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Late FID uframe Check Disable (LATE_FID_UFRAME_CHK_DIS):** 0 Frame ID Match only asserts in uframe 7 for non-TTE Endpoints Frame before match 1 Frame ID Match can assert in any uframe
16	0h RW	**Late FID Extra Interval (LATE_FID_EXTRA_INTER):** This register controls the extra number of intervals added onto the advancing of late FID check essentially a bias used to correct for possible errors in implementation
15:0	037Fh RW	**Valid Isoch Scheduling Range (VALID_ISOCH_SCHEDULING_RANGE):** This register defines the window in milliseconds from the current Frame that will be considered for scheduling in an upcoming Frame. Anything scheduled outside of this window will be considered as late and will trigger the Missed Service Error.

17.2.163 Host Controller Misc Reg2 (HOST_CTRL_MISC_REG2) - Offset 80B4h

Host Controller Misc Reg2.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 80B4h	10000184h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**MAX_SHORT_PKT_ADV_CNT:** Short Packet Advance Throttling 0 - Limit SPA to 4 TRB's 1 - Limit SPA to 16 TRB's 2 - limit SPA to 64 TRB's 3 - limit SPA to 128 TRB's 4 - limit SPA to 512 TRB's 5 - limit SPA to 1024 TRB's 6 - limit SPA to 2048 TRB's 7 - Disabled
28	1h RW	Reserved
27	0h RW	Reserved
26	0h RW	Reserved
25	0h RW	**LTM_BELT_VALID_CLR:** ltm_belt_valid_clr
24	0h RW	**CFG_TRM_DROP_SCH_REQ_DIS:** cfg_trm_drop_sch_req_dis
23	0h RW	**CFG_TRM_DROP_TTE_REQ_DIS:** cfg_trm_drop_tte_req_dis

Bit Range	Default & Access	Field Name (ID): Description
22	0h RW	**CFG_TRM_EDTLA_CLR_DIS:** cfg_trm_edtla_clr_dis
21	0h RW	**CFG_XFER_IS_SERVE_CHK_EN:** Enable checking is_serve condition in XFER, mainly for undoing fix if needed
20	0h RW	**CFG_CPL_NPKT0_FC_DIS:** Set low to allow receiving ACK with NUMP>0 to bring the TRM out of Remote Flow Control
19:18	0h RO	**Reserved**
17	0h RW	**Disable IDT credit leak fix (CFG_DIS_ODMA_IDT_CRD_LEAK_FIX):** Disable the IDT credit leak fix in odma. 0 Fix is enabled 1 Fix is disabled
16	0h RW	**CFG_IDMA_TTYPE_CHK_DIS:** Set to disable packet Transfer Type checking in IDMA
15	0h RW	**HC Reset Controller Isolation Disable (HCRST_CTRL_ISOL_DISABLE):** Setting this bit to 1 will disable the HC Reset based quiescing/isolation flow
14	0h RW	**DISABLE_IDMA_PERF_FIX:** Fix is enabled by default 0 - fix is enabled 1 - fix is disabled
13	0h RW	**EN_HH_FRINDEX_NOT_RUN:** enable_hh_frindex_not_run
12	0h RW	Reserved
11	0h RW	Reserved
10	0h RW	Reserved
9	0h RW	**EN_100MS_WATCH_DOG_TIMER:** 100ms Watch Dog Timer When set, it will enable 100ms Watch Dog Timer for Aux PM FSM for phystatus assertion else watch dog timer is 300ms.
8	1h RW	**EN_WATCH_DOG_TIMER:** Enable Watch Dog Timer: When set, it will enable 100/300ms watch dog timer for AUX PM FSM for phystatus assertion
7	1h RW	**EN_SSP_ISOC_PIPELINING:** enable isoc pipelining feature for ssp devices 1:enable the feature 0:disable the feature
6	0h RW	**DISABLE_TCG_UNGATE_ON_FLUSH:** When set, it will ungate the trunk clock gating for PIPE clock when there is flush when DBC/EXI HHH is not idle.
5	0h RW	**DISABLE_VNN_FRAME_TIMER:** Frame Timer Select This register defines the frame timer used for all frame timer derived ticks. 0 - Frame timer in the VNN is the source for all frame timer related tracking. 1 - Frame timer in the Gated VNN is the source for all frame timer related tracking.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**DISABLE_CLR_CCS_ON_CAS_SET:** Clear CCS on CAS When set, XHCI port will not clear the CAS when CCS is set. (BUGDE 5076358)
3	0h RW	**DISABLE_RHUB_PARK_AT_DBCDISC:** On Default Enables Root Hub s/m to arc to DBC_DISCONNECTED from ERROR and RESET states if the reason to enter into those state was a prior connection failure to exchange Link Capabilities Set 1 Keep the Root hub s/m in ERROR or RESET as the case may be , on a successful connection as a DBC if the first attempt was failed due to PortConfigTimeout
2	1h RW	**DISABLE_BLOCK_WPR_ON_DISPORTS:** Warm Port Reset on Disconnected Port Disable When set, disables the generation of a WPR on a disconnected port.
1:0	0h RW	**HOST_CTRL_MISC_REG2_1_0:** Reserved

17.2.164 Super Speed Port Enable (SSPE_REG) - Offset 80B8h

Super Speed Port Enable.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 80B8h	C0000000h

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**SS_CFG_BLOCK_PWRDWN_4_ACT_LFPS:** Delay power down entry if Rx LFPS is active. Setting this bit will block the controllers power down entry seq (for Sx/D3/D0i2 etc) if Rx LFPS is active. The power down entry will happen once a device stops sending LFPS.
30	1h RW	**DIS_CLR_CCS_4_HCRESET:** Enable Clearing of CCS for HCReset - Setting this bit clears the USB3 ports PORTSC.CCS bit upon HCReset.
29	0h RW	**DISABLE_RAWLFPS_BASED_WAKE_FIX:** Disable Raw Lfps Detection Based Wake from P3 This bit is used to disable RTL fix provided to separate RawLFPS and RxElecIDle detection 0: Transition port to RESUME based on raw LFPS detection 1: Transition port to RESUME based Filtered RxElecIdle detection

Bit Range	Default & Access	Field Name (ID): Description
28	0h RW	**EXI OVERRIDE DISABLE (EXI_OVERRIDE_DIS):** EXI Override Disable
27:4	0h RO	**Reserved**
3:0	0h RW	**SSPE_REG:** USB3 Port Enable This field controls whether SuperSpeed capability is enabled for a given USB3 port. When set to 1, Enables SS termination Enables PORTSC to see the connects on the ports. When set to 0, Disables SS termination Blocks PORTSC from reporting attach/connect. Places port in the lowest power state.

17.2.165 AUX Power Management Control (AUX_CTRL_REG1) - Offset 80E0h

AUX Power Management Control.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 80E0h	8080BCE0h

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**D3 Hot function enable register (D3_HOT_FXN_EN):** This bit is from pin input which is set 1. But it allows software to alter it if it is needed. 1: D3 hot enabled 0: D3 hot not able.
30	0h RW	**Allow L1 Core Clock Gating (ALL_L1_CORE_CG):** When set to 1 allows core clock being gated during L1 state.
29	0h RW	**Allow Engine PHY Status Extension (AL_EP_SEXT):** When set to 1 allows the engine to extend PHY status of PCIe PIPE for one more cycle. This is due to the fact that our rate change function has a potential of not being able to sample the phystatus signal.
28	0h RW	**Allow Engine PCIe Rate Change Passing (ALL_EP_RCP):** When set to 1 allows the engine to pass PCIe rate change signal as it is from PCIe core to PCIe PHY.
27	0h RW	**Allow Engine PERST Fundamental Reset (AL_PERST_FRST):** When set to 1 allow engine to treat PERST# as a fundamental reset
26	0h RW	**Overwrite PCIe P2 to P1 (OVR_PCIE_P2_P1):** When set to 1 will overwrite a PCIe powerdown state of P2 to P1.
25	0h RW	**Set Internal SSV 1 (SET_ISSV_1):** When set to 1 set the internal SSV to 1.
24	0h RW	**Clear Internal SSV 0 (CLR_ISSV_0):** When set to 1 clear the internal SSV to 0.

Bit Range	Default & Access	Field Name (ID): Description
23	1h RW	**Enable save_restore_enable SW Loading (EN_SRE_SW_LD):** This is a bit that enables the save_restore_enable signal being loaded when a software command has set Save bit. This is a debug function.
22	0h RO	**Reserved**
21	0h RW	**Force save_restore 1 (FORCE_SR1):** When set to 1, it will force the save_restore flag to 1. This flag is an bit to ensure that have masked the update during low power state. If software write this bit to 1, it must write it to 0 in order to resume the normal save and restore function.
20	0h RW	**CFG DISABLE_WARM_RST_DET_specUpPorts (CFG_DIS_WRSTDET_SPECU):** 0: Speculative upstream for Debug and SS/SSP port will detect WPR 1: No speculative upstream till port configuration is completed
19	0h RW	**cfg iob drivestrength[1] (CIDS1):** Controls the drive strength of the IO buffer
18	0h RW	**cfg iob drivestrength[0] (CIDS0):** Controls the drive strength of the IO buffer
17	0h RW	**CFG_DIS_ARC_RXDP3:** When set to '1' DIsables arc to RXDET_p3 on disc from U2P3/U3
16	0h RW	**cfg clk gate dis (CCGD):** 1: Disable USB3 port clock gating 0: Enable USB3 port clock gating
15	1h RW	**Enable CFG RXDET P3 (EN_CFG_RDP3):** When set to '1' enable cfg rxdet p3
14	0h RW	**Enable CFG PIPE Reset (EN_CFG_PIPE_RST):** When set to '1' enable cfg pipe rst
13	1h RW	**Enable Filter TX Idle (EN_FILT_TX_IDLE):** When set to 1 enables a filter function to TX electrical idle signal at PCie PIPE. There have a filter that will set TXelecidle signal of PCIe PIPE to 1 whenever in isolation state or power down transition states.
12	1h RW	**Enable Host Engine Generate PME (EN_HE_GEN_PME):** This is a global switch to whether or not able this host engine to generate PME message.
11	1h RW	**Enable Isolation (EN_ISOL):** When set to '1' enable isolation
10	1h RW	**Enable L1 Caused P2 Overwrite (EN_L1_P2_OVR):** Set 1 to enable a new feature. This new feature is designed to use L1 as a state to identify whether it should do P2 Overwrite or not. It used to use P1 state to identify whether or not to invoke P2 overwrite function.
9	0h RW	**Enable Core Clock Gating (EN_CORE_CG):** When set to '1' disable core clock gating based on low power state entered
8	0h RW	**Enable PHY Status Timeout (EN_PHY_STS_TO):** When set to '1' enable PHY status timeout function which is designed to cover the PCIePHY issue that may have not able to detect the PHY status toggle.
7	1h RW	**Ignore aux_pm_en PCIe Core (IGN_APE_PC):** When set to '1' ignore the aux_pm_en reg from PCIe core to continue the remote wake/clock switching support
6	1h RW	**Enable P2 Overwrite P1 (EN_P2_OVR_P1):** When set to '1' enable P2 overwrite P1 when PCIe core has indicated the transition from P0 to P1. This is to enable entering the even lower power state.

Bit Range	Default & Access	Field Name (ID): Description
5	1h RW	**Enable P2 Remote Wake (EN_P2_REM_WAKE):** When set 1 '1' enable the remote wake function by allowing P2 clock/switching and P2 entering
4:1	0h RW	**Forced PM State (FORCED_PM_STATE):** Forced PM state
0	0h RW	**Initiate Force PM State (INIT_FPMS):** When set to '1' force PM state to go to the state indicated in bit 4:1

17.2.166 SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG) - Offset 80ECh

SuperSpeed Port Link Control.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 80ECh	18020C00h

Bit Range	Default & Access	Field Name (ID): Description
31:27	03h RW	**Force LTSSM State (FORCE_LTSSM_ST):** LTSSM state to be forced This value is for test purpose only.
26	0h RW	**Direct Link LTSSM State (DL_LTSSM_ST):** 0: Normal operation mode 1: Direct link to a specific state specified by bit 31:27 This bit is for test purpose only. It shall be written 0 in normal operation mode.
25	0h RW	**Direct Link To U0 (DL_U0):** 0: Normal operation mode 1: Direct link to U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
24:21	0h RW	**Forced Compliance Pattern (FORCED_CMP_PAT):** Compliance pattern to be forced to enter compliance mode This value is for test purpose only.
20	0h RW	**Enable Link Error Slave Count (EN_LES_CNT):** 0: Disable link error slave count 1: Enable link error slave count
19	0h RW	**TS rcv to complete U1/U2/U3 exit LFPS handshake (TS_RCV_UX_EXIT_LFPS_HS):** 1: enable TS receive to complete U1/U2/U3 exit LFPS handshake 0: disable TS receive to complete U1/U2/U3 exit LFPS handshake
18	0h RW	**EN_LOGIC_TO_EXIT_POLLCONF_AND_RECCONF:** 1: enable logic idle receive to exit Polling.Configuration and Recovery.Configuration 0: disable logic idle receive to exit Polling.Configuration and Recovery.Configuration
17	1h RW	**PORT_INTIL_TIMEOUT_VAL:** This bit specifies the port initialization timeout value. 1: 20us - 21us 0: 19us - 20us

Bit Range	Default & Access	Field Name (ID): Description
16:15	0h RW	**PHY Low Power Latency (PHY_LP_LAT):** This field defines the latency to drive the PHY to enter low power mode 0: 4 cycles 1: 8 cycles 2: 16 cycles 3: 32 cycles
14:12	0h RW	**Link Recovery Minimum Time (LR_MIN_TM):** This value defines the minimum time for the link to stay in Recovery.Active other than from U3. The granuity is 128us.
11:9	6h RW	**Link Polling Minimum Time (LP_MIN_TM):** This value defines the minimum time for the link to stay in Polling.Active and Recovery.Active from U3. The granuity is 128us.
8	0h RW	**Force Link Accept PM Command (FORCE_LA_PMC):** 0: Normal operation mode 1: Force link to accept power management command
7	0h RW	**Direct Link Recovery U0 (DL_REC_U0):** 0: Normal operation mode 1: Direct link to Recovery from U0
6	0h RW	**Link Fast Training Mode (LINK_FTM):** 0: Normal operation mode 1: Link fast training mode This bit should be written 0 in normal operation.
5	0h RW	**Disable Link Scrambler (DIS_LINK_SCRAM):** 0: Enable link scrambler 1: Disable link scrambler
4	0h RW	**Direct Link U3 From U0 (DL_U3_U0):** 0: Normal operation mode 1: Direct link to U3 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
3	0h RW	**Direct Link U3 From U0 (DL_U2_U0):** 0: Normal operation mode 1: Direct link to U2 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
2	0h RW	**Direct Link U3 From U0 (DL_U1_U0):** 0: Normal operation mode 1: Direct link to U1 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
1	0h RW	**Enable Link Loopback Master Mode (EN_LINK_LB_MAST):** 0: Disable link loopback master mode 1: Enable link loopback master mode
0	0h RW	**Disable Link Compliance Mode (DIS_LINK_CM):** 0: Enable link compliance mode 1: Disable link compliance mode

17.2.167 USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1) - Offset 80F0h

These set of registers is used to control key USB set of timers. They are spread over 4 registers each 32 bits wide.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 80F0h	314803A0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	31h RW	**FS/LS Mode SE0 Disconnect Delay[7:0] (FSLS_SE0_DIS_DEL_7_0):** # of microseconds of SE0 in FS/LS mode to register disconnect had occurred.
23	0h RW	**EN_SNPS_PHY_FIX:** Enable SNPS PHY Fix: 1: When set, term select will assert at the start of EOR. Fslsserialmode will also deassert at the same clock as txenb. 0: Legacy behavior for Intel PHY.
22	1h RW	**EN_L1_DISC_IN_L0:** Enable Pseudo L0 state when transition from L1 to L2 due to disconnect: 1: When set, {L1 suspendm, L2 suspendm} will go from 01->11->10 to allow the USB2 PHY to exit L1 and enter L2 for deeper PM 0: Legacy behavior (01->10)
21	0h RW	**DIS_PURGE_ON_SETUP_FIX:** To disable the fix for SETUP purge that match for both device address and endpoint number: 0: Only allow purge for SETUP when both device address and endpoint number are matched. 1: Revert back to old behavior that purge is allowed when either device address or endpoint number is matched.
20	0h RW	**L1_EXIT_RECOVERY_MODE:** Mode for extended L1 Exit recovery delay: 0: 12us 1: 50us
19	1h RW	**L1_TO_INCR_MODE:** Mode select for L1 Timeout increments: 0: time out increments is in 125us 1: L1 Timeout increments are in 256us. For additional details , USB2 PORTHLPMC.L1 Timeout in XHCI Spec.
18	0h RO	**Reserved**
17	0h RW	**EN_DETECT_NOMINAL_PKT_EOP:** 0: Detect minimal packet EOP. 1: Detect nominal packet EOP.
16	0h RW	**Disable Chirp Response (DIS_CHIRP_RESPONSE):** 0: Normal 1: Force full speed on host ports (disable chirp response)
15	0h RW	**Disable 192 Byte Limit Check (DIS_192B_LIM):** 0: Enforce 192 byte limit on complete-split INs. Treat any packet) 192 as babble case. 1: Disable 192 byte limit check.
14	0h RW	**External Provided FS/LS Disconnect (EXT_FSLS_DIS):** 0: Internal FS/LS Disconnect from linestate(1:0) 1: External provided FS/LS Disconnect from hostdisconnect input

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**UTMI Reset Source Select (UTMI_RST_SEL):** Select UTMI Reset Source (FRD UTMI Reset Only) 00: HCReset or Force PHY Reset or internal reset after disconnect/suspend for restart (default) 01,11: UTMI reset = ~UTMI suspendm 10: UTMI reset = ~UTMI suspendm and synchronization to port clk.
11	0h RW	**Disable HS Disconnect Window (DIS_HS_DIS_WIN):** 0: Enable HS Disconnect Window Function 1: Disable HS Disconnect Window Function
10	0h RW	**Disable Port Error Detection (DIS_PERR_DET):** 0: Enable Port Error Detection (default) 1: Disable Port Error Detection
9	1h RW	**Disable Peek Function for ISO-OUT (DIS_PF_IOUT):** 0: Enable Peek function for ISO-OUT (default) 1: Disable Peek function for ISO-OUT
8	1h RW	**Drive Resume-K FS/LS Serial Interface (DRV_RESK_FSLS_SER):** 0: Drive Resume-K on parallel Interface 1: Drive Resume-K directly on FS/LS Serial Interface (default)
7	1h RW	**Enable USB2 Drop-Ping (EN_U2_DROP_PING):** 0: Disable Drop-Ping Function in USB2 Protocol (default) 1: Enable Drop-Ping Function in USB2 Protocol
6	0h RW	**Enable USB2 Force-Ping (EN_U2_FORCE_PING):** 0: Disable Force-Ping Function in USB2 Protocol (default) 1: Enable Force-Ping Function in USB2 Protocol
5	1h RW	**Enable USB2 Auto-Ping (EN_U2_AUTO_PING):** 0: Disable Auto-Ping Function 1: Enable Auto-Ping Function in USB2 Protocol (default)
4	0h RW	**Disable PHY SuspendM (DIS_PHY_SUSM):** 0: PHY is suspend=U3,U2,disconnect (default) 1: Disable PHY SuspendM in All States
3	0h RW	**UTMI Internal Clock Gate Disable (UTMI_INT_CG_DIS):** 0: Normal operation (internal clock gated in U2, U3,disconnect) 1: UTMI Internal Clock Gate Disable
2	0h RW	**Disable PHY SuspendM in Disconnect State (DIS_PSUSM_DS):** 0: PHY is suspendM=0 in Disconnect State (default) 1: Disable PHY SuspendM in Disconnect State
1	0h RW	**Force PHY Reset (FORCE_PHY_RST):** 0: Normal Operation (default) 1: Force PHY Reset
0	0h RW	**USB2 Accelerated Simulation Timing (U2_ACC_SIM_TIM):** 0: Normal Operation (default - FPGA/ASIC) 1: USB2 Accelerated Simulation Timing (default - simulation)

17.2.168 USB2 Port Link Control 2 (USB2_LINK_MGR_CTRL_REG2) - Offset 80F4h

These sets of registers is used to control key USB set of timers. They are spread over 4 registers each 32 bits wide.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 80F4h	80C40620h

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**Total Reset Duration[0] (TOT_RST_DUR_0):** # of microseconds for total reset duration
30:18	0031h RW	**Chirp-K Duration (CHIRPK_DUR):** # of microseconds of Chirp-K to register that a device is chirping
17:5	0031h RW	**K/J Disconnect Connect Delay (KJ_DIS_CON_DEL):** # of microseconds of K/J in disconnected state to register connect has occurred.
4:0	00h RW	**FS/LS Mode SE0 Disconnect Delay[12:8] (FSLS_SE0_DIS_DEL_12_8):** # of microseconds of SE0 in FS/LS mode to register disconnect had occurred.

17.2.169 USB2 Port Link Control 3 (USB2_LINK_MGR_CTRL_REG3) - Offset 80F8h

These sets of registers is used to control key USB set of timers. They are spread over 4 registers each 32 bits wide.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 80F8h	F865EB6Bh

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RW	**U2 Entry Ignore Linestate Changes Duration[3:0] (U2_IGN_LS_DUR_3_0):** # of microseconds after entering U2, linestate changes are ignored as bus settles
27:15	10CBh RW	**U3 Entry Ignore Linestate Changes Duration (U3_IGN_LS_DUR):** # of microseconds after entering U3, linestate changes are ignored as bus settles
14:0	6B6Bh RW	**Total Reset Duration[15:1] (TOT_RST_DUR_15_1):** # of microseconds for total reset duration

17.2.170 USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4) - Offset 80FCh

These sets of registers is used to control key USB set of timers. They are spread over 4 registers each 32 bits wide.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 80FCh	02008003h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:27	0h RW	**ADD_GB_4_L1_PREWAKE:** additional guardband for L1 advance prewake. 00 = +0 us 01 = +1uF 10 = +2uF 11 = +4uF
26	0h RW	**select L1 min idle duration that will be driven to Scheduler. Either drive '0' or based on L1 Timeout value (SEL_L1_MIN_IDLE):** select L1 min idle duration that will be driven to Scheduler. Either drive '0' or based on L1 Timeout value
25	1h RW	**Enable periodic_prewake to prevent L1 entry if in U0, or wake from L1 if already in U2. (EN_PER_PREWAKE):** Enable periodic_prewake to prevent L1 entry if in U0, or wake from L1 if already in U2.
24:22	0h RO	**Reserved**
21:9	0040h RW	**U2 Detect Remote Wake Delay (U2D_RWAKE_DEL):** #of microseconds after detecting U2 remote wake condition to reflect K
8:0	003h RW	**U2 Entry Ignore Linestate Changes Duration[12:4] (U2_IGN_LS_DUR_12_4):** # of microseconds after entering U2, linestate changes are ignored as bus settles

17.2.171 Power Scheduler Control-0 (PWR_SCHED_CTRL0) - Offset 8140h

Power Scheduler Control-0.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8140h	0A019132h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0Ah RW	**Engine Idle Hysteresis (EIH):** This register controls the min. idle span that has to be observed from the engine idle indicators before the power state flags (xhc_*_idle) will indicate a 1.
23:12	019h RW	**Backbone PLL Shutdown Advance Wake (BPSAW):** This register controls the time before the next scheduled transaction where the Backbone PLL request will assert. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124)
11:0	132h RW	**Backbone PLL Shutdown Min. Idle Duration (BPSMID):** The sum of this register plus the Backbone PLL Shutdown Advance Wake form to a Total Idle time. When the next scheduled periodic transaction is after present time + Total Idle, the Backbone PLL request will de-assert, allowing the PLL to shutdown. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124)

17.2.172 Power Scheduler Control-1 (PWR_SCHED_CTRL2) - Offset 8144h

These bit enable by EP type those EPs classes that are considered for determining next periodic active interval for pre-wake of the periodic_active signal. EP classes that are disabled may never be observed in setting of the periodic_active signal.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8144h	0000023Fh

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26	0h RW	**Disable Power Scheduler wait for inprogress NDE (DISABLE_INPROG_NDE_WAIT):** Policy for controlling transition of LTR_STATE_* FSM to move from ACTIVE to *_INACTIVE states 0: LTR_STATE_* FSM will wait for in progress NDE message to complete before transitioning to one of the INACTIVE states 1: LTR_STATE_* FSM will not wait for in progress NDE message to complete before transitioning to one of the INACTIVE states
25	0h RW	**Disable sending NDE sideband messages with NoREQ (NDE_SBMSG_NOREQ_DIS):** Policy to disable sending NOREQ NDE sideband messages 0: Controller will send NOREQ NDE sideband messages 1: Controller will not send NOREQ NDE sideband messages
24	0h RW	**Enable NDE sideband messaging (NDE_SBMSG_EN):** Policy to enable NDE Sideband messaging. 0: Controller is not allowed to send NDE sideband messages 1: Controller is allowed to send NDE Sideband messages
23:21	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**Revert LPM Hysteresis Clear (RVRT_LPM_HYS_CLR):** 0: The per-port periodic active signal from the Scheduler is used to reset the per-port hysteresis loop for the LPMs. 1: The global pwr_sch_xhc_engine_prdc_idle signal is used to reset all of the per-port hysteresis loops for LPM. This is the legacy behavior. Note: This bit was created for GEN2.
19	0h RO	**Reserved**
18	0h RW	**Flow-Controlled SS INTR 2SI Mode (FLOW_CTRL_2SI_MODE):** 0: The Power Scheduler will Schedule all Flow-Controlled SS INTR Endpoint's alarm to the SI determined by the Endpoint's Interval value. 1: The Power Scheduler will Schedule all Flow-Controlled SS INTR Endpoint's alarm to twice the SI determined by the Endpoint's Interval value. Note: This bit was created for GEN2.
17	0h RW	**d0i2 Clear Alarm Fix Disable (D0I2_CLR_ALARM_FIX_DISAB):** d0i2 Clear Alarm Fix Disable
16	0h RW	**No Doorbell Clear Valid Disable (NO_DB_CLR_VAL_DISAB):** No Doorbell Clear Valid Disable
15	0h RW	**Disable BELT Latch (DISAB_BELT_LATCH):** 1: The Power Scheduler's interface to the LTR Manager signals BELT and No_Requirement are not latched with the Request signal and can change before Halt is deasserted. Asserting this bit will disable the fix. 0: The Power Scheduler's interface to the LTR Manager signals BELT and No_Requirement are latched when the Request signal is asserted and will remain latched until Halt is deasserted.
14	0h RW	**LPM Prewake Interrupt NAK Disable (LPM_PREWAKE_INTR_NAK_DIS):** LPM Prewake Naked Interrupt Enable 0: Ignore the Naked INTR for LPM. 1: Do not ignore the Naked INTR for LPM.
13:12	0h RW	**LPM Prewake Interrupt Enable (LPM_PREWAKE_INTR_EN):** LPM Prewake Interrupt Enable 11: Disable interrupt prewake for LPM. 01: Enable interrupt OUT prewake for LPM. 10: Enable interrupt IN prewake for LPM. 00: Enable both interrupt IN/OUT prewake for LPM.
11:10	0h RW	**Idle Scale (IDLE_SCALE):** Engine Idle Hysteresis Scale Controls the Engine Idle Hysteresis scale. 0 - clock 1 - 1 us 2 - 125 us
9	1h RW	**HS Interrupt-OUT Alarm (HS_INT_OUT_ALRM):** HS Interrupt OUT Alarm
8	0h RW	**HS Interrupt-IN Alarm (HS_INT_IN_ALRM):** HS Interrupt IN Alarm (HSII): Note: This is required to be set to enable the functionality behind the PCICFG.HSCFG2.HSIIPAPC method of tracking HS Intr IN EP's for Periodic Active.
7	0h RW	**SS Interrupt-OUT FC Alarm (SS_INT_OUT_FC_ALRM):** SS Interrupt OUT Alarm
6	0h RW	**SS Interrupt-IN Alarm (SS_INT_IN_FC_ALRM):** SS Interrupt IN Alarm

Bit Range	Default & Access	Field Name (ID): Description
5	1h RW	**SS Interrupt-OUT & not in FC Alarm (SS_INT_OUT_ALRM):** SS Interrupt OUT and not in FC Frame Alarm
4	1h RW	**SS Interrupt-IN & not in FC Alarm (SS_INT_IN_ALRM):** SS Interrupt IN and not in FC Frame Alarm
3	1h RW	**HS ISO-OUT Alarm (HS_ISO_OUT_ALRM):** HS ISO-OUT Alarm
2	1h RW	**HS ISO-IN Alarm (HS_ISO_IN_ALRM):** HS ISO-IN Alarm
1	1h RW	**SS ISO-OUT Alarm (SS_ISO_OUT_ALRM):** SS ISO-OUT Alarm
0	1h RW	**SS ISO-IN Alarm (SS_ISO_IN_ALRM):** SS ISO-IN Alarm

17.2.173 AUX Power Management Control (AUX_CTRL_REG2) - Offset 8154h

AUX Power Management Control Register2.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8154h	81192206h

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**DIS_L1P2_EXIT_ON_WAKE_EN:** This bit disables the dependency on Wake Enables defined in PORTSC for L1P2 exit when in D0
30	0h RW	**CFG_FAST_TRAINING:** 0: Normal operation mode 1: Link fast training mode This bit should be written 0 in normal operation
29	0h RW	**SNPS_PHYSTATUS_DONE_L1_DIS:** snps_phystatus_done_l1_dis
28	0h RW	**SHADOW_DECODE_DIS:** shadow_decode_dis_reg
27	0h RW	**BATT_CHARGE_D3_EN:** batt_charge_d3_en
26	0h RW	**CFG_DEBOUNCE_EN:** cfg_debounce_en
25	0h RW	**PCIE_P0_EXIT_L1_EN:** pcie_p0_exit_l1_en_reg

Bit Range	Default & Access	Field Name (ID): Description
24	1h RW	**Enable L1 exit notification to SNPS PCIe core (EN_L1_EXIT_NOTIF_PCIE):** This bit enables a L1 exit notification to SNPS PCIe core. There is a case where USB ports have waked up and AUX PM module has started the wakeup process. The AUX PM control state got into a wait for P0 state because it needs to wait until PCIe core to signal powerdown state change. Due to the fact that the core is in D3Hot, there is no run_stop bit set such that no internal interrupt will be fired. This causes the LTSSM of PCIe stayed in L1 even though AUX PM has known that it needs an L1 exit. This bit works together with bit21 of this register. 1: enables this feature 0: disables this feature.
23	0h RW	**DISABLE PLC ON DISCONNECT (DIS_PLC_ON_DISCONNECT):** 1: do not assert PLC for disconnection 0: assert PLC for disconnection
22	0h RW	**TREAT_IDLE_AS_TS2_IN_LTSSM_WAIT_4_TS2:** This bit enables a feature in PCIe core LTSSM to treat IDLE received as TS2 when LTSSM is in wait for TS2 receive state. This is a function requested from PHY where it is possible to not able to receive TS2 without error. 1: treat Logic IDLE as TS2 received when in some PCIe LTSSM state. 0: disable this feature.
21	0h RW	**Disable p2 overwrite due to the D3HOT where PCIe core enters the L1 (DIS_P2_OVERWRITE_DUE2_D3HOT):** Added a feature where if PCIe core LTSSM enters L1 due to the D3hot, the aux PM control will not start a P2 overwrite function in anticipating for the next L23 enter. 1: disables p2 overwrite due to the D3HOT where PCIe core enters the L1. 0: enables P2 overwrite even if it is in D3Hot.
20	1h RW	**Enable the port to enter U3 automatically when in U1/U2 (ENABLE_AUTO_U3_ENTRY_FROM_U2_U3):** 1: enables the port to enter U3 automatically when in U1/U2 0: disables the port to enter U3 automatically when in U1/U2
19	1h RW	**No linkdown reset is issue during low power state (DIS_LINKDOWN_RST_DURING_LOW_POWER):** No linkdown reset is issue during low power state
18	0h RW	**EN_EXIT_DEEP_SLEEP_IF_PCIE_IN_P0:** This bit enables a feature in AUX PM module where if PCIe core LTSSM is in P0 for a duration of time, it will exit the deep sleep state. This is for failure control in case. 1: enables this feature 0: disable this feature
17	0h RW	**U2_EXIT_LFPS_TIMER_VALUE:** This bit selects U2 exit LFPS timer value 0: 320ns 400ns in 25MHz domain 1: 240ns 320ns in 25MHz domain
16	1h RW	**EN_EXIT_DEEP_SLEEP_ON_USB_PORT_WAKEUP:** This bit enables a function that AUX PM module exits from the deep sleep state due to the USB ports wakeup level signal. There have added this feature where USB ports will generates a wakeup level signal to wakeup the AUX PM module if it is in deep sleep state and this level signal will be cleared if the change bits are updated by software. 1: enables this function 0: disables this function which means that a wakeup pulse generated from each USB PortSC event will wake up the AUX PM module from deep sleep if the D3 state is programmed.

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RW	**P3_ENTRY_TIMEOUT:** This field defines the timeout value to enter P3 mode in U2. 00: 7us 8us 01: 511us 512us 10: disables the timer (0us) 11: disables the timer (0us)
13	1h RW	**Enable U2 P3 Mode (EN_U2_P3):** 0: Disable U2 P3 mode 1: Enable U2 P3 mode
12:11	0h RW	**Fine Debug Mode Select (FINE_DM_SEL):** Fine Debug Mode Select
10	0h RW	**Enable Low Power State Based Core Clock Gating (EN_LP_CORE_CG):** When set to '1' enable core clock gating based on low power state entered
9	1h RW	**Disable USB3 Port Status Changed Event (DIS_U3_PORT_SCE):** 0: Enable USB3 port status change event generation if any change bit is not cleared 1: Disable USB3 port status change event generation if any change bit is not cleared Bit 12 default 0
8:4	00h RW	**Debug Mode Select Register (DEB_MODE_SEL):** Debug Mode Select Register
3	0h RW	**Enable Auto Wakeup Non-IDLE (EN_AWAK_NIDLE):** When set to 1 enables the auto wakeup function when engine has identified non IDLE condition.
2	1h RW	**Enable PM Control P1 Exit P2 (EN_PMC_P1_EXIT_P2):** When set 1 enables the PM control module to transition to P1 instead of P0 when exit P2.
1	1h RW	**Enable PCIe PIPE CLK Isolation (EN_PP_CLK_ISOL):** When set to 1 enables the PCIe PIPE CLK to be isolated when main power is removed.
0	0h RW	**Enable P2 Overwrite P1 Allowed Detect (EN_P2OVRP1_ADET):** When set to 1 enables a function that can detect whether or not enable P2 overwrite P1 function. The condition to get to P2 overwrite is when engine is in idle conditions. This means that there is no ISO EP pending.

17.2.174 USB2 PHY Power Management Control (USB2_PHY_PMC) - Offset 8164h

USB2 PHY Power Management Control.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8164h	000000FCh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Reserved
30:8	0h RO	**Reserved**
7	1h RW	**EN_CMDM_TXRXB:** Enable Command Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy
6	1h RW	**EN_TTE_TXRXB:** Enable TTE Active indication for Tx/Rx Bias circuit HS Phy PM Policy
5	1h RW	**EN_IDMA_TXRXB:** Enable IDMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy
4	1h RW	**EN_ODMA_TXRXB:** Enable ODMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy
3	1h RW	**EN_TRM_TXRXB:** Enable Transfer Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy
2	1h RW	**EN_SCH_TXRXB:** Enable Scheduler Active indication for Tx/Rx Bias circuit HS Phy PM Policy
1	0h RW	**Enable Rx Bias ckt disable (EN_RXB_CD):** When set enables the Rx bias ckt to be disabled when conditions met (as in the HS phy PM policy bits)
0	0h RW	**Enable Tx Bias ckt disable (EN_TXB_CD):** When set enables the Tx bias ckt to be disabled when conditions met (as in the HS phy PM policy bits)

17.2.175 XHCI Aux Clock Control Register (XHCI_AUX_CCR) - Offset 816Ch

XHCI Aux Clock Control Register.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 816Ch	000F403Ch

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	1h RW	**USB3 Partition Engine/Link trunk gating Enable (PARUSB3_ENG_GEN):** When set to 1 enables gating of the SOSC trunk to the XHCI engine and link in the PARUSB3 partition.
18	1h RW	**USB3 Partition Frame Timer trunk gating Enable (PARUSB3_LINK_GEN):** When set to 1 enables gating of the SOSC trunk to the Frame timer in the PARUSB3 partition.
17	1h RW	**USB2 link partition clock gating enable (PARUSB2_CLK_GEN):** When set to 1 enables gating of the SOSC trunk to the USB2 link and Phy logic in the PARUSB2 partition.

Bit Range	Default & Access	Field Name (ID): Description
16	1h RW	**USB2/USHIP 12.5 MHz partition clock gating enable (USHIP_PCGEN):** When set to 1 enables gating of the 12.5 MHz SOSC trunk to the USB2 and USHIP logic in the PARUSB2 partition.
15	0h RO	**Reserved**
14	1h RW	**USB3 Port Aux/Core clock gating enable (USB3_AC_CGE):** When set, allows the aux_cclk clock into the USB3 port to be gated when conditions are met. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
13:12	0h RW	**Rx Detect Timer when port Aux Clock is Gated (RX_DT_ACG):** This field defines the value of the timer used to perform Rx Detect when port Aux Clock has been gated. 0x0: 100ms 0x1: 12ms Others: Reserved Note: This timer shall use the Fast Training Timer Tick (about 1us tick) for simulation purposes. For Fast Training mode, the above timeouts will become about 11us and about 100us, +/- implementation uncertainty, respectively.
11:10	0h RO	**Reserved**
9	0h RW	**Aux Clock Gating Counter PipeStage Enable (AUXCLKGT_CNTEN_PIPE_STGEN):** Policy to enable pipe stage on cnten of aux_clk and frame_clk gating logic
8	0h RO	**Reserved**
7	0h RW	**Frame Timer Clock Gating Ports in U2 Enable (FTCGPU2E):** This bit, when set, allows Host Controller to gate the clock to the Frame Timer when ports are in U2.
6	0h RW	**USB2 port clock throttle enable (USB2_PC_TE):** When set, allows the Aux clock into the USB2 ports to be throttled when conditions allow.
5	1h RW	**XHCI Engine Aux clock gating enable (XHCI_AC_GE):** When set, allows the aux clock into the XHCI engine to be gated when idle. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
4	1h RW	**XHCI Aux PM block clock gating enable (XHCI_APMB_CGE):** When set, allows the aux clock into the Aux PM block to be gated when idle. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.

Bit Range	Default & Access	Field Name (ID): Description
3	1h RW	**USB3 Aux Clock Trunk Gating Enable (USB3_AC_TGE):** When set, allows Aux Clock Trunk feeding to USB3.0 ports to be gated when port Aux clock is gated at all USB3.0 ports and all USB3.0 modPHY instances. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
2	1h RW	**USB3 Port Aux/Port clock gating enable (USB3_AP_CGE):** When set, allows the aux_pclk clock into the USB3 port to be gated when conditions are met. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
1	0h RW	**ModPHY port Aux clock gating enable in U2 (MPP_AC_GEU2):** When set, allows the aux clock into the ModPhy to be gated when Link is in U2 and pipe has been in PS3 for at least the time defined by U2 Residency Before ModPHY Clock Gating field. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
0	0h RW	**ModPHY port Aux clock gating enable in Disconnected, U3 or Disabled (MPP_AC_GE_DDU3):** When set, allows the aux clock into the ModPHY to be gated when Link is in Disconnected, U3 or Disabled state. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.

17.2.176 XHC Latency Tolerance Parameters LTV Control (XLTP_LTV1) - Offset 8174h

XHC Latency Tolerance Parameters LTV Control.

Type	Size	Offset	Default
MMIOMMIO	32 bit	MBAR + 8174h	01400C01h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Disable scheduler direct transition from IDLE to NO requirement (DIS_SDT_IDL_NR):** 0: (default) allow scheduler direct transition from IDLE to NO requirement 1: Disable scheduler direct transition from IDLE to NO requirement
30	0h RW	**XHCI LTR Transition Policy (XLTRTP) (LTR_TRANS_POL):** When 0, the LTR messaging state machine transitions through High Med Low Active states assuming enough latency is available for each transition. When 1, LTR messaging state machine transitions from High, Medium, or Low LTR states to Active state upon the Alarm Timer timeout and stays in Active until the next service boundary.
29	0h RW	Reserved
28	0h RW	**XHCI LTR Active Enable (XLTRAE) (XLTRAE):** 0: The Power Scheduler will not request an LTR message on a transition to ACTIVE. 1: The Power Scheduler will request an LTR message on a transition to ACTIVE.
27	0h RW	**Power Scheduler Local Clock Gating Enable (PWRLCGE) (PWRLCGE):** 0: Power Scheduler does not use local clock gating 1: Power Scheduler's local clock gating enabled. Note: This functionality is no longer required. This LCG existed previous to the inclusion of Aux clock gating.
26	0h RW	**LTR EVM Hysteresis Max Count (LTR_HYS_MAX):** Power Scheduler's Periodic IDLE residency before it asserts Periodic Complete 0: Hysteresis set to 127 clock ticks. (.64us) 1: Hysteresis set to 31 clock ticks (.16us)
25	0h RW	**USB2 async active policy (EN_USB2_LTV_U0_PORT_ASYNC_ACTIVE):** Active USB2 slots in U0 will get LTV from slot lookup table
24	1h RW	**XHCI LTR Enable (XLTRE):** This bit must be set to enable LTV messaging from XHCI to the PMC.
23:12	400h RW	**Periodic Active LTV (PA_LTV):** 23:22 Latency Scale 00b: Reserved 01b: Latency Value to be multiplied by 1024 10b: Latency Value to be multiplied by 32,768 11b: Latency Value to be multiplied by 1,048,576 21:12 Latency Value (ns) Defaults to 0 micro seconds
11:0	C01h RW	**USB2 Port L0 LTV (USB2_PL0_LTV):** 11:10 Latency Scale 00b: Reserved 01b: Latency Value to be multiplied by 1024 10b: Latency Value to be multiplied by 32,768 11b: Latency Value to be multiplied by 1,048,576 9:0 Latency Value (ns) Defaults to 128 Micro Seconds

17.2.177 XHC Latency Tolerance Parameters LTV Control 2 (XLTP_LTV2) - Offset 8178h

XHC Latency Tolerance Parameters LTV Control 2.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8178h	000017FFh

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW	**Non Offload Active Periodic TTE Counter Clearing Disable (NONOFLD_ACTV_PRDC_TTE_CNT_CLR_DIS):** Setting this bit will disable clearing Non-offload active periodic TTE counter based on TTE Idle indicator
15	0h RW	**Enable USB2 Port L0 LTV based on active async (EN_USB2_L0_LTV_ASYN):** 0 - USB2 Port L0 LTV is used regardless of whether there is active async EPs being present or not (Legacy mode) 1 - USB2 LTR L0 LTV is used only when there is active async EPs being present on that port. In the absence of active async EPs on given port, the L0 LTR value is NoRequirement for that port.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Audio Offload USB2 Resume to DMA Active Mapping Enable (ADO_USB2RES_DMAACTV_MAP_EN):** Enables USB2 Port Resume Influence on 'XHCI DMA Active' indication (i.e. Run 125) for Ports Handling Audio Offload. 0 - A USB2 port involved with Audio Offload will NOT influence the XHCI DMA Active indication through USB2 Resume (i.e. USB2 resume for the associated port is not consumed when generating XHCI DMA Active). 1 - A USB2 port involved with Audio Offload will influence (legacy mode) the XHCI DMA Active indication through USB2 Resume (i.e. USB2 resume for the associated port is not consumed when generating XHCI DMA Active). Note: When this field is '0' will allow for a different field to determine what constitutes Audio Offload involvement. The different field is located at 0x8174[13]
13	0h RW	**Audio Offload USB2 Resume to DMA Active Mask Policy (ADO_USB2RES_DMAACTV_MASK_POLICY):** Defines the conditions required for what constitutes Audio Offload involvement for appropriate masking of USB2 Resume on 'XHCI DMA Active' indication (i.e. Run 125) for Ports Handling Audio Offload. 0 - Mask USB2 Resume from asserting the XHCI DMA Active if the particular port going through resume is engaged in Audio Offload while an Audio Offload DB is active (i.e. Audio Offload is connected and active). 1 - Mask USB2 Resume from asserting the XHCI DMA Active if the particular port going through resume is engaged in Audio Offload (i.e. Audio Offload is connected) irrespective of a DB being active/idle.
12:0	17FFh RW	**LTV Limit (LTV_LMT):** This register defines a maximum LTR value that is allowed to be advertised to the PMC. This is meant to be used as a workaround or mitigation if issues are discovered with the LTR values generated by the XHC using the defined algorithms. If the LTR value of the XHC is larger than the value in this register field, the value in this field is sent to the PMC instead. Default value is the highest possible - 101b 12:10: Latency Multiplier Field 000b - Value times 1 ns 001b - Value times 32 ns 010b - Value times 1,024 ns 011b - Value times 32,768 ns 100b - Value times 1,048,576 ns 101b - Value times 33,554,432 ns 110b-111b - Not Permitted 9:0: Latency Value Default = 3FFh

17.2.178 XHC Latency Tolerance Parameters High Idle Time Control (XLTP_HITC) - Offset 817Ch

XHC Latency Tolerance Parameters High Idle Time Control.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 817Ch	00050002h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:16	0005h RW	**Minimum High Idle Time (MHIT):** This is the minimum schedule idle time that must be available before a "High" LTR value can be indicated. This value must be larger than HIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)
15:13	0h RO	**Reserved**
12:0	0002h RW	**High Idle Wake Latency (HIWL):** This is the latency to access memory from the High Idle Latency state. This value must be larger than MIWL and LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)

17.2.179 XHC Latency Tolerance Parameters Medium Idle Time Control (XLTP_MITC) - Offset 8180h

XHC Latency Tolerance Parameters Medium Idle Time Control.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8180h	00050002h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:16	0005h RW	**Minimum Medium Idle Time (MMIT):** This is the minimum schedule idle time that must be available before a "Medium" LTR value can be indicated. This value must be larger than MIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)
15:13	0h RO	**Reserved**
12:0	0002h RW	**Medium Idle Wake Latency (MIWL):** This is the latency to access memory from the Medium Idle Latency state. This value must be larger than LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)

17.2.180 XHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC) - Offset 8184h

XHC Latency Tolerance Parameters Low Idle Time Control.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8184h	00050002h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:16	0005h RW	**Minimum Low Idle Time (MLIT):** This is the minimum schedule idle time that must be available before a "Low" LTR value can be indicated. This value must be larger than LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)
15:13	0h RO	**Reserved**
12:0	0002h RW	**Low Idle Wake Latency (LIWL):** This is the latency to access memory from the Medium Idle Latency state. 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)

17.2.181 LFPS On Count (LFPSONCOUNT_REG) - Offset 81B8h

LFPS On Count.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 81B8h	000420C8h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW	**RTCCLKGENOVERRIDE:** when set it will Disable the RTC tick generation unconditionally. This will be used by software to disable the tick and CRO if WDE/WCE is disabled during D3
20	0h RW	Reserved
19	0h RW	**RXLFPSFILT_8US_EN:** 0- RXLFPS detection filter for U3 Exit is 4 ticks of 128ns 1- RXLFPS Filter will remain at 8us
18	1h RW	**XDISRTCPOLLING:** 1: Disable the RTC tick generation which is consumed for the RxDet Polling, LFPS Polling and Aux Clock PCG Wakeup to enable this. 0: RTC tick generation based on the defined interval

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**U2P3 LFPS Periodic Sampling Control (XU2P3LPSC):** This field controls the OFF time for the LFPS periodic sampling for SS ports in U2P3. If LFPSPM for a port is 1, it will override the OFF time and LFPS receiver will remain OFF permanently. For Fast Sim mode, 500us will be equivalent to 5us. 0x0 Polling Disable. (RXDET Polling will become 100ms.) 0x1 500us OFF Time 0x2 1ms OFF Time 0x3 1.5ms OFF Time
15:10	08h RW	**XLFPSONCNTSSIC:** This time would describe the number of clocks LFPS will remain ON. LFPS detection operation may be carried out on using RTC clock or Oscillator clock. The value of this register should be adjusted accordingly. For RTC recommended value is 2. For Oscillator clock, recommended value is 8.
9:0	0C8h RW	**XLFPSONCNTSS:** This time would describe the number of clocks LFPS will remain ON. LFPS detection operation may be carried out on using RTC clock or Oscillator clock. The value of this register should be adjusted accordingly. For RTC recommended value is 2. For Oscillator clock, recommended value is 200.

17.2.182 USB2 Power Management Control (USB2PMCTRL_REG) - Offset 81C4h

USB2 Power Management Control.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 81C4h	00020908h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RF PG Fix Disable (DIS_RFPGFIX):** 0 - Enable RF Power gating fix (Default) 1 - Disable RF Power gating fix
30:19	0h RO	**Reserved**
18:16	2h RW	**L1 USB2 PLL Spin Up Time (L1USB2PLLSUT):** 111: 70us 110: 60us ... 001: 10us 000: 0us
15	0h RO	**Reserved**
14	0h RW	**RTC Resume Disable (DIS_RTCRSM):** 1: When set, RTC resume will be disabled and fallback to use portmgr for resumes 0: When cleared, RTC resume will take over portmgr's U3 resume

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Bypass Suspend SM (BYPSUSSM):** 1: When set, Suspend SM is bypassed and L1/L2 suspendm from the controller goes directly to the PHY 0: When cleared, Suspend SM controls the L1/L2 suspendm to the PHY
12	0h RW	**USB2 HOST PHY UTMI Clock Gate Disable Policy (U2HPUCGDP):** This controls the policy for Host PHY UTMI Clock Gating. When Set HOST PHY UTMI Clock Gating is disabled else Host PHY UTMI Clock Gating is enabled
11	1h RW	**USB2 PHY SUS Power Gate PORTSC Block Policy (U2PSPGPSCBP):** This controls the policy for blocking PORTSC Updates while the USB2 PHY SUS Well is power gated. When set, the controller will block any updates to the PORTSC caused by port status change if the USB2 PHY SUS is power gated. 0 Do not
10:8	1h RW	**USB2 PHY SUS Well Power Gate Entry Hysteresis Count (U2PSPGEHC):** This controls the amount of hysteresis time the controller will enforce after detecting the USB2 PHY SUS Power Gate entry condition. 0h 0 clocks 1h 32 clocks 2h 64 clocks 3h 128 clocks 4h 256 clocks 5h 512 clocks 6h 1024 clocks 7h 2048 clocks
7:4	0h RW	**USB2 PHY SUS Power Gate PORTSC Block Policy (U2CLPGLAT):** This field represents the worst case latency for the USB2 Common Lane to enter and exit its power gate state. This fields is required to be compared to a ports HIRD/HIRD value for the ports that have allowed L1 to L2 mapping to determine if the Common Lane can be allowed to power off. If the power gate entry/exit latency is greater than the HIRD/HIRDD then the common lane should not be allowed to power gate as this will result in a L1 exit violation. 0h 100 us 1h 200 us 2h 300 us Eh 1500us Fh 1600 us
3:2	2h RW	**USB2 PHY SUS Well Power Gate Policy (U2PSUSPGP):** This field controls when to enable the USB2 PHY SUS Well Power Gating when the proper conditions are met. 00 USB2 PHY SUS Power Gating is Disabled. 01 USB2 PHY SUS Power Gating is Enabled in Only D0 and D0i2 (Excludes D0i3 and D3) 10 USB2 PHY SUS Power Gating is Enabled in only in D0, D0i2 and D0i3 (Excludes D3) 11 USB2 PHY SUS Power Gating is Enabled in D0/D0i2/D0i3/D3
1:0	0h RO	**Reserved**

17.2.183 USB Legacy Support Capability (USBLEGSUP) - Offset 846Ch

This register is modified and maintained by BIOS.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 846Ch	00002201h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**HC OS Owned Semaphore (HCOSOS):** HC OS Owned Semaphore
23:17	0h RO	**Reserved**
16	0h RW	**HC BIOS Owned Semaphore (HCBIOSOS):** HC BIOS Owned Semaphore
15:8	22h RW/L	**Next Capability Pointer (NEXTCP):** Next Capability Pointer **Locked by:** XHCC1.ACCTRL
7:0	01h RW/L	**Capability ID (CID):** Capability ID **Locked by:** XHCC1.ACCTRL

17.2.184 USB Legacy Support Control Status (USBLEGCTLSTS) - Offset 8470h

USB Legacy Support Control Status.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8470h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**SMI on BAR (SMIBAR):** SMI on BAR
30	0h RW/1C	**SMI on PCI Command (SMIPCIC):** SMI on PCI Command
29	0h RW/1C	**SMI on OS Ownership Change (SMIOSOC):** SMI on OS Ownership Change
28:21	0h RO	**Reserved**
20	0h RO	**SMI on Host System Error (SMIHSE):** SMI on Host System Error
19:17	0h RO	**Reserved**
16	0h RO	**SMI on Event Interrupt (SMIEI):** SMI on Event Interrupt
15	0h RW	**SMI on BAR Enable (SMIBARE):** SMI on BAR Enable

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**SMI on PCI Command Enable (SMIPCICE):** SMI on PCI Command Enable
13	0h RW	**SMI on OS Ownership Enable (SMIOSOE):** SMI on OS Ownership Enable
12:5	0h RO	**Reserved**
4	0h RW	**SMI on Host System Error Enable (SMIHSEE):** SMI on Host System Error Enable
3:1	0h RO	**Reserved**
0	0h RW	**USB SMI Enable (USBSMIE):** USB SMI Enable

17.2.185 Port Disable Override Capability Register (PDO_CAPABILITY) - Offset 84F4h

Port Disable Override Capability Register.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 84F4h	000003C6h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	03h RW/L	**Next Capability Pointer (NCP):** Next Capability Pointer **Locked by:** XHCC1.ACCTRL
7:0	C6h RW/L	**Capability ID (CID):** Capability ID **Locked by:** XHCC1.ACCTRL

17.2.186 Debug Capability ID Register (DCID) - Offset 8700h

This register is modified and maintained by BIOS.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8700h	0005100Ah

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:16	05h RW/L	**Debug Capability Event Ring Segment Table Max (DCERSTM):** Note: This register is sticky. **Locked by:** XHCC1.ACCTRL
15:8	10h RW/L	**Next Capability Pointer (NCP):** Note: This register is sticky. **Locked by:** XHCC1.ACCTRL
7:0	0Ah RW/L	**Capability ID (CID):** Note: This register is sticky. **Locked by:** XHCC1.ACCTRL

17.2.187 Debug Capability Doorbell Register (DCDB) - Offset 8704h

Debug Capability Doorbell Register.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8704h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**Doorbell Target (DBTGT):** This field defines the target of the doorbell reference. Below defines the Debug Capability notification that is generated by ringing the doorbell. Value Definition 0 Data EP 1 OUT Enqueue Pointer Update 1 Data EP 1 IN Enqueue Pointer Update 2:255 Reserved This field returns '0' when read and the value should be treated as undefined by software.
7:0	0h RO	**Reserved**

17.2.188 Debug Capability Event Ring Segment Table Size Register (DCERSTSZ) - Offset 8708h

Debug Capability Event Ring Segment Table Size Register.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8708h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Event Ring Segment Table Size (ERSTS):** This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Debug Capability Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the DCERST Max field in the DCID register Software shall initialize this register before setting the Debug Capability Enable field in the DCCTRL register to '1'.

17.2.189 Debug Capability Event Ring Segment Table Base Address Register (DCERSTBA) - Offset 8710h

Debug Capability Event Ring Segment Table Base Address Register.

Type	Size	Offset	Default
MMIO	64 bit	MBAR + 8710h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:4	0000000000000000h RW	**Event Ring Segment Table Base Address Register (ERSTBAR):** This field defines the high order bits of the start address of the Debug Capability Event Ring Segment Table. Software shall initialize this register before setting the Debug Capability Enable field in the DCCTRL register to '1'.
3:0	0h RO	**Reserved**

17.2.190 Debug Capability Event Ring Dequeue Pointer Register (DCERDP) - Offset 8718h

Debug Capability Event Ring Dequeue Pointer Register.

Type	Size	Offset	Default
MMIO	64 bit	MBAR + 8718h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:4	00000000 0000000h RW	**Dequeue Pointer (DQP):** This field defines the high order bits of the 64-bit address of the current Debug Capability Event Ring Dequeue Pointer. Software shall initialize this register before setting the Debug Capability Enable field in the DCCTRL register to '1'.
3	0h RO	**Reserved**
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in.

17.2.191 Debug Capability Control Register (DCCTRL) - Offset 8720h

Debug Capability Event Ring Dequeue Pointer Register.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8720h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Debug Capability Enable (DCE):** Debug Capability Enable
30:24	00h RO	**Device Address (DADDR):** Device Address
23:16	00h RO	**Debug Max Burst Size (DMBS):**
15:5	0h RO	**Reserved**
4	0h RW/1C	**DbC Run Change (DRC):** DbC Run Change
3	0h RW/1S	**Halt IN TR (HIT):** Halt IN TR
2	0h RW/1S	**Halt OUT TR (HOT):** Halt OUT TR
1	0h RW	**Link Status Event Enable (LSE):** Link Status Event Enable
0	0h RO	**DbC Run (DCR):** DbC Run

17.2.192 Debug Capability Status Register (DCST) - Offset 8724h

Debug Capability Status Register.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8724h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Debug Port Number (DPNUM):** This field provides the ID of the Root Hub port that the Debug Capability has been automatically attached to. The value is '0' when the Debug Capability is not attached to a Root Hub port.
23:1	0h RO	**Reserved**
0	0h RO	**Event Ring Not Empty (ERNE):** When '1', this field indicates that the Debug Capability Event Ring has a Transfer Event on it. It is automatically cleared to '0' by the xHC when the Debug Capability Event Ring is empty, i.e. the Debug Capability Enqueue Pointer is equal to the Debug Capability Event Ring Dequeue Pointer register.

17.2.193 Debug Capability Port Status And Control Register (DCPORTSC) - Offset 8728h

Debug Capability Port Status And Control Register.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8728h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW/1C	**USB3-Port Config Error Change. USB2-Reserved for USB2 Debug Capability (CEC):** USB3-This flag indicates that the port failed to configure its link partner. 0 = No change. 1 = Port Config Error detected. Software shall clear this bit by writing a '1' to it. USB2-This bit shall never be set when operating in USB2 Kernel Debug mode.
22	0h RW/1C	**Port Link Status Change (PLC):** This flag is set to '1' due to the following PLS transitions: U0 -) U3 Suspend signaling detected from Debug Host U3 -) U0 Resume complete Polling -) Disabled Training Error Ux or Recovery -) Inactive Error Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'
21	0h RW/1C	**Port Reset Change (PRC):** This bit is set when reset processing on this port is complete (i.e. a '1' to '0' transition of PR). '0' = No change. '1' = Reset complete. Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'.
20:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW/1C	**Connect Status Change (CSC):** '1' = Change in Current Connect Status. '0' = No change. Indicates a change has occurred in the port's Current Connect Status. The xHC sets this bit to '1' for all changes to the Debug Device connect status, even if system software has not cleared an existing DbC Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, hardware will be "setting" an already-set bit (i.e., the bit will remain '1'). Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'.
16:14	0h RO	**Reserved**
13:10	0h RO	**Port Speed (PSPD):** This field identifies the speed of the port. This field is only relevant when a Debug Host is attached (CCS = '1') in all other cases this field shall indicate Undefined Speed. 0 Undefined Speed 1-15 Protocol Speed ID (PSI) Note: The Debug Capability only does not supports LS, FS, or HS operation.
9	0h RO	**Reserved**
8:5	4h RO	**Port Link State (PLS):** This field reflects its current link state. This field is only relevant when a Debug Host is attached (Debug Port Number) '0'). Value Meaning 0 Link is in the U0 State 1 Link is in the U1 State 2 Link is in the U2 State 3 Link is in the U3 State (Device Suspended) 4 Link is in the Disabled State 5 Link is in the RxDetect State 6 Link is in the Inactive State 7 Link is in the Polling State 8 Link is in the Recovery State 9 Link is in the Hot Reset State 15:10 Reserved Note: Transitions between different states are not reflected until the transition is complete.
4	0h RO	**Port Reset (PR):** '1' = Port is in Reset. '0' = Port is not in Reset. This bit is set to '1' when the bus reset sequence as defined in the USB Specification is detected on the Root Hub port assigned to the Debug capability. It is cleared when the bus reset sequence is completed by the Debug Host, and the DbC shall transition to the USB Default state. A '0' to '1' transition of this bit shall clear DCPORTSC PED ('0'). This field is '0' if DCE or CCS are '0'.

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Port Enabled/Disabled (PED):** Default = '0'. '1' = Enabled. '0' = Disabled. This flag shall be set to '1' by a '0' to '1' transition of CCS or a '1' to '0' transition of the PR. When PED transitions from '1' to '0' due to the assertion of PR, the port's link shall transition to the Rx.Detect state. This flag may be used by software to enable or disable the operation of the Root Hub port assigned to the Debug Capability. The Debug Capability Root Hub port operation may be disabled by a fault condition (disconnect event or other fault condition, e.g. a LTSSM Polling substate timeout, tPortConfiguration timeout error, etc.), the assertion of DCPORTSC PR, or by software. 0 = Debug Capability Root Hub port is disabled. 1 = Debug Capability Root Hub port is enabled. When the port is disabled (PED = '0') the port's link shall enter the SS.Disabled state and remain there until PED is reasserted ('1') or DCE is negated ('0'). Note that the Root Hub port is remains mapped to Debug Capability while PED = '0'. While PED = '0' the Debug Capability will appear to be disconnected to the Debug Host. Note, this bit is not affected by PORTSC PR bit transitions. This field is '0' if DCE or CCS are '0'.
0	0h RO	**Current Connect Status (CCS):** '1' = A Root Hub port is connected to a Debug Host and assigned to the Debug Capability. '0' = No Debug Host is present. This value reflects the current state of the port, and may not correspond to the value reported by the Connect Status Change (CSC) field in the Port Status Change Event. Port Status Change Event is generated when both PED and CSC are set to 1. This is a change compared to USB3 because for USB2, the Port Speed field is only valid after PED is set to 1, which only happens some time after CSC is set to 1. This flag is '0' if Debug Capability Enable (DCE) is '0'.

17.2.194 Debug Capability Context Pointer Register (DCCP) - Offset 8730h

Debug Capability Context Pointer Register.

Type	Size	Offset	Default
MMIO	64 bit	MBAR + 8730h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:4	0000000000000000h RW	**Debug Capability Context Pointer Register (DCCPR):** This field defines the high order bits of the start address of the Debug Capability Context data structure associated with the Debug Capability. Software shall initialize this register before setting the Debug Capability Enable bit in the Debug Capability Control Register to '1'.
3:0	0h RO	**Reserved**

17.2.195 GLOBAL TIME SYNC CAP REG (GLOBAL_TIME_SYNC_CAP_REG) - Offset 8E10h

GLOBAL TIME SYNC CAP REG.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8E10h	000012C9h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	12h RW/L	**Next Capability pointer (NCP):** Next Capability pointer **Locked by:** XHCC1.ACCTRL
7:0	C9h RW/L	**Capability ID (CID):** Capability ID **Locked by:** XHCC1.ACCTRL

17.2.196 GLOBAL TIME SYNC CTRL REG (GLOBAL_TIME_SYNC_CTRL_REG) - Offset 8E14h

GLOBAL TIME SYNC CTRL REG.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8E14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/1S	**Time Stamp Counter Capture Initiate (TIME_STAMP_CNTR_CAPTURE_INITIATE):** SW sets this bit to initiate a time capture. Once the time capture is complete and the time values are valid in the Local and Global time capture registers, HW clears the bit.

17.2.197 MICROFRAME TIME REG (MICROFRAME_TIME_REG) - Offset 8E18h

MICROFRAME TIME REG.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8E18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO	**Captured Frame List Current Index/Frame Number (CMFI):** The value in this register is updated in response to sample_now signal. Bits [29:16] reflect state of bits [13:0] of FRINDEX
15:13	0h RO	**Reserved**
12:0	0000h RO	**Captured Micro-frame BLIF (CMFB):** The value is updated in response to sample_now signal and provides information about offset within micro-frame. Captured value represents number of 8 high-speed bit time units from start of micro-frame. At the beginning of micro-frame captured value will be 0 and increase to maximum value at the end. Default maximum value is 7499 but it may be changed as result of adjustment done via Bus Interval Adjust (BIA).

17.2.198 GLOBAL TIME LOW REG (GLOBAL_TIME_LOW_REG) - Offset 8E20h

Global Time Value (Low).

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8E20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**GLOBAL_TIME_LOW:** Global Time Value (Low)

17.2.199 GLOBAL TIME HI REG (GLOBAL_TIME_HI_REG) - Offset 8E24h

Global Time Value (High)

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8E24h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**GLOBAL_TIME_HI:** Global Time Value (High)

17.2.200 XHCI USB2 Overcurrent Pin Mapping (U2OCM1) - Offset 90A4h

The RW/L property of this register is controlled by OCCFDONE bit.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 90A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RW/L	**OC Mapping (OCM):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std Note: The USB-R port which is the most significant USB2 port does not have an OC pin. Thus the OC assignment for the USB-R port is ignored. **Locked by:** XHCC2.OCCFGDONE

17.2.201 XHCI USB2 Overcurrent Pin Mapping (U2OCM2) - Offset 90A8h

The RW/L property of this register is controlled by OCCFDONE bit.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 90A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RW/L	**OC Mapping (OCM):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std Note: The USB-R port which is the most significant USB2 port does not have an OC pin. Thus the OC assignment for the USB-R port is ignored. **Locked by:** XHCC2.OCCFGDONE

17.2.202 XHCI USB2 Overcurrent Pin Mapping (U2OCM3) - Offset 90ACh

The RW/L property of this register is controlled by OCCFDONE bit.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 90ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RW/L	**OC Mapping (OCM):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std Note: The USB-R port which is the most significant USB2 port does not have an OC pin. Thus the OC assignment for the USB-R port is ignored. **Locked by:** XHCC2.OCCFGDONE

17.2.203 XHCI USB2 Overcurrent Pin Mapping (U2OCM4) - Offset 90B0h

The RW/L property of this register is controlled by OCCFDONE bit.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 90B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RW/L	**OC Mapping (OCM):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std Note: The USB-R port which is the most significant USB2 port does not have an OC pin. Thus the OC assignment for the USB-R port is ignored. **Locked by:** XHCC2.OCCFGDONE

17.2.204 XHCI USB2 Overcurrent Pin Mapping (U2OCM5) - Offset 90B4h

The RW/L property of this register is controlled by OCCFDONE bit.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 90B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RW/L	**OC Mapping (OCM):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std Note: The USB-R port which is the most significant USB2 port does not have an OC pin. Thus the OC assignment for the USB-R port is ignored. **Locked by:** XHCC2.OCCFGDONE

17.2.205 XHCI USB2 Overcurrent Pin Mapping (U2OCM6) - Offset 90B8h

The RW/L property of this register is controlled by OCCFDONE bit.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 90B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RW/L	**OC Mapping (OCM):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std Note: The USB-R port which is the most significant USB2 port does not have an OC pin. Thus the OC assignment for the USB-R port is ignored. **Locked by:** XHCC2.OCCFGDONE

17.2.206 XHCI USB2 Overcurrent Pin Mapping (U2OCM7) - Offset 90BCh

The RW/L property of this register is controlled by OCCFDONE bit.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 90BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RW/L	**OC Mapping (OCM):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std Note: The USB-R port which is the most significant USB2 port does not have an OC pin. Thus the OC assignment for the USB-R port is ignored. **Locked by:** XHCC2.OCCFGDONE

17.2.207 XHCI USB2 Overcurrent Pin Mapping (U2OCM8) - Offset 90C0h

The RW/L property of this register is controlled by OCCFDONE bit.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 90C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RW/L	**OC Mapping (OCM):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std Note: The USB-R port which is the most significant USB2 port does not have an OC pin. Thus the OC assignment for the USB-R port is ignored. **Locked by:** XHCC2.OCCFGDONE

17.2.208 XHCI USB3 Overcurrent Pin Mapping (U3OCM1) - Offset 9124h

The RW/L property of this register is controlled by OCCFDONE bit.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 9124h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW/L	**OC Mapping (OCM):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std. port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std **Locked by:** XHCC2.OCCFGDONE

17.2.209 XHCI USB3 Overcurrent Pin Mapping (U3OCM2) - Offset 9128h

The RW/L property of this register is controlled by OCCFDONE bit.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 9128h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW/L	**OC Mapping (OCM):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std. port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std **Locked by:** XHCC2.OCCFGDONE

17.2.210 XHCI USB3 Overcurrent Pin Mapping (U3OCM3) - Offset 912Ch

The RW/L property of this register is controlled by OCCFDONE bit.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 912Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW/L	**OC Mapping (OCM):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std. port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std **Locked by:** XHCC2.OCCFGDONE

17.2.211 XHCI USB3 Overcurrent Pin Mapping (U3OCM4) - Offset 9130h

The RW/L property of this register is controlled by OCCFDONE bit.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 9130h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW/L	**OC Mapping (OCM):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std. port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std **Locked by:** XHCC2.OCCFGDONE

17.2.212 XHCI USB3 Overcurrent Pin Mapping (U3OCM5) - Offset 9134h

The RW/L property of this register is controlled by OCCFDONE bit.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 9134h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW/L	**OC Mapping (OCM):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std. port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std **Locked by:** XHCC2.OCCFGDONE

17.2.213 XHCI USB3 Overcurrent Pin Mapping (U3OCM6) - Offset 9138h

The RW/L property of this register is controlled by OCCFDONE bit.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 9138h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW/L	**OC Mapping (OCM):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std. port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std **Locked by:** XHCC2.OCCFGDONE

17.2.214 XHCI USB3 Overcurrent Pin Mapping (U3OCM7) - Offset 913Ch

The RW/L property of this register is controlled by OCCFDONE bit.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 913Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW/L	**OC Mapping (OCM):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std. port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std **Locked by:** XHCC2.OCCFGDONE

17.2.215 XHCI USB3 Overcurrent Pin Mapping (U3OCM8) - Offset 9140h

The RW/L property of this register is controlled by OCCFDONE bit.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 9140h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW/L	**OC Mapping (OCM):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std. port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std **Locked by:** XHCC2.OCCFGDONE

17.3 USB Configuration Registers Summary

The USB Configuration Registers are distributed within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface using the following Target Port (Destination Port) Identification:

Target Port (Destination Port) Identification = 0xCA

For complete details on how to use the PCH Sideband Interface to access these PCH Private Configuration Registers reference the latest Platform Controller Hub BIOS Specification.

Table 17-3. Summary of USB Configuration Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
402Bh	4	GLB ADP VBUS COMP REG (GLB_ADP_VBUS_COMP_REG)	006A4005h
4100h	4	c73usb2ad_USB2 PER PORT (USB2_PER_PORT_PP0)	00003D00h
4126h	4	c73usb2ad_USB2 PER PORT 2 (USB2_PER_PORT_2_PP0)	01800000h

17.3.1 GLB ADP VBUS COMP REG (GLB_ADP_VBUS_COMP_REG) - Offset 402Bh

GLB ADP VBUS COMP REG

Type	Size	Offset	Default
MMIO	32 bit	FDCA0000h + 402Bh	006A4005h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22	1h RW	**Reserved**
21	1h RW	**Reserved**
20:19	1h RW	**Reserved**
18:16	2h RW	**Reserved**
15:14	1h RW	**Reserved**
13	0h RO/V	**Reserved**
12	0h RO/V	**Reserved**
11	0h RO/V	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO/V	**Reserved**
9	0h RO/V	**Reserved**
8	0h RW	**IUSBIDPULLUPLVGEN:** Internal pull-up resistor for Ball A12. 0 - Disabled 1 - Enabled
7	0h RW	**Reserved**
6	0h RW	**Reserved**
5	0h RW	**Reserved**
4	0h RW	**Reserved**
3:2	1h RW	**Reserved**
1:0	1h RW	**Reserved**

17.3.2 c73usb2ad_USB2 PER PORT (USB2_PER_PORT_PP0) - Offset 4100h

c73usb2ad_USB2 PER PORT

Type	Size	Offset	Default
MMIO	32 bit	FDCA0000h + 4100h	00003D00h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14	0h RW	**PerPort Half Bit Pre-emphasis (PERPORTTXPEHALF):** Config bit (per port) to select between half-bit or full-bit implementation 1 - select half-bit pre-emphasis 0 - select full-bit pre-emphasis
13:11	7h RW	**PerPort HS Pre-emphasis Bias (PERPORTPETXISET):** Config bit (per port) HS Pre-emphasis Bias current offset bit (2:0) Value Preempen: deempen = 01 Preempen: deempen = 10 Preempen: deempen = 11 (preemphasis strength/demphasis strength) Value (De-emphasis ON) (Pre-emphasis ON) (preemphasis strength/demphasis strength) 000 0mV 0mV 0mV 001 40.5mV 20.5mV 20.5mV/20.5mV 010 60.5mV 30.5mV 30.5mV/30.5mV 011 102mV 52mV 52mV/52mV 100 102mV 52mV 52mV/52mV 101 142mV 72.5mV 72.5mV/72.5mV 110 162.5mV 85mV 85mV/85mV 111 202.5mV 105mV 105mV/105mV
10:8	5h RW	**PerPort HS Transmitter Bias (PERPORTTXISET):** Config bit (per port) HS Pre-emphasis Bias current offset bit2 (2:0) Value Preempen: deempen = 01 Preempen: deempen = 10 Preempen: deempen = 11 (preemphasis strength/demphasis strength) Value (De-emphasis ON) (Pre-emphasis ON) (preemphasis strength/demphasis strength) 000 0mV 0mV 0mV 001 40.5mV 20.5mV 20.5mV/20.5mV 010 60.5mV 30.5mV 30.5mV/30.5mV 011 102mV 52mV 52mV/52mV 100 102mV 52mV 52mV/52mV 101 142mV 72.5mV 72.5mV/72.5mV 110 162.5mV 85mV 85mV/85mV 111 202.5mV 105mV 105mV/105mV
7:0	0h RO	**Reserved**

17.3.3 c73usb2ad_USB2 PER PORT 2 (USB2_PER_PORT_2_PP0) - Offset 4126h

c73usb2ad_USB2 PER PORT 2

Type	Size	Offset	Default
MMIO	32 bit	FDCA0000h + 4126h	01800000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:23	3h RW	**Per Port HS Transmitter Emphasis (IUSBTXEMPHASISEN):** Config bit (per port) Enables HS transmitter Emphasis for the respective ports Value Description 00 Emphasis OFF 01 De-emphasis ON (strength = TXISET+PETXISET) Default 10 Pre-emphasis ON (strength = TXISET+PETXISET) 11 Pre-emphasis and De-emphasis ON (strength = TXISET+PETXISET)
22:0	0h RO	**Reserved**

18 USB eXtensible Device Controller Interface (xDCI)

18.1 USB xDCI Configuration Registers Summary

This chapter records the registers in Bus: 0, Device 20, Function 1.

Table 18-1. Summary of Bus: 0, Device: 20, Function: 1 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID And Vendor ID Register (DEVVENDID)	4B7E8086h
4h	4	Status And Command (STATUSCOMMAND)	00100000h
10h	4	Base Address Register (BAR)	00000004h
14h	4	Base Address Register High (BAR_HIGH)	00000000h
18h	4	Base Address Register1 (BAR1)	00000004h
1Ch	4	Base Address Register1 High (BAR1_HIGH)	00000000h
2Ch	4	Subsystem Vendor And Subsystem ID (SUBSYSTEMID)	00000000h
34h	4	Capabilities Pointer Register (CAPABILITYPTR)	00000080h
3Ch	4	Interrupt Register (INTERRUPTREG)	00000100h
80h	4	Power Management Capability Id (POWERCAPID)	48039001h
84h	4	Power Management Control And Status Register (PMECTRLSTATUS)	00000008h
90h	4	Pci Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD)	F0140009h
94h	4	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG)	01400010h
98h	4	Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)	00000000h
9Ch	4	Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG)	010F8301h
A0h	4	D0i3 And Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG)	00080800h

18.1.1 Device ID And Vendor ID Register (DEVVENDID) - Offset 0h

Device ID and Vendor ID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:1] + 0h	4B7E8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4B7Eh RO/P	**Device ID Field (DEVICEID):** Device ID identifies the particular PCI device
15:0	8086h RO	**Vendor Id Field (VENDORID):** Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device

18.1.2 Status And Command (STATUSCOMMAND) - Offset 4h

Command and Status Registers.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:1] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW/1C	**RMA Field (RMA):** Received Master Abort
28	0h RW/1C	**RTA Field (RTA):** Received Target Abort
27:21	0h RO	**Reserved**
20	1h RO	**Cap List Field (CAPLIST):** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**Interrupt Status Field (INTR_STATUS):** Interrupt Status: This bit reflects state of interrupt in the device
18:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** This field is Interrupt Disable
9	0h RO	**Reserved**
8	0h RW	**SERR Enable Field (SERR_ENABLE):** SERR Enable Not implemented
7:3	0h RO	**Reserved**
2	0h RW	**BME Field (BME):** Bus Master Enable
1	0h RW	**MSE Field (MSE):** Memory Space Enable
0	0h RO	**Reserved**

18.1.3 Base Address Register (BAR) - Offset 10h

Base Address Register Low [31:2] type[2:1] in 32bit or 64bit address range and memory space indicator [0].

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:1] + 10h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:21	000h RW	**Base Address Field (BASEADDR):** Base Address Register Low Base address of the OCP fabric memory space. Taken from Strap values as ones
20:12	0h RO	**Reserved**
11:4	00h RO	**Size Field (SIZEINDICATOR):** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**Prefetchable Field (PREFETCHABLE):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	2h RO	**Type Field (TYPE0):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** Memory Space Indicator: 0 indicates this BAR is present in the memory space.

18.1.4 Base Address Register High (BAR_HIGH) - Offset 14h

Base Address Register High enabled if [2:1] of BAR is 10.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:1] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR_HIGH):** Base Address high - MSB

18.1.5 Base Address Register1 (BAR1) - Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K type in [2:1] and memory space indicator in [0].

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:1] + 18h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR1):** Base Address1 This field is present if BAR1 is enabled through private configuration space.
11:4	00h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	2h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

18.1.6 Base Address Register1 High (BAR1_HIGH) - Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1 register is 10.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:1] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR1_HIGH):** Base Address: Base address of the OCP fabric memory space. Taken from Strap values as ones

18.1.7 Subsystem Vendor And Subsystem ID (SUBSYSTEMID) - Offset 2Ch

SVID register along with SID register is to distinguish subsystem from another.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:1] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system.
15:0	0000h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

18.1.8 Capabilities Pointer Register (CAPABILITYPTR) - Offset 34h

Capabilities Pointer register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:1] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Capabilities Pointer: Indicates what the next capability is.

18.1.9 Interrupt Register (INTERRUPTREG) - Offset 3Ch

Interrupt line Register isn't used in Bridge directly Interrupt Pin register reflects the IPIN value in private configuration space. Min_gnt register indicating the req of latency timers and max_lat register max latency.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:1] + 3Ch	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**Min GNT Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers // Re-Check Desc Padma
15:12	0h RO	**Reserved**
11:8	1h RO	**Interrupt Pin Field (INTPIN):** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW/P	**Interrupt Line Field (INTLINE):** Interrupt Line: It is used to communicate to software the interrupt line to which the interrupt pin is connected

18.1.10 Power Management Capability ID (POWERCAPID) - Offset 80h

Power Management Capability ID register points to Next Capability Structure and Power Management Capability with Power Management capabilities register for PME support and version.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:1] + 80h	48039001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	09h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved**
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h RO	**Next Cap Field (NXTCAP):** Next Capability: Points to the next capability structure.
7:0	01h RO	**Power Capability ID Field (POWER_CAP):** Power Management Capability: Indicates this is Power Management Capability

18.1.11 Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h

Power Management Control And Status Register to set and read PME Status, PME Enable, No Soft Reset and Power State.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:1] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/P	**PME Status Field (PMESTATUS):** This field is PME Status
14:9	0h RO	**Reserved**
8	0h RW/P	**PME Enable Field (PMEENABLE):** This field is PME Enable
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	0h RO	**Reserved**
1:0	0h RW	**Power State Field (POWERSTATE):** Power State: This field is used both to determine the current power state and to set a new power state

18.1.12 PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h

PCI Device Vendor Specific Capability register defines Vendor Specific Capability ID, Revision Length, Next Capability and CAPID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:1] + 90h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision ID Field (REVID):** Revision ID of Capability Structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	00h RO	**Next Capability Field (NEXT_CAP):** This field is Next Capability
7:0	09h RO	**Capability Id Field (CAPID):** This field is Capability ID

18.1.13 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h

Extended Vendor Capability Register for VSEC Length, Revision and ID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:1] + 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific Id Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor specific Extended Capability Revision
15:0	0010h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

18.1.14 Software LTR Update MMIO LSW LTR location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h

Software Location Pointer in MMIO space as an offset specified by BAR.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:1] + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR BAR Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW LTR Valid Field (SW_LAT_VALID):** This value is reflected from the SW LTR valid strap at the top level

18.1.15 Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch

Device IDLE pointer register giving details on Device MMIO offset location BAR NUM and D0i3 Valid Strap.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:1] + 9Ch	010F8301h

Bit Range	Default & Access	Field Name (ID): Description
31:4	010F830h RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** Contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR Num Field (BAR_NUM):** BAR Num: Indicates that the D0i3 MMIO location is always at BAR0
0	1h RO	**D0i3 Valid Field (VALID):** Valid: This value is reflected from the D0i3 valid strap at the top level.

18.1.16 D0i3 And Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h

D0idle_Max_Power_On_Latency register set at boot and Power control enable register to enable communication with the PGCB block below the Bridge.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:1] + A0h	00080800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW/P	**HAE Field (HAE):** Hardware Autonomous Enable
20	0h RO	**Reserved**
19	1h RW/P	**Sleep Enable Field (SLEEP_EN):** This field is Sleep Enable
18	0h RW/P	**D3 Hen Field (D3HEN):** D3-Hot Enable (D3HEN): If 1 then function will power gate when idle and the PMCSR[1:0] register in the function =11 (D3).
17	0h RW/P	**Device Idle En Field (DEVIDLEN):** DEVIDLE Enable (DEVIDLEN): If 1 then the function will power gate when idle and the DevIdle register (DevIdleC[2] = 1) is set.
16	0h RW/P	**PMC Request Enable Field (PMCRE):** PMCRE: PMC Request Enable
15:13	0h RO	**Reserved**
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** Power On Latency Scale
9:0	000h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** Power On Latency Value

19 Intel® Safety Island (Intel® SI)

19.1 Intel®SI Configuration Registers Summary

This chapter records the registers in Bus: 0, Device 26, Function 3.

Table 19-1. Summary of Bus: 0, Device: 26, Function: 3 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID And Vendor ID Register (DEVVENDID)	4B4A8086h
4h	4	Status And Command (STATUSCOMMAND)	00100000h
8h	4	Revision ID And Class Code (REVCLASSCODE)	00000000h
Ch	4	Cache Line Latency Header And BIST (CLLATHEADERBIST)	00000000h
10h	4	Base Address Register (BAR)	00000004h
14h	4	Base Address Register High (BAR_HIGH)	00000000h
18h	4	Base Address Register1 (BAR1)	00000000h
1Ch	4	Base Address Register1 High (BAR1_HIGH)	00000000h
2Ch	4	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)	00000000h
30h	4	Expansion Rom Base Address (EXPANSION_ROM_BASEADDR)	00000000h
34h	4	Capabilities Pointer (CAPABILITYPTR)	00000080h
3Ch	4	Interrupt Register (INTERRUPTREG)	00000000h
80h	4	Power Management Capability ID (POWERCAPID)	00039001h
84h	4	Power Management Control And Status Register (PMECTRLSTATUS)	00000008h
90h	4	PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD)	F014D009h
94h	4	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG)	01400010h
98h	4	Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)	00000000h
9Ch	4	Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG)	00000000h
A0h	4	D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG)	00250000h
C0h	4	General Purpose Input Register (GEN_INPUT_REG)	00000000h
D0h	4	MSI Capability Register (MSI_CAP_REG)	01800005h
D4h	4	MSI Message Low Address (MSI_ADDR_LOW)	00000000h
D8h	4	MSI Message High Address (MSI_ADDR_HIGH)	00000000h
DCh	4	MSI Message Data (MSI_MSG_DATA)	00000000h
E0h	4	MSI Mask Register (MSI_MASK)	00000000h
E4h	4	MSI Pending Register (MSI_PENDING)	00000000h
F8h	4	Manufacturers ID (MANID)	00000000h

19.1.1 Device ID And Vendor ID Register (DEVVENDID) - Offset 0h

Device ID and Vendor ID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + 0h	4B4A8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4B4Ah RO/P	**Device Id Field (DEVICEID):** Device ID identifies the particular PCI device
15:0	8086h RO	**Vendor Id Field (VENDORID):** Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device

19.1.2 Status And Command (STATUSCOMMAND) - Offset 4h

Command and Status.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**Detected Parity Error (DPE):** Detected Parity Error
30	0h RW/1C	**Signaled System Error (SSE):** Signaled System Error
29	0h RW/1C	**RMA Field (RMA):** Received Master Abort
28	0h RW/1C	**RTA Field (RTA):** Received Target Abort
27:25	0h RO	**Reserved**
24	0h RW/1C	**Master Data Parity Error (MDPE):** Master Data Parity Error
23:21	0h RO	**Reserved**
20	1h RO	**Capability List Field (CAPLIST):** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**Interrupt Status Field (INTR_STATUS):** Interrupt Status: This bit reflects state of interrupt in the device
18:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** Interrupt Disable
9	0h RO	**Reserved**
8	0h RW	**SERR Enable Field (SERR_ENABLE):** SERR Enable Not implemented
7	0h RO	**Reserved**
6	0h RW	**Parity Error Response Enable (PERE):** Parity Error Response Enable

Bit Range	Default & Access	Field Name (ID): Description
5:3	0h RO	**Reserved**
2	0h RW	**BME Field (BME):** Bus Master Enable
1	0h RW	**MSE Field (MSE):** Memory Space Enable
0	0h RO	**Reserved**

19.1.3 Revision ID And Class Code (REVCLASSCODE) - Offset 8h

Revision ID and Class Code Registers.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Revision ID Field (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	00h RO/P	**Class Code Field (RID):** Revision ID identifies the revision of particular PCI device.

19.1.4 Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch

Cache Line size as RW with def 0 Latency timer RW with def 0 Header type with Type 0 configuration header and Reserved BIST register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**Multifunction Device Field (MULFNDEV):** Multi-Function Device

Bit Range	Default & Access	Field Name (ID): Description
22:16	00h RO	**Header Type Field (HEADERTYPE):** Header Type: Implements Type 0 Configuration header
15:8	00h RO	**Latency Timer Field (LATTIMER):** Latency Timer:This register is implemented as R/W with default as 0
7:0	00h RW/P	**Cache Line Size Field (CACHELINE_SIZE):** Cache line Size

19.1.5 Base Address Register (BAR) - Offset 10h

Base Address Register Low [31:2] type[2:1] in 32bit or 64bit address range and memory space indicator [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + 10h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR):** Base Address Register Low Base address of the AXI fabric memory space. Taken from Strap values as ones
11:4	00h RO	**Size Field (SIZEINDICATOR):** Size Indicator Ro Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**Prefetchable Field (PREFETCHABLE):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	2h RO	**Type Field (TYPE0):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** Memory Space Indicator: 0 indicates this BAR is present in the memory space.

19.1.6 Base Address Register High (BAR_HIGH) - Offset 14h

Base Address Register High enabled if [2:1] of BAR_HIGH is 10.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR_HIGH):** Base Address high - MSB

19.1.7 Base Address Register1 (BAR1) - Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K type in [2:1] and memory space indicator in [0].

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR1):** Base Address1 This field is present if BAR1 is enabled through private configuration space.
11:4	00h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

19.1.8 Base Address Register1 High (BAR1_HIGH) - Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1 register is 10.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR1_HIGH):** Base Address: Base address of the AXI fabric memory space. Taken from Strap values as ones

19.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID) - Offset 2Ch

SVID register along with SID register is to distinguish subsystem from another.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O/P	**Subsystem Id Field (SUBSYSTEMID):** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system.
15:0	0000h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

19.1.10 Expansion Rom Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h

Expansion Rom Base Address Register is a Ro indicates support for expansion ROMs.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Expansion Rom base address field (EXPANSION_ROM_BASE):** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

19.1.11 Capabilities Pointer (CAPABILITYPTR) - Offset 34h

Capabilities Pointer Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Capabilities Pointer: Indicates what the next capability is.

19.1.12 Interrupt Register (INTERRUPTREG) - Offset 3Ch

Interrupt line Register isn't used in Bridge directly Interrupt Pin register reflects the IPIN value in private config space. Min_GNT register indicating the req of latency timers and Max_LAT register max latency.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + 3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**Min GNT Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	**Reserved**
11:8	0h RO	**Interrupt Pin Field (INTPIN):** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW/P	**Interrupt Line Field (INTLINE):** Interrupt Line: It is used to communicate to software the interrupt line to which the interrupt pin is connected

19.1.13 Power Management Capability ID (POWERCAPID) - Offset 80h

Power Management Capability ID register points to Next Capability Structure And Power Management Capability with Power Management capabilities register for PME support and version.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + 80h	00039001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved**
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h RO	**Next Cap Field (NXTCAP):** Next Capability: Points to the next capability structure.
7:0	01h RO	**Power Capability Id Field (POWER_CAP):** Power Management Capability: Indicates this is power management capability

19.1.14 Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h

Power Management Control And Status Register to set and read PME Status, PME Enable, No Soft Reset and Power State.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/P	**PME Status Field (PMESTATUS):** PME Status
14:9	0h RO	**Reserved**
8	0h RW/P	**PME Enable Field (PMEENABLE):** PME Enable
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	0h RO	**Reserved**
1:0	0h RW	**Power State Field (POWERSTATE):** Power State: This field is used both to determine the current power state and to set a new power state

19.1.15 PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h

PCI Device Vendor Specific Capability register defines Vendor Specific Capability ID, Revision Length, Next Capability and CAPID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + 90h	F014D009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision ID Field (REVID):** Revision ID of Capability Structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	D0h RO	**Next Capability Field (NEXT_CAP):** Next Capability
7:0	09h RO	**Capability Id Field (CAPID):** Capability ID

19.1.16 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h

Extended Vendor capability register for VSEC Length Revision and ID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific Id Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor specific Extended Capability Revision
15:0	0010h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

19.1.17 Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h

Software Location Pointer in MMIO space as an offset specified by BAR.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR BAR Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW LTR Valid Field (SW_LAT_VALID):** This value is reflected from the SW LTR valid strap at the top level

19.1.18 Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch

Device IDLE pointer register giving details on Device MMIO offset location BAR NUM and D0i3 Valid Strap.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** Contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** BAR Num: Indicates that the D0i3 MMIO location is always at BAR0
0	0h RO	**D0i3 Valid Field (VALID):** Valid: This value is reflected from the D0i3 valid strap at the top level

19.1.19 D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h

D0idle_Max_Power_On_Latency Register set at boot and Power Control Enable Register to enable communication with the PGCB block below the Bridge.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + A0h	00250000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	1h RW/P	**HAE:** Hardware Autonomous Enable
20	0h RO	**Reserved**
19	0h RW/P	**Sleep Enable Field (SLEEP_EN):** Sleep Enable
18	1h RW/P	**D3 Hen Field (D3HEN):** DEVIDLE Enable (DEVIDLEN): If '1', then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set.
17	0h RW/P	**Device Idle En Field (DEVIDLEN):** PMCRE: PMC Request Enable
16	1h RW/P	**PMC Request Enable Field (PMCRE):** D3-Hot Enable (D3HEN): If '1', then function will power gate when idle and the PMCSR[1:0] register in the function = '11' (D3).
15:13	0h RO	**Reserved**
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** Power On Latency Scale
9:0	000h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** Power On Latency Value

19.1.20 General Purpose Input Register (GEN_INPUT_REG) - Offset C0h

General Purpose Input Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General Purpose Input Register: This register value reflects the value of GEN_REG_INPUT_RW

19.1.21 MSI Capability Register (MSI_CAP_REG) - Offset D0h

MSI Capability Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + D0h	01800005h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	1h RO	**Per Vector Masking Capability Field (PER_VECTOR_MSK_CAP):** Per Vector Masking Capability
23	1h RO	**MSI Capability Field (MSI_CAP_64B):** 64 bit message address capability
22:20	0h RW	**Multi Message En Field (MUL_MSG_EN):** Multiple Message Enable
19:17	0h RO	**Multi Message Cap Field (MUL_MSG_CAP):** Multiple Message Capable
16	0h RW	**MSI Enable Field (MSG_MSI_ENABLE):** MSI Enable
15:8	00h RO	**Next Pointer Field (MSG_NXT_PTR):** Next Capability Pointer
7:0	05h RO	**MSI Capability Field (MSG_CAP_ID):** MSI Capability ID

19.1.22 MSI Message Low Address (MSI_ADDR_LOW) - Offset D4h

MSI Message Low Address.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**MSI Message Low Address Field (MSI_ADDR_LOW):** MSI Message Low Address
1:0	0h RO	**Reserved**

19.1.23 MSI Message High Address (MSI_ADDR_HIGH) - Offset D8h

MSI Message High Address.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Message High Address Field (MSI_ADDR_HIGH):** MSI Message High Address

19.1.24 MSI Message Data (MSI_MSG_DATA) - Offset DCh

MSI Message Data.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**MSI Message Data Field (MSI_MSG_DATA):** MSI Message Data

19.1.25 MSI Mask Register (MSI_MASK) - Offset E0h

MSI Mask bits.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Mask Field (MSI_MASK):** MSI Mask bits

19.1.26 MSI Pending Register (MSI_PENDING) - Offset E4h

MSI Pending bits.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**MSI Pending Field (MSI_PENDING):** MSI Pending bits

19.1.27 Manufacturers ID (MANID) - Offset F8h

Manufacturers ID register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:3] + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/P	**Manufacturers Id Field (MANID):** Manufacturer ID: Default value comes from straps.

20 General Purpose I/O

20.1 GPIO Community 0 Registers Summary

This chapter documents GPIO 0 Registers.

Table 20-1. Summary of GPIO 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8h	4	Family Base Address (FAMBAR)	00000300h
Ch	4	Pad Base Address (PADBAR)	00000700h
10h	4	Miscellaneous Configuration (MISCCFG)	32043200h
20h	4	Pad Ownership (PAD_OWN_GPP_B_0)	00000000h
24h	4	Pad Ownership (PAD_OWN_GPP_B_1)	00000000h
28h	4	Pad Ownership (PAD_OWN_GPP_B_2)	00000000h
30h	4	Pad Ownership (PAD_OWN_GPP_T_0)	00000000h
34h	4	Pad Ownership (PAD_OWN_GPP_T_1)	00000000h
38h	4	Pad Ownership (PAD_OWN_GPP_G_0)	00000000h
3Ch	4	Pad Ownership (PAD_OWN_GPP_G_1)	00000000h
40h	4	Pad Ownership (PAD_OWN_GPP_G_2)	00000000h
80h	4	Pad Configuration Lock (PADCFGLOCK_GPP_B_0)	00000000h
84h	4	Pad Configuration Lock GPIO TxState Register (PAD CFGLOCKTX_GPP_B_0)	00000000h
88h	4	Pad Configuration Lock (PAD CFGLOC_GPP_T_0)	00000000h
8Ch	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_T_0)	00000000h
90h	4	Pad Configuration Lock (PADCFGLOCK_GPP_G_0)	00000000h
94h	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_G_0)	00000000h
B0h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_B_0)	00000000h
B4h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_T_0)	00000000h
B8h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_G_0)	00000000h
100h	4	GPI Interrupt Status (GPI_IS_GPP_B_0)	00000000h
104h	4	GPI Interrupt Status (GPI_IS_GPP_T_0)	00000000h
108h	4	GPI Interrupt Status (GPI_IS_GPP_G_0)	00000000h
120h	4	GPI Interrupt Enable (GPI_IE_GPP_B_0)	00000000h
124h	4	GPI Interrupt Enable (GPI_IE_GPP_T_0)	00000000h
128h	4	GPI Interrupt Enable (GPI_IE_GPP_G_0)	00000000h
140h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_B_0)	00000000h
144h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_T_0)	00000000h
148h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_G_0)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
160h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_B_0)	00000000h
164h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_T_0)	00000000h
168h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_G_0)	00000000h
180h	4	SMI Status (GPI_SMI_STS_GPP_B_0)	00000000h
184h	4	SMI Status (GPI_SMI_STS_GPP_T_0)	00000000h
188h	4	SMI Status (GPI_SMI_STS_GPP_G_0)	00000000h
1A0h	4	SMI Enable (GPI_SMI_EN_GPP_B_0)	00000000h
1A4h	4	SMI Enable (GPI_SMI_EN_GPP_T_0)	00000000h
1A8h	4	SMI Enable (GPI_SMI_EN_GPP_G_0)	00000000h
1C0h	4	NMI Status (GPI_NMI_STS_GPP_B_0)	00000000h
1C4h	4	NMI Status (GPI_NMI_STS_GPP_T_0)	00000000h
1C8h	4	NMI Status (GPI_NMI_STS_GPP_G_0)	00000000h
1E0h	4	NMI Enable (GPI_NMI_EN_GPP_B_0)	00000000h
1E4h	4	NMI Enable (GPI_NMI_EN_GPP_T_0)	00000000h
1E8h	4	NMI Enable (GPI_NMI_EN_GPP_G_0)	00000000h
700h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_0)	44000700h
704h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_0)	00000018h
710h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_1)	44000700h
714h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_1)	00000019h
720h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_2)	44001300h
724h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_2)	0000301Ah
730h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_3)	44001300h
734h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_3)	0000301Bh
740h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_4)	44001300h
744h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_4)	0000301Ch
750h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_5)	44000300h
754h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_5)	0000001Dh
760h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_6)	44000300h
764h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_6)	0000001Eh
770h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_7)	44000300h
774h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_7)	0000001Fh
780h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_8)	44000300h
784h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_8)	00000020h
790h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_9)	44001300h
794h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_9)	00003021h
7A0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_10)	44001300h
7A4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_10)	00003022h
7B0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_11)	44000300h
7B4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_11)	00000023h
7C0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_12)	44000700h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
7C4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_12)	00000024h
7D0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_13)	44000700h
7D4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_13)	00000025h
7E0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_14)	44000200h
7E4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_14)	00000026h
7F0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_15)	44001700h
7F4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_15)	00003027h
800h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_16)	44000300h
804h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_16)	00000028h
810h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_17)	44000300h
814h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_17)	00000029h
820h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_18)	44000200h
824h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_18)	0000002Ah
830h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_19)	44001700h
834h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_19)	0000302Bh
840h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_20)	44000300h
844h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_20)	0000002Ch
850h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_21)	44000300h
854h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_21)	0000002Dh
860h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_22)	44000200h
864h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_22)	0000002Eh
870h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_23)	44000200h
874h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_23)	0000002Fh
8A0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_0)	44000300h
8A4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_0)	00000030h
8B0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_1)	44000300h
8B4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_1)	000000h
8C0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_2)	44000300h
8C4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_2)	00000032h
8D0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_3)	44000300h
8D4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_3)	00000033h
8E0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_4)	44000300h
8E4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_4)	00000034h
8F0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_5)	44000300h
8F4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_5)	00000035h
900h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_6)	44000300h
904h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_6)	00000036h
910h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_7)	44000300h
914h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_7)	00000037h
920h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_8)	44000300h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
924h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_8)	00000038h
930h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_9)	44000300h
934h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_9)	00000039h
940h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_10)	44000300h
944h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_10)	0000003Ah
950h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_11)	44000300h
954h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_11)	0000003Bh
960h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_12)	44000300h
964h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_12)	0000003Ch
970h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_13)	44000300h
974h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_13)	0000003Dh
980h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_14)	44000300h
984h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_14)	0000003Eh
990h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_15)	44000300h
994h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_15)	0000003Fh
9A0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_0)	44000300h
9A4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_0)	00000058h
9B0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_1)	44000300h
9B4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_1)	00000059h
9C0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_2)	44000300h
9C4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_2)	0000005Ah
9D0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_3)	44000300h
9D4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_3)	0000005Bh
9E0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_4)	44000300h
9E4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_4)	0000005Ch
9F0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_5)	44000300h
9F4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_5)	0000005Dh
A00h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_6)	44000300h
A04h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_6)	0000005Eh
A10h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_7)	44000300h
A14h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_7)	0000005Fh
A20h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_8)	44000B00h
A24h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_8)	00000060h
A30h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_9)	44000B00h
A34h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_9)	00000061h
A40h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_10)	44000300h
A44h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_10)	00000062h
A50h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_11)	44000300h
A54h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_11)	00000063h
A60h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_12)	44000300h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
A64h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_12)	00000064h
A70h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_13)	44000300h
A74h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_13)	00000065h
A80h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_14)	44000300h
A84h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_14)	00000066h
A90h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_15)	44000700h
A94h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_15)	00003067h
AA0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_16)	44000700h
AA4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_16)	00003068h
AB0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_17)	44000700h
AB4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_17)	00003069h
AC0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_18)	44000700h
AC4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_18)	0000306Ah
AD0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_19)	44000300h
AD4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_19)	0000006Bh
AE0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_20)	44000700h
AE4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_20)	0000306Ch
AF0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_21)	44000700h
AF4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_21)	0000106Dh
B00h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_22)	44000700h
B04h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_22)	0000006Eh
B10h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_23)	44000300h
B14h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_23)	0000006Fh

20.1.1 Family Base Address (FAMBAR) - Offset 8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 8h	00000300h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0300h RO	**Family Base Address (FAMBAR):** This field provides the starting byte-align address of Family0 register sets within a Community. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

20.1.2 Pad Base Address (PADBAR) - Offset Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + Ch	00000700h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0700h RO	**Pad Base Address (PADBAR):** This field provides the starting byte-align address of Pad0 register sets within a Community. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

20.1.3 Miscellaneous Configuration (MISCCFG) - Offset 10h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 10h	32043200h

Bit Range	Default & Access	Field Name (ID): Description
31:24	32h RW	**GPIO Driver Mode Interrupt Select (GPDMINTSEL):** IRQ globally for all pads (GPI_IS with corresponding GPI_IE enable). 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255
23:20	0h RO	**Reserved**
19:16	4h RO	**Reserved**
15:12	3h RW	**GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The setting is processor specific.
11:8	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[:0]. The setting is processor specific.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**GPIO IOSF Sideband VNNREQ Enable (GPVNNREQEN):** Specify whether the GPIO Community should take part in IOSFSB VNNREQ/ACK handshake 0 = Disable participation in IOSF SB VNNREQ and VNNACK handshake 1 = Enable participation in IOSF SB VNNREQ and VNNACK handshake When this bit set to 1, GPIO controller will de-assert the VNNREQ when there is no outstanding IOSF SB upstream cycle from GPIO controller. When this bit set to 1 and MISCSECCFG.SBTRIGDIS is 0, GPIO controller will assert the VNNREQ to request for the following list of IOSF-SB Message initiation. Event list: IRQ NMI SMI SSMI Fuse/Soft strap pull VNNREQ shall de-assert when MISCSECCFG.SBTRIGDIS is set to 1. As VNNAON IP, GPIO controller will assert the VNNREQ when in reset. The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pwrgate_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this power gating, this register always default to 1.
6	0h RW	**GPIO PGCB Clock Dynamic Partition Clock Gating Enable (GPPGCBDPCGEN):** Specify whether the GPIO Community PGCB clock should take part in partition clock gating 0 = Disable participation in PGCB clock dynamic partition clock gating 1 = Enable participation in PGCB clock dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
5	0h RW	**GPIO IOSF Sideband Dynamic Partition Clock Gating Enable (GPSIDEDPCGEN):** Specify whether the GPIO Community IOSF sideband clock should take part in partition clock gating 0 = Disable participation in IOSF sideband clock dynamic partition clock gating 1 = Enable participation in IOSF sideband clock dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
4	0h RW	**GPIO RCOMP clock Dynamic Local Clock Gating (GPRCOMPCDLCGEN):** Specify whether the GPIO Community should perform local clock gating on RCOMP clock 0 = Disable dynamic RCOMP clock local clock gating 1 = Enable dynamic RCOMP clock local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GPIO RTC clock Dynamic Local Clock Gating (GPRTCDLCGEN):** Specify whether the GPIO Community should perform local clock gating on RTC clock 0 = Disable dynamic RTC clock local clock gating 1 = Enable dynamic RTC clock local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
2	0h RO	**Reserved**
1	0h RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN):** Specify whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
0	0h RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN):** Specify whether the GPIO Community should perform local clock gating 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0

20.1.4 Pad Ownership (PAD_OWN_GPP_B_0) - Offset 20h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = Reserved '11' = Reserved All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_6):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.1.5 Pad Ownership (PAD_OWN_GPP_B_1) - Offset 24h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 24h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_15):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_14):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_13):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_12):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_11):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_10):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_9):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_8):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.1.6 Pad Ownership (PAD_OWN_GPP_B_2) - Offset 28h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 28h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_23):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_22):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_21):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_20):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_19):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_18):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_17):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_16):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.1.7 Pad Ownership (PAD_OWN_GPP_T_0) - Offset 30h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_T_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_T_6):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_T_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_T_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_T_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_T_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_T_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_T_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.1.8 Pad Ownership (PAD_OWN_GPP_T_1) - Offset 34h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_T_15):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_T_14):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_T_13):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_T_12):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_T_11):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_T_10):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_T_9):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_T_8):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.1.9 Pad Ownership (PAD_OWN_GPP_G_0) - Offset 38h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_6):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.1.10 Pad Ownership (PAD_OWN_GPP_G_1) - Offset 3Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_15):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_14):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_13):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_12):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_11):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_10):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_9):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_8):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.1.11 Pad Ownership (PAD_OWN_GPP_G_2) - Offset 40h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_23):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_22):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_21):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_20):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_19):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_18):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_17):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_G_16):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.1.12 Pad Configuration Lock (PADCFGLOCK_GPP_B_0) - Offset 80h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_23):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
22	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_22):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_21):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
20	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_20):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_19):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
18	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_18):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_17):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
16	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_16):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_15):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_14):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_13):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_12):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_11):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_10):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_9):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_8):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_6):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

20.1.13 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_B_0) - Offset 84h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_23):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
22	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_22):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_21):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
20	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_20):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_19):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
18	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_18):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_17):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
16	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_16):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_15):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_14):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_13):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_12):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_11):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_10):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_9):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_8):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_6):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

20.1.14 Pad Configuration Lock (PADCFGLOCK_GPP_T_0) - Offset 88h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_T_15):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_T_14):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_T_13):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_T_12):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_T_11):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_T_10):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_T_9):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_T_8):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_T_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_T_6):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_T_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_T_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_T_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_T_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_T_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_T_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

20.1.15 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_T_0) - Offset 8Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 8Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_T_15):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_T_14):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_T_13):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_T_12):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_T_11):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_T_10):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_T_9):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_T_8):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_T_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_T_6):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_T_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_T_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_T_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_T_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_T_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_T_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

20.1.16 Pad Configuration Lock (PADCFGLOCK_GPP_G_0) - Offset 90h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_23):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
22	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_22):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_21):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
20	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_20):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_19):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
18	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_18):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_17):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
16	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_16):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_15):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_14):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_13):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_12):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_11):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_10):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_9):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_8):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_6):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_G_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

20.1.17 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_G_0) - Offset 94h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_23):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
22	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_22):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_21):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
20	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_20):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_19):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
18	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_18):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_17):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
16	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_16):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_15):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_14):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_13):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_12):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_11):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_10):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_9):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_8):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_6):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_G_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

20.1.18 Host Software Pad Ownership (HOSTSW_OWN_GPP_B_0) - Offset B0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**HOSTSW_OWN_GPPC_B_23:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
22	0h RW	**HOSTSW_OWN_GPPC_B_22:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
21	0h RW	**HOSTSW_OWN_GPPC_B_21:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**HOSTSW_OWN_GPPC_B_20:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
19	0h RW	**HOSTSW_OWN_GPPC_B_19:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
18	0h RW	**HOSTSW_OWN_GPPC_B_18:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**HOSTSW_OWN_GPPC_B_17:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
16	0h RW	**HOSTSW_OWN_GPPC_B_16:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
15	0h RW	**HOSTSW_OWN_GPPC_B_15:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**HOSTSW_OWN_GPPC_B_14:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
13	0h RW	**HOSTSW_OWN_GPPC_B_13:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
12	0h RW	**HOSTSW_OWN_GPPC_B_12:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**HOSTSW_OWN_GPPC_B_11:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
10	0h RW	**HOSTSW_OWN_GPPC_B_10:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
9	0h RW	**HOSTSW_OWN_GPPC_B_9:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**HOSTSW_OWN_GPPC_B_8:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
7	0h RW	**HOSTSW_OWN_GPPC_B_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
6	0h RW	**HOSTSW_OWN_GPPC_B_6:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**HOSTSW_OWN_GPPC_B_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
4	0h RW	**HOSTSW_OWN_GPPC_B_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
3	0h RW	**HOSTSW_OWN_GPPC_B_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPPC_B_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPPC_B_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPPC_B_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

20.1.19 Host Software Pad Ownership (HOSTSW_OWN_GPP_T_0) - Offset B4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**HOSTSW_OWN_GPPC_T_15:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
14	0h RW	**HOSTSW_OWN_GPPC_T_14:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**HOSTSW_OWN_GPPC_T_13:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
12	0h RW	**HOSTSW_OWN_GPPC_T_12:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
11	0h RW	**HOSTSW_OWN_GPPC_T_11:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**HOSTSW_OWN_GPPC_T_10:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
9	0h RW	**HOSTSW_OWN_GPPC_T_9:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
8	0h RW	**HOSTSW_OWN_GPPC_T_8:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**HOSTSW_OWN_GPPC_T_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
6	0h RW	**HOSTSW_OWN_GPPC_T_6:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
5	0h RW	**HOSTSW_OWN_GPPC_T_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**HOSTSW_OWN_GPPC_T_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
3	0h RW	**HOSTSW_OWN_GPPC_T_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPPC_T_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPPC_T_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPPC_T_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

20.1.20 Host Software Pad Ownership (HOSTSW_OWN_GPP_G_0) - Offset B8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**HOSTSW_OWN_GPPC_G_23:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
22	0h RW	**HOSTSW_OWN_GPPC_G_22:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**HOSTSW_OWN_GPPC_G_21:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
20	0h RW	**HOSTSW_OWN_GPPC_G_20:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
19	0h RW	**HOSTSW_OWN_GPPC_G_19:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**HOSTSW_OWN_GPPC_G_18:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
17	0h RW	**HOSTSW_OWN_GPPC_G_17:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
16	0h RW	**HOSTSW_OWN_GPPC_G_16:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**HOSTSW_OWN_GPPC_G_15:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
14	0h RW	**HOSTSW_OWN_GPPC_G_14:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
13	0h RW	**HOSTSW_OWN_GPPC_G_13:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**HOSTSW_OWN_GPPC_G_12:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
11	0h RW	**HOSTSW_OWN_GPPC_G_11:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
10	0h RW	**HOSTSW_OWN_GPPC_G_10:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**HOSTSW_OWN_GPPC_G_9:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
8	0h RW	**HOSTSW_OWN_GPPC_G_8:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
7	0h RW	**HOSTSW_OWN_GPPC_G_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**HOSTSW_OWN_GPPC_G_6:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
5	0h RW	**HOSTSW_OWN_GPPC_G_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
4	0h RW	**HOSTSW_OWN_GPPC_G_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**HOSTSW_OWN_GPPC_G_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPPC_G_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPPC_G_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPPC_G_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

20.1.21 GPI Interrupt Status (GPI_IS_GPP_B_0) - Offset 100h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 100h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_23):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_22):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_21):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
20	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_20):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
19	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_19):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_18):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
17	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_17):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
16	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_16):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_15):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_14):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_13):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_12):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_11):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_10):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_9):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_8):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_6):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.1.22 GPI Interrupt Status (GPI_IS_GPP_T_0) - Offset 104h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 104h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_T_15):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_T_14):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_T_13):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_T_12):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_T_11):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_T_10):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_T_9):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_T_8):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_T_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_T_6):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_T_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_T_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_T_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_T_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_T_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_T_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.1.23 GPI Interrupt Status (GPI_IS_GPP_G_0) - Offset 108h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 108h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_23):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_22):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
21	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_21):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_20):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
19	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_19):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_18):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_17):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
16	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_16):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_15):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_14):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_13):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_12):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_11):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_10):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_9):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_8):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_6):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_G_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.1.24 GPI Interrupt Enable (GPI_IE_GPP_B_0) - Offset 120h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 120h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_23):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_22):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
21	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_21):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_20):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
19	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_19):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_18):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
17	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_17):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_16):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_15):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_14):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_13):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_12):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_11):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_10):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_9):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_8):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_6):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.1.25 GPI Interrupt Enable (GPI_IE_GPP_T_0) - Offset 124h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 124h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_T_15):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_T_14):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_T_13):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_T_12):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_T_11):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_T_10):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_T_9):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_T_8):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_T_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_T_6):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_T_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_T_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_T_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_T_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_T_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_T_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.1.26 GPI Interrupt Enable (GPI_IE_GPP_G_0) - Offset 128h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 128h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_23):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_22):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
21	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_21):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_20):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
19	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_19):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_18):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
17	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_17):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_16):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_15):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_14):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_13):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_12):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_11):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_10):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_9):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_8):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_6):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_G_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.1.27 GPI General Purpose Events Status (GPI_GPE_STS_GPP_B_0) - Offset 140h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 140h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_23):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_22):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_21):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
20	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_20):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
19	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_19):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_18):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
17	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_17):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_16):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_15):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_14):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_13):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_12):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_11):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_10):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_9):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_8):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_6):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.1.28 GPI General Purpose Events Status (GPI_GPE_STS_GPP_T_0) - Offset 144h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 144h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_T_15):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_T_14):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_T_13):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
12	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_T_12):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_T_11):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_T_10):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
9	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_T_9):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_T_8):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_T_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_T_6):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_T_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_T_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_T_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_T_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_T_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_T_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.1.29 GPI General Purpose Events Status (GPI_GPE_STS_GPP_G_0) - Offset 148h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 148h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_23):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_22):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_21):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
20	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_20):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
19	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_19):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_18):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
17	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_17):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_16):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_15):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_14):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_13):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_12):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_11):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_10):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_9):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_8):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_6):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_G_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.1.30 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_B_0) - Offset 160h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 160h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_23):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_22):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
21	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_21):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_20):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
19	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_19):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
18	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_18):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
17	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_17):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_16):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_15):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_14):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_13):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_12):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_11):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_10):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_9):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_8):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_6):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.1.31 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_T_0) - Offset 164h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 164h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_T_15):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_T_14):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_T_13):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_T_12):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_T_11):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_T_10):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_T_9):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_T_8):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_T_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_T_6):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_T_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_T_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_T_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_T_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_T_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_T_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.1.32 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_G_0) - Offset 168h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 168h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_23):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_22):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
21	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_21):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_20):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
19	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_19):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
18	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_18):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
17	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_17):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_16):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_15):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_14):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_13):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_12):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_11):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_10):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_9):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_8):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_6):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_G_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.1.33 SMI Status (GPI_SMI_STS_GPP_B_0) - Offset 180h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 180h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_B_23):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
22	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_22):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_21):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
20	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_B_20):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_19):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
18	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_18):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_17):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
16	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_16):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_15):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
14	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_B_14):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_13):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
12	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_12):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_11):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
10	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_10):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_9):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
8	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_8):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
6	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_6):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
4	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

20.1.34 SMI Status (GPI_SMI_STS_GPP_T_0) - Offset 184h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 184h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_T_15):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
14	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_T_14):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_T_13):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
12	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_T_12):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_T_11):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
10	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_T_10):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_T_9):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
8	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_T_8):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_T_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
6	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_T_6):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_T_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
4	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_T_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_T_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_T_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_T_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_T_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

20.1.35 SMI Status (GPI_SMI_STS_GPP_G_0) - Offset 188h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 188h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_23):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
22	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_22):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_21):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
20	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_20):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_19):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
18	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_18):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_17):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
16	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_16):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_15):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
14	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_14):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_13):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
12	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_12):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_11):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
10	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_10):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_9):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
8	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_8):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
6	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_6):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
4	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_G_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

20.1.36 SMI Enable (GPI_SMI_EN_GPP_B_0) - Offset 1A0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 1A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_23):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
22	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_22):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
21	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_21):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_20):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
19	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_19):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
18	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_18):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_17):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
16	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_16):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
15	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_15):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_14):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
13	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_13):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
12	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_12):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_11):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
10	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_10):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
9	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_9):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_8):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
7	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
6	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_6):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
4	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
3	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

20.1.37 SMI Enable (GPI_SMI_EN_GPP_T_0) - Offset 1A4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 1A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_T_15):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
14	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_T_14):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
13	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_T_13):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
12	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_T_12):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
11	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_T_11):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
10	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_T_10):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
9	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_T_9):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
8	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_T_8):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_T_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
6	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_T_6):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
5	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_T_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_T_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
3	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_T_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_T_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_T_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_T_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

20.1.38 SMI Enable (GPI_SMI_EN_GPP_G_0) - Offset 1A8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 1A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_23):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
22	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_22):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
21	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_21):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
20	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_20):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
19	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_19):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
18	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_18):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
17	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_17):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
16	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_16):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_15):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
14	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_14):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
13	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_13):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_12):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
11	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_11):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
10	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_10):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_9):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
8	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_8):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
7	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_6):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
5	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
4	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_G_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

20.1.39 NMI Status (GPI_NMI_STS_GPP_B_0) - Offset 1C0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 1C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_B_23):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_22):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_21):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
20	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_B_20):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
19	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_19):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_18):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
17	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_17):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_16):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_15):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_B_14):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_13):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_12):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_11):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_10):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_9):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_8):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_6):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.1.40 NMI Status (GPI_NMI_STS_GPP_T_0) - Offset 1C4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 1C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_T_15):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_T_14):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_T_13):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
12	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_T_12):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_T_11):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_T_10):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
9	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_T_9):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_T_8):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_T_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_T_6):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_T_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_T_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_T_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_T_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_T_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_T_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.1.41 NMI Status (GPI_NMI_STS_GPP_G_0) - Offset 1C8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 1C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_23):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_22):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_21):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
20	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_20):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
19	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_19):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_18):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
17	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_17):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_16):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_15):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_14):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_13):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_12):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_11):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_10):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_9):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_8):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_6):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_G_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.1.42 NMI Enable (GPI_NMI_EN_GPP_B_0) - Offset 1E0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 1E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_23):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_22):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_21):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
20	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_20):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
19	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_19):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_18):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
17	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_17):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_16):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_15):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_14):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_13):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_12):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_11):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_10):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_9):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_8):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_6):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.1.43 NMI Enable (GPI_NMI_EN_GPP_T_0) - Offset 1E4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 1E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_T_15):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_T_14):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_T_13):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_T_12):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_T_11):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_T_10):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_T_9):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_T_8):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_T_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_T_6):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_T_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_T_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_T_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_T_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_T_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_T_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.1.44 NMI Enable (GPI_NMI_EN_GPP_G_0) - Offset 1E8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 1E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_23):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_22):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
21	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_21):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_20):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
19	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_19):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
18	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_18):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_17):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_16):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
15	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_15):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_14):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_13):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
12	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_12):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_11):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_10):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
9	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_9):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_8):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_6):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_G_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.1.45 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_0) - Offset 700h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 700h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.46 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_0) - Offset 704h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 704h	00000018h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	I2C Enable (I2CEN): 00 = CMOS mode 01 = I2C mode 10 = Reserved 11 = Reserved
29	0h RW	**Current Source Enable (CSEN):** Current Source enable for I2C High Speed Mode.
28	0h RO	Park Mode Enable (parkmodeen_b): Park Mode can be used to lower the TX buffer leakage power when there is no new data to be transmitted.
27:26	0h RO	**Hysteresis Control (hysctl)**
25	0h RO	**Pad Tolerance (padtol):** When padtol = 0, v1p8mode = "0", PAD and VCCIO both "3.3V" tolerant. v1p8mode = "1", PAD and VCCIO both "1.8V" tolerant. When padtol = 1, v1p8mode = "0", PAD 1.8V tolerant and VCCIO "3.3V" tolerant.
24:22	0h RO	**Driver Impedance Selection (strsel) :** For a single voltage family, this register controls the buffer strsel. Increasing the value of the field decreases the impedance. For a dual voltage family, when v1p8mode is 0, this register controls the buffer strsel. Increasing the value of the field decreases the impedance.
21	0h RO	**High Speed Mode (hsmode)**
20	0h RO	**On Die Termination Up or Down (odtupdn):** Mode on die termination up and down. 0 - Pull down termination 1 - Pull up termination
19	0h RO	**On Die Termination Enable (odten):** Mode on die termination enable (active high).
18	0h RO	**Analog Mux Enable (analogmuxen)**
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	18h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.47 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_1) - Offset 710h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 710h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.48 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_1) - Offset 714h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 714h	00000019h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	19h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.49 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_2) - Offset 720h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 720h	44001300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	4h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.50 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_2) - Offset 724h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 724h	0000301Ah

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Ch RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	1Ah RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.51 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_3) - Offset 730h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 730h	44001300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	4h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.52 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_3) - Offset 734h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 734h	0000301Bh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Ch RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	1Bh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.53 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_4) - Offset 740h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 740h	44001300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	4h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.54 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_4) - Offset 744h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 744h	0000301Ch

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Ch RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	1Ch RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.55 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_5) - Offset 750h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 750h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.56 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_5) - Offset 754h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 754h	0000001Dh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	1Dh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.57 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_6) - Offset 760h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 760h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.58 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_6) - Offset 764h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 764h	0000001Eh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	1Eh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.59 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_7) - Offset 770h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 770h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.60 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_7) - Offset 774h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 774h	0000001Fh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	1Fh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.61 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_8) - Offset 780h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 780h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.62 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_8) - Offset 784h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 784h	00000020h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	20h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.63 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_9) - Offset 790h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 790h	44001300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	4h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.64 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_9) - Offset 794h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 794h	00003021h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Ch RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	21h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.65 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_10) - Offset 7A0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 7A0h	44001300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	4h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.66 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_10) - Offset 7A4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 7A4h	00003022h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Ch RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	22h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.67 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_11) - Offset 7B0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 7B0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.68 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_11) - Offset 7B4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 7B4h	00000023h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	23h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.69 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_12) - Offset 7C0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 7C0h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.70 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_12) - Offset 7C4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 7C4h	00000024h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	24h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.71 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_13) - Offset 7D0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 7D0h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.72 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_13) - Offset 7D4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 7D4h	00000025h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	25h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.73 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_14) - Offset 7E0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 7E0h	44000200h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.74 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_14) - Offset 7E4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 7E4h	00000026h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	26h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.75 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_15) - Offset 7F0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 7F0h	44001700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	5h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.76 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_15) - Offset 7F4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 7F4h	00003027h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Ch RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	27h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.77 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_16) - Offset 800h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 800h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.78 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_16) - Offset 804h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 804h	00000028h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	28h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.79 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_17) - Offset 810h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 810h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.80 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_17) - Offset 814h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 814h	00000029h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	29h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.81 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_18) - Offset 820h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 820h	44000200h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.82 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_18) - Offset 824h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 824h	0000002Ah

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	2Ah RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.83 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_19) - Offset 830h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 830h	44001700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	5h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.84 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_19) - Offset 834h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 834h	0000302Bh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Ch RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	2Bh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.85 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_20) - Offset 840h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 840h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.86 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_20) - Offset 844h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 844h	0000002Ch

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	2Ch RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.87 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_21) - Offset 850h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 850h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.88 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_21) - Offset 854h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 854h	0000002Dh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	2Dh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.89 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_22) - Offset 860h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 860h	44000200h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.90 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_22) - Offset 864h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 864h	0000002Eh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	2Eh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.91 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_23) - Offset 870h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 870h	44000200h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.92 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_23) - Offset 874h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 874h	0000002Fh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	2Fh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.93 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_0) - Offset 8A0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 8A0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.94 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_0) - Offset 8A4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 8A4h	00000030h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	30h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.95 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_1) - Offset 8B0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 8B0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.96 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_1) - Offset 8B4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 8B4h	000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.97 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_2) - Offset 8C0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 8C0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.98 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_2) - Offset 8C4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 8C4h	00000032h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	32h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.99 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_3) - Offset 8D0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 8D0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.100 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_3) - Offset 8D4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 8D4h	00000033h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	33h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.101 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_4) - Offset 8E0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 8E0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.102 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_4) - Offset 8E4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 8E4h	00000034h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	34h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.103 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_5) - Offset 8F0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 8F0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.104 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_5) - Offset 8F4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 8F4h	00000035h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	35h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.105 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_6) - Offset 900h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 900h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RW	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.106 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_6) - Offset 904h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 904h	00000036h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	36h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.107 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_7) - Offset 910h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 910h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.108 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_7) - Offset 914h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 914h	00000037h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	37h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.109 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_8) - Offset 920h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 920h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RW	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.110 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_8) - Offset 924h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 924h	00000038h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	38h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.111 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_9) - Offset 930h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 930h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.112 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_9) - Offset 934h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 934h	00000039h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	39h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.113 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_10) - Offset 940h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 940h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.114 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_10) - Offset 944h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 944h	0000003Ah

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	3Ah RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.115 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_11) - Offset 950h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 950h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RW	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.116 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_11) - Offset 954h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 954h	0000003Bh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	3Bh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.117 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_12) - Offset 960h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 960h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.118 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_12) - Offset 964h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 964h	0000003Ch

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	3Ch RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.119 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_13) - Offset 970h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 970h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.120 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_13) - Offset 974h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 974h	0000003Dh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	3Dh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.121 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_14) - Offset 980h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 980h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.122 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_14) - Offset 984h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 984h	0000003Eh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	3Eh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.123 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_15) - Offset 990h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 990h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.124 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_15) - Offset 994h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 994h	0000003Fh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	3Fh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.125 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_0) - Offset 9A0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 9A0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.126 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_0) - Offset 9A4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 9A4h	00000058h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	58h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.127 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_1) - Offset 9B0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 9B0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.128 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_1) - Offset 9B4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 9B4h	00000059h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	59h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.129 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_2) - Offset 9C0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 9C0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.130 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_2) - Offset 9C4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 9C4h	0000005Ah

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	5Ah RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.131 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_3) - Offset 9D0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 9D0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.132 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_3) - Offset 9D4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 9D4h	0000005Bh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	5Bh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.133 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_4) - Offset 9E0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 9E0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.134 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_4) - Offset 9E4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 9E4h	0000005Ch

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	5Ch RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.135 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_5) - Offset 9F0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 9F0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.136 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_5) - Offset 9F4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 9F4h	0000005Dh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	5Dh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.137 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_6) - Offset A00h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + A00h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.138 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_6) - Offset A04h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + A04h	0000005Eh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	5Eh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.139 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_7) - Offset A10h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + A10h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.140 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_7) - Offset A14h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + A14h	0000005Fh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	5Fh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.141 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_8) - Offset A20h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + A20h	44000B00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	2h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.142 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_8) - Offset A24h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + A24h	00000060h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	60h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.143 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_9) - Offset A30h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + A30h	44000B00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	2h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.144 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_9) - Offset A34h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + A34h	00000061h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	61h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.145 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_10) - Offset A40h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + A40h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.146 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_10) - Offset A44h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + A44h	00000062h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	62h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.147 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_11) - Offset A50h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + A50h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.148 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_11) - Offset A54h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + A54h	00000063h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	63h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.149 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_12) - Offset A60h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + A60h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.150 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_12) - Offset A64h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + A64h	00000064h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	64h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.151 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_13) - Offset A70h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + A70h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.152 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_13) - Offset A74h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + A74h	00000065h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	65h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.153 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_14) - Offset A80h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + A80h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.154 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_14) - Offset A84h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + A84h	00000066h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	66h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.155 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_15) - Offset A90h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + A90h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.156 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_15) - Offset A94h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + A94h	00003067h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Ch RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	67h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.157 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_16) - Offset AA0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + AA0h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.158 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_16) - Offset AA4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + AA4h	00003068h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Ch RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	68h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.159 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_17) - Offset AB0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + AB0h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	1h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.160 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_17) - Offset AB4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + AB4h	00003069h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Ch RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	69h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.161 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_18) - Offset AC0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + AC0h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	1h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.162 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_18) - Offset AC4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + AC4h	0000306Ah

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Ch RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	6Ah RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.163 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_19) - Offset AD0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + AD0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.164 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_19) - Offset AD4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + AD4h	0000006Bh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	6Bh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.165 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_20) - Offset AE0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + AE0h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.166 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_20) - Offset AE4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + AE4h	0000306Ch

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Ch RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	6Ch RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.167 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_21) - Offset AF0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + AF0h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.168 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_21) - Offset AF4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + AF4h	0000106Dh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	4h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	6Dh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.169 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_22) - Offset B00h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + B00h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.170 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_22) - Offset B04h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + B04h	0000006Eh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	6Eh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.1.171 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_23) - Offset B10h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + B10h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.1.172 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_23) - Offset B14h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + B14h	0000006Fh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	6Fh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2 GPIO Community 1 Registers Summary

This chapter documents GPIO 1 Registers.

Table 20-2. Summary of GPIO 1 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8h	4	Family Base Address (FAMBAR)	00000300h
Ch	4	Pad Base Address (PADBAR)	00000700h
10h	4	Miscellaneous Configuration (MISCCFG)	33043200h
20h	4	Pad Ownership (PAD_OWN_GPP_V_0)	00000000h
24h	4	Pad Ownership (PAD_OWN_GPP_V_1)	00000000h
28h	4	Pad Ownership (PAD_OWN_GPP_H_0)	00000000h
2Ch	4	Pad Ownership (PAD_OWN_GPP_H_1)	00000000h
30h	4	Pad Ownership (PAD_OWN_GPP_H_2)	00000000h
34h	4	Pad Ownership (PAD_OWN_GPP_D_0)	00000000h
38h	4	Pad Ownership (PAD_OWN_GPP_D_1)	00000000h
3Ch	4	Pad Ownership (PAD_OWN_GPP_D_2)	00000000h
40h	4	Pad Ownership (PAD_OWN_GPP_U_0)	00000000h
44h	4	Pad Ownership (PAD_OWN_GPP_U_1)	00000000h
48h	4	Pad Ownership (PAD_OWN_GPP_U_2)	00000000h
80h	4	Pad Configuration Lock (PADCFGLOCK_GPP_V_0)	00000000h
84h	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_V_0)	00000000h
88h	4	Pad Configuration Lock (PADCFGLOCK_GPP_H_0)	00000000h
8Ch	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_H_0)	00000000h
90h	4	Pad Configuration Lock (PADCFGLOCK_GPP_D_0)	00000000h
94h	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_D_0)	00000000h
98h	4	Pad Configuration Lock (PADCFGLOCK_GPP_U_0)	00000000h
9Ch	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_U_0)	00000000h
B0h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_V_0)	00000000h
B4h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_H_0)	00000000h
B8h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_D_0)	00000000h
BCh	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_U_0)	00000000h
100h	4	GPI Interrupt Status (GPI_IS_GPP_V_0)	00000000h
104h	4	GPI Interrupt Status (GPI_IS_GPP_H_0)	00000000h
108h	4	GPI Interrupt Status (GPI_IS_GPP_D_0)	00000000h
10Ch	4	GPI Interrupt Status (GPI_IS_GPP_U_0)	00000000h
120h	4	GPI Interrupt Enable (GPI_IE_GPP_V_0)	00000000h
124h	4	GPI Interrupt Enable (GPI_IE_GPP_H_0)	00000000h
128h	4	GPI Interrupt Enable (GPI_IE_GPP_D_0)	00000000h
12Ch	4	GPI Interrupt Enable (GPI_IE_GPP_U_0)	00000000h
140h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_V_0)	00000000h
144h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_H_0)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
148h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_D_0)	00000000h
14Ch	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_U_0)	00000000h
160h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_V_0)	00000000h
164h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_H_0)	00000000h
168h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_D_0)	00000000h
16Ch	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_U_0)	00000000h
180h	4	SMI Status (GPI_SMI_STS_GPP_V_0)	00000000h
184h	4	SMI Status (GPI_SMI_STS_GPP_H_0)	00000000h
188h	4	SMI Status (GPI_SMI_STS_GPP_D_0)	00000000h
18Ch	4	SMI Status (GPI_SMI_STS_GPP_U_0)	00000000h
1A0h	4	SMI Enable (GPI_SMI_EN_GPP_V_0)	00000000h
1A4h	4	SMI Enable (GPI_SMI_EN_GPP_H_0)	00000000h
1A8h	4	SMI Enable (GPI_SMI_EN_GPP_D_0)	00000000h
1ACh	4	SMI Enable (GPI_SMI_EN_GPP_U_0)	00000000h
1C0h	4	NMI Status (GPI_NMI_STS_GPP_V_0)	00000000h
1C4h	4	NMI Status (GPI_NMI_STS_GPP_H_0)	00000000h
1C8h	4	NMI Status (GPI_NMI_STS_GPP_D_0)	00000000h
1CCh	4	NMI Status (GPI_NMI_STS_GPP_U_0)	00000000h
1E0h	4	NMI Enable (GPI_NMI_EN_GPP_V_0)	00000000h
1E4h	4	NMI Enable (GPI_NMI_EN_GPP_H_0)	00000000h
1E8h	4	NMI Enable (GPI_NMI_EN_GPP_D_0)	00000000h
1ECh	4	NMI Enable (GPI_NMI_EN_GPP_U_0)	00000000h
204h	4	PWM Control (PWMC)	00000000h
20Ch	4	GPIO Serial Blink Enable (GP_SER_BLINK)	00000000h
210h	4	GPIO Serial Blink Command/Status (GP_SER_CMDSTS)	00080000h
214h	4	GPIO Serial Blink Data (GP_SER_DATA)	00000000h
700h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_0)	44000300h
704h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_0)	0000002Ch
710h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_1)	44000300h
714h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_1)	0000002Dh
720h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_2)	44000300h
724h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_2)	0000002Eh
730h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_3)	44000300h
734h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_3)	0000002Fh
740h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_4)	44000300h
744h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_4)	00000030h
750h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_5)	44000300h
754h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_5)	000000h
760h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_6)	44000300h
764h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_6)	00000032h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
770h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_7)	44000300h
774h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_7)	00000033h
780h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_8)	44000300h
784h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_8)	00000034h
790h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_9)	44000300h
794h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_9)	00000035h
7A0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_10)	44000300h
7A4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_10)	00000036h
7B0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_11)	44000300h
7B4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_11)	00000037h
7C0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_12)	44000300h
7C4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_12)	00000038h
7D0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_13)	44000300h
7D4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_13)	00000039h
7E0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_14)	44000300h
7E4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_14)	0000003Ah
7F0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_15)	44000300h
7F4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_15)	0000003Bh
800h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_0)	44000200h
804h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_0)	0000003Ch
810h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_1)	44000300h
814h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_1)	0000003Dh
820h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_2)	44000200h
824h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_2)	0000003Eh
830h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_3)	44000300h
834h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_3)	0000003Fh
840h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_4)	44000300h
844h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_4)	00000040h
850h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_5)	44000300h
854h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_5)	00000041h
860h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_6)	44000300h
864h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_6)	00000042h
870h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_7)	44000300h
874h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_7)	00000043h
880h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_8)	44000300h
884h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_8)	00000044h
890h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_9)	44000300h
894h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_9)	00000045h
8A0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_10)	44000300h
8A4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_10)	00000046h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8B0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_11)	44000300h
8B4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_11)	00000047h
8C0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_12)	44000300h
8C4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_12)	00000048h
8D0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_13)	44000300h
8D4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_13)	00000049h
8E0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_14)	44000300h
8E4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_14)	0000004Ah
8F0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_15)	44000300h
8F4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_15)	0000004Bh
900h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_16)	44000300h
904h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_16)	0000004Ch
910h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_17)	44000300h
914h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_17)	0000004Dh
920h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_18)	44000700h
924h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_18)	0000004Eh
930h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_19)	44000300h
934h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_19)	0000004Fh
940h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_20)	44000300h
944h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_20)	00000050h
950h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_21)	44000300h
954h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_21)	00000051h
960h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_22)	44000300h
964h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_22)	00000052h
970h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_23)	44000300h
974h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_23)	00000053h
980h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_0)	44000300h
984h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_0)	00000054h
990h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_1)	44000300h
994h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_1)	0000006Eh
9A0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_2)	44000300h
9A4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_2)	0000006Fh
9B0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_3)	44000300h
9B4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_3)	00000070h
9C0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_4)	44000300h
9C4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_4)	00000071h
9D0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_5)	44000300h
9D4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_5)	00000072h
9E0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_6)	44000300h
9E4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_6)	00000073h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
9F0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_7)	44000300h
9F4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_7)	00000074h
A00h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_8)	44000300h
A04h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_8)	00000075h
A10h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_9)	44000300h
A14h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_9)	00000076h
A20h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_10)	44000300h
A24h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_10)	00000077h
A30h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_11)	44000300h
A34h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_11)	00000018h
A40h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_12)	44000300h
A44h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_12)	00000019h
A50h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_13)	44000300h
A54h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_13)	0000001Ah
A60h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_14)	44000300h
A64h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_14)	0000001Bh
A70h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_15)	44000300h
A74h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_15)	0000001Ch
A80h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_16)	44000300h
A84h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_16)	0000001Dh
A90h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_17)	44000300h
A94h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_17)	0000001Eh
AA0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_18)	44000300h
AA4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_18)	0000001Fh
AB0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_19)	44000300h
AB4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_19)	00000020h
AD0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_0)	44000300h
AD4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_0)	00000022h
AE0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_1)	44000300h
AE4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_1)	00000023h
AF0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_2)	44000300h
AF4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_2)	00000024h
B00h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_3)	44000300h
B04h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_3)	00000025h
B10h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_4)	44000300h
B14h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_4)	00000056h
B20h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_5)	44000300h
B24h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_5)	00000057h
B30h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_6)	44000300h
B34h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_6)	00000058h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
B40h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_7)	44000300h
B44h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_7)	00000059h
B50h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_8)	44000300h
B54h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_8)	0000005Ah
B60h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_9)	44000300h
B64h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_9)	0000005Bh
B70h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_10)	44000300h
B74h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_10)	0000005Ch
B80h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_11)	44000300h
B84h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_11)	0000005Dh
B90h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_12)	44000700h
B94h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_12)	0000105Eh
BA0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_13)	44000700h
BA4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_13)	0000105Fh
BB0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_14)	44000300h
BB4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_14)	00000060h
BC0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_15)	44000300h
BC4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_15)	00000061h
BD0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_16)	44600700h
BD4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_16)	00000062h
BE0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_17)	44600700h
BE4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_17)	00000063h
BF0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_18)	44600700h
BF4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_18)	00000064h
C00h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_19)	44000300h
C04h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_19)	00000065h

20.2.1 Family Base Address (FAMBAR) - Offset 8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 8h	00000300h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0300h RO	**Family Base Address (FAMBAR):** This field provides the starting byte-align address of Family0 register sets within a Community. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

20.2.2 Pad Base Address (PADBAR) - Offset Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + Ch	00000700h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0700h RO	**Pad Base Address (PADBAR):** This field provides the starting byte-align address of Pad0 register sets within a Community. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

20.2.3 Miscellaneous Configuration (MISCCFG) - Offset 10h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 10h	33043200h

Bit Range	Default & Access	Field Name (ID): Description
31:24	33h RW	**GPIO Driver Mode Interrupt Select (GPDMINTSEL):** IRQ globally for all pads (GPI_IS with corresponding GPI_IE enable). 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255
23:20	0h RO	**Reserved**
19:16	4h RO	**Reserved**
15:12	3h RW	**GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The setting is processor specific.

Bit Range	Default & Access	Field Name (ID): Description
11:8	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[:0]. The setting is processor specific.
7	0h RW	**GPIO IOSF Sideband VNNREQ Enable (GPVNNREQEN):** Specify whether the GPIO Community should take part in IOSFSB VNNREQ/ACK handshake 0 = Disable participation in IOSF SB VNNREQ and VNNACK handshake 1 = Enable participation in IOSF SB VNNREQ and VNNACK handshake When this bit set to 1, GPIO controller will de-assert the VNNREQ when there is no outstanding IOSF SB upstream cycle from GPIO controller. When this bit set to 1 and MISCSECCFG.SBTRIGDIS is 0, GPIO controller will assert the VNNREQ to request for the following list of IOSF-SB Message initiation. Event list: IRQ NMI SMI SSMI Fuse/Soft strap pull VNNREQ shall de-assert when MISCSECCFG.SBTRIGDIS is set to 1. As VNNAON IP, GPIO controller will assert the VNNREQ when in reset. The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pwrgate_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this power gating, this register always default to 1.
6	0h RW	**GPIO PGCB Clock Dynamic Partition Clock Gating Enable (GPPGCBDPCGEN):** Specify whether the GPIO Community PGCB clock should take part in partition clock gating 0 = Disable participation in PGCB clock dynamic partition clock gating 1 = Enable participation in PGCB clock dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
5	0h RW	**GPIO IOSF Sideband Dynamic Partition Clock Gating Enable (GPSIDEDPCGEN):** Specify whether the GPIO Community IOSF sideband clock should take part in partition clock gating 0 = Disable participation in IOSF sideband clock dynamic partition clock gating 1 = Enable participation in IOSF sideband clock dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
4	0h RW	**GPIO RCOMP clock Dynamic Local Clock Gating (GPRCOMPCDLCGEN):** Specify whether the GPIO Community should perform local clock gating on RCOMP clock 0 = Disable dynamic RCOMP clock local clock gating 1 = Enable dynamic RCOMP clock local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GPIO RTC clock Dynamic Local Clock Gating (GPRTCDLCGEN):** Specify whether the GPIO Community should perform local clock gating on RTC clock 0 = Disable dynamic RTC clock local clock gating 1 = Enable dynamic RTC clock local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
2	0h RO	**Reserved**
1	0h RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN):** Specify whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
0	0h RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN):** Specify whether the GPIO Community should perform local clock gating 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0

20.2.4 Pad Ownership (PAD_OWN_GPP_V_0) - Offset 20h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_V_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_V_6):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_V_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_V_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_V_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_V_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_V_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_V_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.2.5 Pad Ownership (PAD_OWN_GPP_V_1) - Offset 24h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 24h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_V_15):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_V_14):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_V_13):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_V_12):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_V_11):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_V_10):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_V_9):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_V_8):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.2.6 Pad Ownership (PAD_OWN_GPP_H_0) - Offset 28h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 28h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_6):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.2.7 Pad Ownership (PAD_OWN_GPP_H_1) - Offset 2Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_15):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_14):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_13):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_12):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_11):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_10):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_9):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_8):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.2.8 Pad Ownership (PAD_OWN_GPP_H_2) - Offset 30h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_23):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_22):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_21):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_20):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_19):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_18):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_17):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_16):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.2.9 Pad Ownership (PAD_OWN_GPP_D_0) - Offset 34h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_6):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.2.10 Pad Ownership (PAD_OWN_GPP_D_1) - Offset 38h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_15):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_14):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_13):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_12):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_11):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_10):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_9):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_8):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.2.11 Pad Ownership (PAD_OWN_GPP_D_2) - Offset 3Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RO	**Reserved**
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_19):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_18):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_17):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_16):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.2.12 Pad Ownership (PAD_OWN_GPP_U_0) - Offset 40h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_U_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_U_6):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_U_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_U_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_U_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_U_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_U_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_U_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.2.13 Pad Ownership (PAD_OWN_GPP_U_1) - Offset 44h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 44h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_U_15):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_U_14):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_U_13):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_U_12):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_U_11):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_U_10):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_U_9):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_U_8):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.2.14 Pad Ownership (PAD_OWN_GPP_U_2) - Offset 48h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RO	**Reserved**
27:26	0h RO	**Reserved**
25:24	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
23:22	0h RO	**Reserved**
21:20	0h RO	**Reserved**
19:18	0h RO	**Reserved**
17:16	0h RO	**Reserved**
15:14	0h RO	**Reserved**
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_U_19):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_U_18):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_U_17):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_U_16):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.2.15 Pad Configuration Lock (PADCFGLOCK_GPP_V_0) - Offset 80h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_V_15):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_V_14):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_V_13):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_V_12):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_V_11):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_V_10):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_V_9):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_V_8):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_V_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_V_6):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_V_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_V_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_V_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_V_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_V_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_V_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

20.2.16 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_V_0) - Offset 84h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_V_15):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_V_14):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_V_13):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_V_12):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_V_11):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_V_10):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_V_9):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_V_8):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_V_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_V_6):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_V_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_V_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_V_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_V_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_V_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_V_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

20.2.17 Pad Configuration Lock (PADCFGLOCK_GPP_H_0) - Offset 88h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_23):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
22	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_22):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_21):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
20	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_20):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_19):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
18	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_18):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_17):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
16	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_16):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_15):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_14):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_13):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_12):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_11):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_10):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_9):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_8):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_6):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

20.2.18 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_H_0) - Offset 8Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 8Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_23):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
22	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_22):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_21):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
20	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_20):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_19):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
18	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_18):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_17):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
16	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_16):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_15):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_14):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_13):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_12):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_11):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_10):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_9):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_8):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_6):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

20.2.19 Pad Configuration Lock (PADCFGLOCK_GPP_D_0) - Offset 90h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_19):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
18	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_18):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_17):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
16	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_16):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_15):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_14):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_13):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_12):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_11):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_10):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_9):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_8):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_6):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

20.2.20 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_D_0) - Offset 94h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_19):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
18	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_18):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_17):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
16	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_16):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_15):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_14):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_13):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_12):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_11):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_10):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_9):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_8):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_6):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

20.2.21 Pad Configuration Lock (PADCFGLOCK_GPP_U_0) - Offset 98h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**Reserved**
22	0h RO	**Reserved**
21	0h RO	**Reserved**
20	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_U_19):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
18	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_U_18):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_U_17):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
16	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_U_16):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_U_15):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_U_14):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_U_13):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_U_12):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_U_11):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_U_10):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_U_9):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_U_8):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_U_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_U_6):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_U_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_U_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_U_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_U_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_U_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_U_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

20.2.22 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_U_0) - Offset 9Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**Reserved**
22	0h RO	**Reserved**
21	0h RO	**Reserved**
20	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_U_19):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
18	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_U_18):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_U_17):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
16	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_U_16):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_U_15):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_U_14):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_U_13):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_U_12):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_U_11):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_U_10):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_U_9):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_U_8):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_U_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_U_6):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_U_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_U_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_U_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_U_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_U_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_U_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

20.2.23 Host Software Pad Ownership (HOSTSW_OWN_GPP_V_0) - Offset B0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**HOSTSW_OWN_GPPC_V_15:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
14	0h RW	**HOSTSW_OWN_GPPC_V_14:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
13	0h RW	**HOSTSW_OWN_GPPC_V_13:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**HOSTSW_OWN_GPPC_V_12:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
11	0h RW	**HOSTSW_OWN_GPPC_V_11:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
10	0h RW	**HOSTSW_OWN_GPPC_V_10:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**HOSTSW_OWN_GPPC_V_9:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
8	0h RW	**HOSTSW_OWN_GPPC_V_8:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
7	0h RW	**HOSTSW_OWN_GPPC_V_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**HOSTSW_OWN_GPPC_V_6:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
5	0h RW	**HOSTSW_OWN_GPPC_V_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
4	0h RW	**HOSTSW_OWN_GPPC_V_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**HOSTSW_OWN_GPPC_V_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPPC_V_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPPC_V_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPPC_V_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

20.2.24 Host Software Pad Ownership (HOSTSW_OWN_GPP_H_0) - Offset B4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**HOSTSW_OWN_GPPC_H_23:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
22	0h RW	**HOSTSW_OWN_GPPC_H_22:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**HOSTSW_OWN_GPPC_H_21:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
20	0h RW	**HOSTSW_OWN_GPPC_H_20:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
19	0h RW	**HOSTSW_OWN_GPPC_H_19:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**HOSTSW_OWN_GPPC_H_18:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
17	0h RW	**HOSTSW_OWN_GPPC_H_17:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
16	0h RW	**HOSTSW_OWN_GPPC_H_16:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**HOSTSW_OWN_GPPC_H_15:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
14	0h RW	**HOSTSW_OWN_GPPC_H_14:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
13	0h RW	**HOSTSW_OWN_GPPC_H_13:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**HOSTSW_OWN_GPPC_H_12:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
11	0h RW	**HOSTSW_OWN_GPPC_H_11:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
10	0h RW	**HOSTSW_OWN_GPPC_H_10:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**HOSTSW_OWN_GPPC_H_9:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
8	0h RW	**HOSTSW_OWN_GPPC_H_8:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
7	0h RW	**HOSTSW_OWN_GPPC_H_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**HOSTSW_OWN_GPPC_H_6:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
5	0h RW	**HOSTSW_OWN_GPPC_H_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
4	0h RW	**HOSTSW_OWN_GPPC_H_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**HOSTSW_OWN_GPPC_H_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPPC_H_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPPC_H_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPPC_H_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

20.2.25 Host Software Pad Ownership (HOSTSW_OWN_GPP_D_0) - Offset B8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RW	**HOSTSW_OWN_GPPC_D_19:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
18	0h RW	**HOSTSW_OWN_GPPC_D_18:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**HOSTSW_OWN_GPPC_D_17:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
16	0h RW	**HOSTSW_OWN_GPPC_D_16:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
15	0h RW	**HOSTSW_OWN_GPPC_D_15:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**HOSTSW_OWN_GPPC_D_14:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
13	0h RW	**HOSTSW_OWN_GPPC_D_13:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
12	0h RW	**HOSTSW_OWN_GPPC_D_12:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**HOSTSW_OWN_GPPC_D_11:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
10	0h RW	**HOSTSW_OWN_GPPC_D_10:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
9	0h RW	**HOSTSW_OWN_GPPC_D_9:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**HOSTSW_OWN_GPPC_D_8:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
7	0h RW	**HOSTSW_OWN_GPPC_D_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
6	0h RW	**HOSTSW_OWN_GPPC_D_6:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**HOSTSW_OWN_GPPC_D_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
4	0h RW	**HOSTSW_OWN_GPPC_D_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
3	0h RW	**HOSTSW_OWN_GPPC_D_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPPC_D_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPPC_D_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPPC_D_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

20.2.26 Host Software Pad Ownership (HOSTSW_OWN_GPP_U_0) - Offset BCh

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**Reserved**
22	0h RO	**Reserved**
21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RW	**HOSTSW_OWN_GPPC_U_19:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
18	0h RW	**HOSTSW_OWN_GPPC_U_18:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**HOSTSW_OWN_GPPC_U_17:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
16	0h RW	**HOSTSW_OWN_GPPC_U_16:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
15	0h RW	**HOSTSW_OWN_GPPC_U_15:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**HOSTSW_OWN_GPPC_U_14:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
13	0h RW	**HOSTSW_OWN_GPPC_U_13:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
12	0h RW	**HOSTSW_OWN_GPPC_U_12:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**HOSTSW_OWN_GPPC_U_11:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
10	0h RW	**HOSTSW_OWN_GPPC_U_10:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
9	0h RW	**HOSTSW_OWN_GPPC_U_9:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**HOSTSW_OWN_GPPC_U_8:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
7	0h RW	**HOSTSW_OWN_GPPC_U_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
6	0h RW	**HOSTSW_OWN_GPPC_U_6:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**HOSTSW_OWN_GPPC_U_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
4	0h RW	**HOSTSW_OWN_GPPC_U_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
3	0h RW	**HOSTSW_OWN_GPPC_U_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPPC_U_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPPC_U_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPPC_U_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

20.2.27 GPI Interrupt Status (GPI_IS_GPP_V_0) - Offset 100h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 100h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_V_15):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_V_14):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_V_13):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_V_12):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_V_11):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_V_10):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_V_9):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_V_8):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_V_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_V_6):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_V_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_V_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_V_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_V_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_V_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_V_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.2.28 GPI Interrupt Status (GPI_IS_GPP_H_0) - Offset 104h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 104h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_23):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_22):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
21	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_21):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_20):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
19	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_19):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_18):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_17):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
16	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_16):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_15):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_14):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_13):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_12):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_11):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_10):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_9):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_8):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_6):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.2.29 GPI Interrupt Status (GPI_IS_GPP_D_0) - Offset 108h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 108h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_19):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_18):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
17	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_17):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_16):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_15):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_14):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_13):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_12):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_11):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_10):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_9):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_8):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_6):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.2.30 GPI Interrupt Status (GPI_IS_GPP_U_0) - Offset 10Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 10Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**Reserved**
22	0h RO	**Reserved**
21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_U_19):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_U_18):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_U_17):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
16	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_U_16):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_U_15):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_U_14):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_U_13):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_U_12):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_U_11):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_U_10):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_U_9):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_U_8):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_U_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_U_6):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_U_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_U_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_U_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_U_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_U_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_U_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.2.31 GPI Interrupt Enable (GPI_IE_GPP_V_0) - Offset 120h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 120h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_V_15):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_V_14):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_V_13):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_V_12):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_V_11):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_V_10):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_V_9):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_V_8):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_V_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_V_6):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_V_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_V_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_V_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_V_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_V_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_V_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.2.32 GPI Interrupt Enable (GPI_IE_GPP_H_0) - Offset 124h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 124h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_23):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_22):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
21	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_21):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_20):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
19	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_19):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_18):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
17	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_17):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_16):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_15):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_14):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_13):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_12):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_11):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_10):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_9):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_8):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_6):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.2.33 GPI Interrupt Enable (GPI_IE_GPP_D_0) - Offset 128h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 128h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_19):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_18):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
17	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_17):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
16	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_16):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_15):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_14):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_13):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_12):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_11):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_10):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_9):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_8):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_6):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.2.34 GPI Interrupt Enable (GPI_IE_GPP_U_0) - Offset 12Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 12Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**Reserved**
22	0h RO	**Reserved**
21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_U_19):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_U_18):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
17	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_U_17):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_U_16):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_U_15):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_U_14):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_U_13):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_U_12):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_U_11):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_U_10):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_U_9):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_U_8):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_U_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_U_6):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_U_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_U_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_U_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_U_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_U_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_U_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.2.35 GPI General Purpose Events Status (GPI_GPE_STS_GPP_V_0) - Offset 140h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 140h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_V_15):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_V_14):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_V_13):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_V_12):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_V_11):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_V_10):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_V_9):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_V_8):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_V_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_V_6):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_V_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_V_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_V_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_V_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_V_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_V_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.2.36 GPI General Purpose Events Status (GPI_GPE_STS_GPP_H_0) - Offset 144h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 144h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_23):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_22):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_21):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
20	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_20):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
19	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_19):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_18):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
17	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_17):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_16):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_15):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_14):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_13):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_12):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_11):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_10):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_9):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_8):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_6):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.2.37 GPI General Purpose Events Status (GPI_GPE_STS_GPP_D_0) - Offset 148h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 148h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_19):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
18	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_18):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_17):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_16):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
15	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_15):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_14):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_13):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
12	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_12):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_11):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_10):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
9	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_9):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_8):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_6):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.2.38 GPI General Purpose Events Status (GPI_GPE_STS_GPP_U_0) - Offset 14Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 14Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**Reserved**
22	0h RO	**Reserved**
21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_U_19):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
18	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_U_18):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_U_17):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_U_16):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
15	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_U_15):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_U_14):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_U_13):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
12	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_U_12):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_U_11):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_U_10):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
9	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_U_9):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_U_8):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_U_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_U_6):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_U_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_U_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_U_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_U_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_U_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_U_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.2.39 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_V_0) - Offset 160h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 160h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_V_15):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_V_14):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_V_13):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_V_12):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_V_11):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_V_10):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_V_9):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_V_8):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_V_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_V_6):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_V_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_V_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_V_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_V_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_V_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_V_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.2.40 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_H_0) - Offset 164h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 164h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_23):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_22):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
21	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_21):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_20):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
19	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_19):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
18	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_18):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_17):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_16):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_15):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_14):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_13):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_12):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_11):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_10):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_9):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_8):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_6):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.2.41 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_D_0) - Offset 168h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 168h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_19):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
18	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_18):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_17):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_16):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_15):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_14):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_13):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_12):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_11):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_10):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_9):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_8):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_6):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.2.42 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_U_0) - Offset 16Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 16Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**Reserved**
22	0h RO	**Reserved**
21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_U_19):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
18	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_U_18):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
17	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_U_17):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_U_16):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_U_15):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_U_14):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_U_13):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_U_12):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_U_11):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_U_10):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_U_9):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_U_8):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_U_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_U_6):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_U_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_U_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_U_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_U_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_U_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_U_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.2.43 SMI Status (GPI_SMI_STS_GPP_V_0) - Offset 180h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 180h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_V_15):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
14	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_V_14):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_V_13):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
12	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_V_12):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_V_11):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
10	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_V_10):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_V_9):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
8	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_V_8):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_V_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
6	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_V_6):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_V_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
4	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_V_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_V_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_V_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_V_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_V_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

20.2.44 SMI Status (GPI_SMI_STS_GPP_H_0) - Offset 184h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 184h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_23):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
22	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_22):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_21):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
20	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_20):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_19):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
18	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_18):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_17):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
16	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_16):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_15):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
14	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_14):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_13):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
12	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_12):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_11):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
10	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_10):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_9):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
8	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_8):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
6	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_6):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
4	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

20.2.45 SMI Status (GPI_SMI_STS_GPP_D_0) - Offset 188h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 188h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_19):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
18	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_18):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_17):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
16	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_16):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_15):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
14	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_14):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_13):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
12	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_12):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_11):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
10	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_10):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_9):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
8	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_8):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
6	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_6):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
4	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_D_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_D_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_D_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_D_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_D_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

20.2.46 SMI Status (GPI_SMI_STS_GPP_U_0) - Offset 18Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 18Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RSV	**Reserved**
22	0h RSV	**Reserved**
21	0h RSV	**Reserved**
20	0h RSV	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
19	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_U_19):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
18	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_U_18):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_U_17):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
16	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_U_16):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_U_15):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
14	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_U_14):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_U_13):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
12	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_U_12):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_U_11):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
10	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_U_10):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_U_9):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
8	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_U_8):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_U_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
6	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_U_6):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_U_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
4	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_U_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_U_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_U_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_U_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_U_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

20.2.47 SMI Enable (GPI_SMI_EN_GPP_V_0) - Offset 1A0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_V_15):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
14	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_V_14):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
13	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_V_13):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_V_12):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
11	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_V_11):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
10	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_V_10):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_V_9):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
8	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_V_8):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
7	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_V_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_V_6):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
5	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_V_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
4	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_V_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_V_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_V_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_V_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_V_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

20.2.48 SMI Enable (GPI_SMI_EN_GPP_H_0) - Offset 1A4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_23):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
22	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_22):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
21	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_21):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
20	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_20):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
19	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_19):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
18	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_18):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
17	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_17):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
16	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_16):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_15):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
14	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_14):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
13	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_13):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_12):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
11	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_11):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
10	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_10):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_9):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
8	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_8):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
7	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_6):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
5	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
4	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

20.2.49 SMI Enable (GPI_SMI_EN_GPP_D_0) - Offset 1A8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_19):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
18	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_18):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_17):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
16	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_16):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
15	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_15):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_14):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
13	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_13):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
12	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_12):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_11):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
10	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_10):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
9	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_9):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_8):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
7	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
6	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_6):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
4	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
3	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

20.2.50 SMI Enable (GPI_SMI_EN_GPP_U_0) - Offset 1ACh

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RSV	**Reserved**
22	0h RSV	**Reserved**
21	0h RSV	**Reserved**
20	0h RSV	**Reserved**
19	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_U_19):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
18	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_U_18):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_U_17):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
16	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_U_16):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
15	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_U_15):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_U_14):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
13	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_U_13):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
12	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_U_12):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_U_11):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
10	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_U_10):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
9	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_U_9):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_U_8):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
7	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_U_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
6	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_U_6):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_U_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
4	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_U_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
3	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_U_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_U_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_U_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_U_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

20.2.51 NMI Status (GPI_NMI_STS_GPP_V_0) - Offset 1C0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_V_15):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_V_14):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_V_13):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
12	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_V_12):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_V_11):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_V_10):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
9	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_V_9):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_V_8):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_V_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_V_6):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_V_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_V_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_V_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_V_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_V_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_V_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.2.52 NMI Status (GPI_NMI_STS_GPP_H_0) - Offset 1C4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_23):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_22):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_21):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
20	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_20):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
19	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_19):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_18):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
17	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_17):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_16):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_15):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_14):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_13):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_12):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_11):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_10):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_9):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_8):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_6):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.2.53 NMI Status (GPI_NMI_STS_GPP_D_0) - Offset 1C8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_19):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
18	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_18):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_17):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_16):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
15	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_15):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_14):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_13):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
12	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_12):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_11):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_10):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
9	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_9):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_8):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_6):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_D_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_D_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_D_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_D_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_D_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.2.54 NMI Status (GPI_NMI_STS_GPP_U_0) - Offset 1CCh

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RSV	**Reserved**
22	0h RSV	**Reserved**
21	0h RSV	**Reserved**
20	0h RSV	**Reserved**
19	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_U_19):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
18	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_U_18):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_U_17):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_U_16):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
15	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_U_15):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_U_14):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_U_13):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
12	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_U_12):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_U_11):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_U_10):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
9	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_U_9):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_U_8):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_U_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_U_6):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_U_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_U_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_U_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_U_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_U_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_U_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.2.55 NMI Enable (GPI_NMI_EN_GPP_V_0) - Offset 1E0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_V_15):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_V_14):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_V_13):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
12	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_V_12):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_V_11):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_V_10):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
9	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_V_9):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_V_8):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_V_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_V_6):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_V_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_V_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_V_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_V_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_V_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_V_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.2.56 NMI Enable (GPI_NMI_EN_GPP_H_0) - Offset 1E4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_23):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_22):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
21	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_21):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_20):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
19	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_19):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
18	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_18):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_17):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_16):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
15	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_15):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_14):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_13):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
12	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_12):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_11):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_10):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
9	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_9):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_8):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_6):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.2.57 NMI Enable (GPI_NMI_EN_GPP_D_0) - Offset 1E8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_19):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
18	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_18):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
17	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_17):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_16):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
15	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_15):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_14):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_13):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
12	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_12):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_11):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_10):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
9	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_9):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_8):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_6):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.2.58 NMI Enable (GPI_NMI_EN_GPP_U_0) - Offset 1ECh

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RSV	**Reserved**
22	0h RSV	**Reserved**
21	0h RSV	**Reserved**
20	0h RSV	**Reserved**
19	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_U_19):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
18	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_U_18):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_U_17):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_U_16):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
15	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_U_15):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_U_14):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_U_13):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
12	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_U_12):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_U_11):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_U_10):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
9	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_U_9):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_U_8):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_U_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_U_6):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_U_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_U_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_U_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_U_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_U_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_U_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.2.59 PWM Control (PWMC) - Offset 204h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 204h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
	0h RW	**EN:** 0 = Disable PWM Output 1 = Enable PWM Output
30	0h RW/1S/V	**Software Update (SWUP):** Indication that there is an update to PWM settings pending. SW sets this bit to 1 when updating the PWM_base_unit or PWM_on_time_divisor fields. The PWM module will apply the new settings at the end of the current cycle and reset this bit. 0 = No updates pending 1 = Update pending
29:8	000000h RW	**Base Unit (BASEUNIT):** Base unit register. Unsigned 8 integer bits, 14 fraction bits. Used to determine PWM output frequency. The PWM base frequency for SPT is 32.768 KHz. Refer to PWM section for programming details.
7:0	00h RW	**On Time Divisor (ONTIMEDIV):** PWM duty cycle = PWM_on-time_divisor/256.

20.2.60 GPIO Serial Blink Enable (GP_SER_BLINK) - Offset 20Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 20Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RW	**GP SER BLINK (GP_SER_BLINK):** The setting of this bit has no effect if the corresponding GPIO is programmed as an input, if the corresponding GPIO has the PWM enabled, or if Serial Blink capability does not exist . This bit should be set to a 1 before output buffer is enabled. When set to a '0', the corresponding GPIO will function normally. This bit should be set to a 1 while the corresponding PMode bit is set to 0h (GPIO Mode). Setting the PMode bit to other value (non-GPIO Mode) after the GP_SER_BLINK bit ensures PCH will not drive a 1 on the pin as an output. When this corresponding bit is set to a 1 and the pin is configured to output mode, the serial blink capability is enabled and the programmed message is serialized out through an open-drain buffer configuration. The value of the corresponding GPIOTxState bit remains unchanged and does not impact the serial blink capability in any way. Writes to this register have no effect when the corresponding pin is configured in native mode and the read value returned is undefined. Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= Pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

20.2.61 GPIO Serial Blink Command/Status (GP_SER_CMDSTS) - Offset 210h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 210h	00080000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:22	0h RW	**Data Length Select (DLS):** This read/write field determines the number of bytes to serialize on GPIO 00: Serialize bits 7:0 of GP_GB_DATA (1 byte) 01: Serialize bits 15:0 of GP_GB_DATA (2 bytes) 10: Undefined - Software must not write this value 11: Serialize bits :0 of GP_GB_DATA (4 bytes) Software should not modify the value in this register unless the Busy bit is clear
21:16	08h RW	**Data Rate Select (DRS):** This read/write field selects the number of 166.64ns (4 clock periods GPIO clock - if GPIO clock is 24MHz) time intervals to count between Manchester data transitions. The default of 8h results in a 1333.33 ns minimum time between transitions. A value of 0h in this register produces undefined behavior. Software should not modify the value in this register unless the Busy bit is clear.
15:9	0h RO	**Reserved**
8	0h RO/V	**BUSY:** This read-only status bit is the hardware indication that a serialization is in progress. Hardware sets this bit to 1 based on the Go bit being set. Hardware clears this bit when the Go bit is cleared by the hardware.
7:1	0h RO	**Reserved**
0	0h RW	**GO:** This bit is set to 1 by software to start the serialization process. Hardware clears the bit after the serialized data is sent. Writes of 0 to this register have no effect. Software should not write this bit to 1 unless the Busy status bit is cleared.

20.2.62 GPIO Serial Blink Data (GP_SER_DATA) - Offset 214h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 214h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GP Serial Blink Data (GP_GB_DATA):** This read-write register contains the data serialized out. The number of bits shifted out is selected through the DLS field in the GP_GB_CMDSTS register. This register should not be modified by software when the Busy bit is set.

20.2.63 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_0) - Offset 700h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 700h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally

Bit Range	Default & Access	Field Name (ID): Description
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.

Bit Range	Default & Access	Field Name (ID): Description
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.64 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_0) - Offset 704h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 704h	0000002Ch

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	2Ch RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.65 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_1) - Offset 710h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 710h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.66 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_1) - Offset 714h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 714h	0000002Dh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	2Dh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.67 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_2) - Offset 720h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 720h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.68 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_2) - Offset 724h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 724h	0000002Eh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	2Eh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.69 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_3) - Offset 730h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 730h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.70 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_3) - Offset 734h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 734h	0000002Fh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	2Fh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.71 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_4) - Offset 740h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 740h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.72 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_4) - Offset 744h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 744h	00000030h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	30h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.73 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_5) - Offset 750h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 750h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.74 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_5) - Offset 754h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 754h	000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.75 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_6) - Offset 760h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 760h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.76 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_6) - Offset 764h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 764h	00000032h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	32h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.77 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_7) - Offset 770h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 770h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.78 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_7) - Offset 774h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 774h	00000033h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	33h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.79 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_8) - Offset 780h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 780h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.80 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_8) - Offset 784h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 784h	00000034h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	34h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.81 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_9) - Offset 790h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 790h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.82 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_9) - Offset 794h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 794h	00000035h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	35h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.83 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_10) - Offset 7A0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 7A0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.84 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_10) - Offset 7A4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 7A4h	00000036h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	36h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.85 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_11) - Offset 7B0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 7B0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.86 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_11) - Offset 7B4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 7B4h	00000037h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	37h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.87 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_12) - Offset 7C0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 7C0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.88 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_12) - Offset 7C4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 7C4h	00000038h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	38h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.89 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_13) - Offset 7D0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 7D0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.90 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_13) - Offset 7D4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 7D4h	00000039h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	39h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.91 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_14) - Offset 7E0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 7E0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.92 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_14) - Offset 7E4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 7E4h	0000003Ah

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	3Ah RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.93 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_V_15) - Offset 7F0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 7F0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.94 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_V_15) - Offset 7F4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 7F4h	0000003Bh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	3Bh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.95 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_0) - Offset 800h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 800h	44000200h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.96 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_0) - Offset 804h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 804h	0000003Ch

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	3Ch RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.97 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_1) - Offset 810h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 810h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.98 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_1) - Offset 814h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 814h	0000003Dh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	3Dh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.99 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_2) - Offset 820h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 820h	44000200h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.100 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_2) - Offset 824h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 824h	0000003Eh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	3Eh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.101 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_3) - Offset 830h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 830h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.102 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_3) - Offset 834h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 834h	0000003Fh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	3Fh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.103 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_4) - Offset 840h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 840h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.104 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_4) - Offset 844h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 844h	00000040h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	40h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.105 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_5) - Offset 850h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 850h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.106 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_5) - Offset 854h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 854h	00000041h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	41h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.107 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_6) - Offset 860h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 860h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.108 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_6) - Offset 864h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 864h	00000042h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	42h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.109 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_7) - Offset 870h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 870h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.110 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_7) - Offset 874h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 874h	00000043h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	43h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.111 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_8) - Offset 880h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 880h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.112 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_8) - Offset 884h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 884h	00000044h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	44h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.113 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_9) - Offset 890h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 890h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.114 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_9) - Offset 894h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 894h	00000045h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	45h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.115 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_10) - Offset 8A0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 8A0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.116 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_10) - Offset 8A4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 8A4h	00000046h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	46h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.117 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_11) - Offset 8B0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 8B0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.118 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_11) - Offset 8B4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 8B4h	00000047h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	47h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.119 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_12) - Offset 8C0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 8C0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.120 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_12) - Offset 8C4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 8C4h	00000048h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	48h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.121 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_13) - Offset 8D0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 8D0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.122 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_13) - Offset 8D4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 8D4h	00000049h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	49h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.123 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_14) - Offset 8E0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 8E0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.124 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_14) - Offset 8E4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 8E4h	0000004Ah

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	4Ah RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.125 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_15) - Offset 8F0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 8F0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.126 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_15) - Offset 8F4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 8F4h	0000004Bh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	4Bh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.127 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_16) - Offset 900h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 900h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.128 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_16) - Offset 904h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 904h	0000004Ch

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	4Ch RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.129 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_17) - Offset 910h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 910h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.130 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_17) - Offset 914h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 914h	0000004Dh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	4Dh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.131 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_18) - Offset 920h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 920h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.132 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_18) - Offset 924h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 924h	0000004Eh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	4Eh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.133 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_19) - Offset 930h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 930h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.134 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_19) - Offset 934h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 934h	0000004Fh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	4Fh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.135 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_20) - Offset 940h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 940h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.136 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_20) - Offset 944h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 944h	00000050h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	50h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.137 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_21) - Offset 950h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 950h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.138 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_21) - Offset 954h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 954h	00000051h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	51h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.139 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_22) - Offset 960h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 960h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.140 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_22) - Offset 964h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 964h	00000052h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	52h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.141 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_23) - Offset 970h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 970h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.142 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_23) - Offset 974h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 974h	00000053h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	53h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.143 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_0) - Offset 980h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 980h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.144 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_0) - Offset 984h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 984h	00000054h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	54h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.145 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_1) - Offset 990h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 990h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.146 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_1) - Offset 994h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 994h	0000006Eh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	6Eh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.147 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_2) - Offset 9A0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 9A0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.148 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_2) - Offset 9A4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 9A4h	0000006Fh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	6Fh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.149 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_3) - Offset 9B0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 9B0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.150 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_3) - Offset 9B4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 9B4h	00000070h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	70h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.151 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_4) - Offset 9C0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 9C0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.152 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_4) - Offset 9C4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 9C4h	00000071h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	71h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.153 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_5) - Offset 9D0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 9D0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.154 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_5) - Offset 9D4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 9D4h	00000072h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	72h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.155 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_6) - Offset 9E0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 9E0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.156 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_6) - Offset 9E4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 9E4h	00000073h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	73h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.157 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_7) - Offset 9F0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 9F0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.158 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_7) - Offset 9F4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 9F4h	00000074h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	74h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.159 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_8) - Offset A00h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + A00h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.160 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_8) - Offset A04h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + A04h	00000075h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	75h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.161 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_9) - Offset A10h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + A10h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.162 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_9) - Offset A14h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + A14h	00000076h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	76h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.163 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_10) - Offset A20h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + A20h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.164 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_10) - Offset A24h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + A24h	00000077h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	77h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.165 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_11) - Offset A30h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + A30h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.166 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_11) - Offset A34h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + A34h	00000018h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	18h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.167 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_12) - Offset A40h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + A40h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.168 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_12) - Offset A44h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + A44h	00000019h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	19h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.169 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_13) - Offset A50h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + A50h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.170 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_13) - Offset A54h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + A54h	0000001Ah

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	1Ah RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.171 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_14) - Offset A60h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + A60h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.172 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_14) - Offset A64h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + A64h	0000001Bh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	1Bh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.173 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_15) - Offset A70h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + A70h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.174 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_15) - Offset A74h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + A74h	0000001Ch

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	1Ch RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.175 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_16) - Offset A80h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + A80h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.176 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_16) - Offset A84h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + A84h	0000001Dh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	1Dh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.177 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_17) - Offset A90h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + A90h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.178 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_17) - Offset A94h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + A94h	0000001Eh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	1Eh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.179 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_18) - Offset AA0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + AA0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.180 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_18) - Offset AA4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + AA4h	0000001Fh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	1Fh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.181 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_19) - Offset AB0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + AB0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.182 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_19) - Offset AB4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + AB4h	00000020h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	20h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.183 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_0) - Offset AD0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + AD0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.184 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_0) - Offset AD4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + AD4h	00000022h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	22h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.185 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_1) - Offset AE0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + AE0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.186 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_1) - Offset AE4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + AE4h	00000023h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	23h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.187 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_2) - Offset AF0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + AF0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.188 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_2) - Offset AF4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + AF4h	00000024h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	24h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.189 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_3) - Offset B00h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B00h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.190 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_3) - Offset B04h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B04h	00000025h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	25h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.191 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_4) - Offset B10h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B10h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.192 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_4) - Offset B14h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B14h	00000056h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	56h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.193 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_5) - Offset B20h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B20h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.194 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_5) - Offset B24h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B24h	00000057h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	57h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.195 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_6) - Offset B30h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B30h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.196 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_6) - Offset B34h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B34h	00000058h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	58h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.197 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_7) - Offset B40h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B40h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.198 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_7) - Offset B44h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B44h	00000059h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	59h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.199 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_8) - Offset B50h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B50h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.200 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_8) - Offset B54h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B54h	0000005Ah

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	5Ah RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.201 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_9) - Offset B60h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B60h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.202 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_9) - Offset B64h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B64h	0000005Bh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	5Bh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.203 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_10) - Offset B70h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B70h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.204 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_10) - Offset B74h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B74h	0000005Ch

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	5Ch RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.205 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_11) - Offset B80h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B80h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.206 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_11) - Offset B84h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B84h	0000005Dh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	5Dh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.207 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_12) - Offset B90h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B90h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.208 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_12) - Offset B94h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B94h	0000105Eh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	4h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	5Eh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.209 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_13) - Offset BA0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + BA0h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.210 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_13) - Offset BA4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + BA4h	0000105Fh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	4h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	5Fh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.211 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_14) - Offset BB0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + BB0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.212 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_14) - Offset BB4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + BB4h	00000060h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	60h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.213 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_15) - Offset BC0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + BC0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.214 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_15) - Offset BC4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + BC4h	00000061h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	61h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.215 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_16) - Offset BD0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + BD0h	44600700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	3h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.216 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_16) - Offset BD4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + BD4h	00000062h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	62h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.217 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_17) - Offset BE0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + BE0h	44600700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	3h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.218 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_17) - Offset BE4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + BE4h	00000063h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	63h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.219 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_18) - Offset BF0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + BF0h	44600700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	3h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.220 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_18) - Offset BF4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + BF4h	00000064h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	64h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.2.221 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_19) - Offset C00h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + C00h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.2.222 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_19) - Offset C04h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + C04h	00000065h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	65h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.3 GPIO Community 2 Registers Summary

This chapter documents GPIO 2 Registers.

Table 20-3. Summary of GPIO 2 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8h	4	Family Base Address (FAMBAR)	00000300h
Ch	4	Pad Base Address (PADBAR)	00000700h
10h	4	Miscellaneous Configuration (MISCCFG)	34043200h
20h	4	Pad Ownership (PAD_OWN_DSW_0)	00000000h
24h	4	Pad Ownership (PAD_OWN_DSW_1)	00000000h
80h	4	Pad Configuration Lock (PADCFGLOCK_DSW_0)	00000000h
84h	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_DSW_0)	00000000h
B0h	4	Host Software Pad Ownership (HOSTSW_OWN_DSW_0)	00000000h
100h	4	GPI Interrupt Status (GPI_IS_DSW_0)	00000000h
120h	4	GPI Interrupt Enable (GPI_IE_DSW_0)	00000000h
140h	4	GPI General Purpose Events Status (GPI_GPE_STS_DSW_0)	00000000h
160h	4	GPI General Purpose Events Enable (GPI_GPE_EN_DSW_0)	00000000h
180h	4	SMI Status (GPI_SMI_STS_DSW_0)	00000000h
1A0h	4	SMI Enable (GPI_SMI_EN_DSW_0)	00000000h
1C0h	4	NMI Status (GPI_NMI_STS_DSW_0)	00000000h
1E0h	4	NMI Enable (GPI_NMI_EN_DSW_0)	00000000h
250h	4	Event Trigger Output Enable (EVOUTEN_0)	00000000h
260h	8	Event Trigger Mapping (EVMAP_0)	0000000000000000h
700h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_0)	04000700h
704h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_0)	00003021h
710h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_1)	04000700h
714h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_1)	00003C22h
720h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_2)	04000700h
724h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_2)	00003C23h
730h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_3)	04000700h
734h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_3)	00003024h
740h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_4)	04000600h
744h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_4)	00000025h
750h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_5)	04000600h
754h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_5)	00000026h
770h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_7)	04000200h
774h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_7)	00000028h
780h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_8)	04000700h
784h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_8)	00000029h
790h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_9)	04000600h
794h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_9)	0000002Ah
7A0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_10)	04000600h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
7A4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_10)	0000002Bh
7B0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_11)	04000600h
7B4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_11)	0000006Bh

20.3.1 Family Base Address (FAMBAR) - Offset 8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 8h	00000300h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0300h RO	**Family Base Address (FAMBAR):** This field provides the starting byte-align address of Family0 register sets within a Community. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

20.3.2 Pad Base Address (PADBAR) - Offset Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + Ch	00000700h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0700h RO	**Pad Base Address (PADBAR):** This field provides the starting byte-align address of Pad0 register sets within a Community. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

20.3.3 Miscellaneous Configuration (MISCCFG) - Offset 10h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 10h	34043200h

Bit Range	Default & Access	Field Name (ID): Description
31:24	34h RW	**GPIO Driver Mode Interrupt Select (GPDMINTSEL):** IRQ globally for all pads (GPI_IS with corresponding GPI_IE enable). 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255
23:20	0h RO	**Reserved**
19:16	4h RO	**Reserved**
15:12	3h RW	**GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The setting is processor specific.
11:8	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[:0]. The setting is processor specific.
7	0h RW	**GPIO IOSF Sideband VNNREQ Enable (GPVNNREQEN):** Specify whether the GPIO Community should take part in IOSFSB VNNREQ/ACK handshake 0 = Disable participation in IOSF SB VNNREQ and VNNACK handshake 1 = Enable participation in IOSF SB VNNREQ and VNNACK handshake When this bit set to 1, GPIO controller will de-assert the VNNREQ when there is no outstanding IOSF SB upstream cycle from GPIO controller. When this bit set to 1 and MISCSECCFG.SBTRIGDIS is 0, GPIO controller will assert the VNNREQ to request for the following list of IOSF-SB Message initiation. Event list: IRQ NMI SMI SSMI Fuse/Soft strap pull VNNREQ shall de-assert when MISCSECCFG.SBTRIGDIS is set to 1. As VNNAON IP, GPIO controller will assert the VNNREQ when in reset. The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pwrgate_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this power gating, this register always default to 1.
6	0h RW	**GPIO PGCB Clock Dynamic Partition Clock Gating Enable (GPPGCBDPCGEN):** Specify whether the GPIO Community PGCB clock should take part in partition clock gating 0 = Disable participation in PGCB clock dynamic partition clock gating 1 = Enable participation in PGCB clock dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**GPIO IOSF Sideband Dynamic Partition Clock Gating Enable (GPSIDEDPCGEN):** Specify whether the GPIO Community IOSF sideband clock should take part in partition clock gating 0 = Disable participation in IOSF sideband clock dynamic partition clock gating 1 = Enable participation in IOSF sideband clock dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
4	0h RW	**GPIO RCOMP clock Dynamic Local Clock Gating (GPRCOMPCDLCGEN):** Specify whether the GPIO Community should perform local clock gating on RCOMP clock 0 = Disable dynamic RCOMP clock local clock gating 1 = Enable dynamic RCOMP clock local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
3	0h RW	**GPIO RTC clock Dynamic Local Clock Gating (GPRTCDLCGEN):** Specify whether the GPIO Community should perform local clock gating on RTC clock 0 = Disable dynamic RTC clock local clock gating 1 = Enable dynamic RTC clock local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
2	0h RO	**Reserved**
1	0h RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN):** Specify whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
0	0h RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN):** Specify whether the GPIO Community should perform local clock gating 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0

20.3.4 Pad Ownership (PAD_OWN_DSW_0) - Offset 20h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPD_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**
25:24	0h RO	**Reserved**
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPD_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPD_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPD_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPD_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPD_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPD_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.3.5 Pad Ownership (PAD_OWN_DSW_1) - Offset 24h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 24h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RO	**Reserved**
27:26	0h RO	**Reserved**
25:24	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
23:22	0h RO	**Reserved**
21:20	0h RO	**Reserved**
19:18	0h RO	**Reserved**
17:16	0h RO	**Reserved**
15:14	0h RO	**Reserved**
13:12	0h RW	**Pad Ownership (PAD_OWN_GPD_11):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPD_10):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPD_9):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPD_8):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.3.6 Pad Configuration Lock (PADCFGLOCK_DSW_0) - Offset 80h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RO	**Reserved**
15	0h RO	**Reserved**
14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**Reserved**
12	0h RO	**Reserved**
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_11):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_10):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_9):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_8):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
6	0h RO	**Reserved**
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

20.3.7 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_DSW_0) - Offset 84h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RO	**Reserved**
15	0h RO	**Reserved**
14	0h RO	**Reserved**
13	0h RO	**Reserved**
12	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_11):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_10):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_9):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_8):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
6	0h RO	**Reserved**
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

20.3.8 Host Software Pad Ownership (HOSTSW_OWN_DSW_0) - Offset B0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RO	**Reserved**
15	0h RO	**Reserved**
14	0h RO	**Reserved**
13	0h RO	**Reserved**
12	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**HOSTSW_OWN_GPD_11:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
10	0h RW	**HOSTSW_OWN_GPD_10:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
9	0h RW	**HOSTSW_OWN_GPD_9:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**HOSTSW_OWN_GPD_8:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
7	0h RW	**HOSTSW_OWN_GPD_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
6	0h RO	**Reserved**
5	0h RW	**HOSTSW_OWN_GPD_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**HOSTSW_OWN_GPD_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
3	0h RW	**HOSTSW_OWN_GPD_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPD_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPD_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPD_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

20.3.9 GPI Interrupt Status (GPI_IS_DSW_0) - Offset 100h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 100h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RO	**Reserved**
15	0h RO	**Reserved**
14	0h RO	**Reserved**
13	0h RO	**Reserved**
12	0h RO	**Reserved**
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_11):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_10):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_9):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_8):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.3.10 GPI Interrupt Enable (GPI_IE_DSW_0) - Offset 120h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 120h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RO	**Reserved**
15	0h RO	**Reserved**
14	0h RO	**Reserved**
13	0h RO	**Reserved**
12	0h RO	**Reserved**
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_11):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_10):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_9):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_8):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RO	**Reserved**
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.3.11 GPI General Purpose Events Status (GPI_GPE_STS_DSW_0) - Offset 140h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 140h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RO	**Reserved**
15	0h RO	**Reserved**
14	0h RO	**Reserved**
13	0h RO	**Reserved**
12	0h RO	**Reserved**
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_11):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_10):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_9):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_8):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.3.12 GPI General Purpose Events Enable (GPI_GPE_EN_DSW_0) - Offset 160h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 160h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RO	**Reserved**
15	0h RO	**Reserved**
14	0h RO	**Reserved**
13	0h RO	**Reserved**
12	0h RO	**Reserved**
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_11):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_10):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_9):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_8):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.3.13 SMI Status (GPI_SMI_STS_DSW_0) - Offset 180h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 180h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RO	**Reserved**
15	0h RO	**Reserved**
14	0h RO	**Reserved**
13	0h RO	**Reserved**
12	0h RO	**Reserved**
11	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_11):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
10	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_10):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_9):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
8	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_8):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
6	0h RO	**Reserved**
5	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
3	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

20.3.14 SMI Enable (GPI_SMI_EN_DSW_0) - Offset 1A0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 1A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RO	**Reserved**
15	0h RO	**Reserved**
14	0h RO	**Reserved**
13	0h RO	**Reserved**
12	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
11	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_11):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
10	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_10):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
9	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_9):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_8):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
7	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
6	0h RO	**Reserved**
5	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
3	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

20.3.15 NMI Status (GPI_NMI_STS_DSW_0) - Offset 1C0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 1C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RO	**Reserved**
15	0h RO	**Reserved**
14	0h RO	**Reserved**
13	0h RO	**Reserved**
12	0h RO	**Reserved**
11	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_11):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_10):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_9):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_8):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.3.16 NMI Enable (GPI_NMI_EN_DSW_0) - Offset 1E0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 1E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RO	**Reserved**
15	0h RO	**Reserved**
14	0h RO	**Reserved**
13	0h RO	**Reserved**
12	0h RO	**Reserved**
11	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_11):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_10):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_9):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_8):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.3.17 Event Trigger Output Enable (EVOUTEN_0) - Offset 250h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 250h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**EV Trigger Output Enable (EVOUTEN):** When a bit is '0', the corresponding output is masked to '0' I.e. no valid pin assigned to. When a bit is set to '1' the corresponding output is enabled and depends on the EVMAP settings.

20.3.18 Event Trigger Mapping (EVMAP_0) - Offset 260h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	64 bit	FD6C0000h + 260h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:61	0h RO	**Reserved**
60	0h RW	**Event Trigger Mapping to PMU[15] (EVMAPPM_15):** 000b = GPIOevent trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
59:57	0h RO	**Reserved**
56	0h RW	**Event Trigger Mapping to PMU[14] (EVMAPPM_14):** 000b = GPIOevent trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
55:53	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
52	0h RW	**Event Trigger Mapping to PMU[13] (EVMAPPM_13):** 000b = GPIOevent trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
51:49	0h RO	**Reserved**
48	0h RW	**Event Trigger Mapping to PMU[12] (EVMAPPM_12):** 000b = GPIOevent trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
47:45	0h RO	**Reserved**
44	0h RW	**Event Trigger Mapping to PMU[11] (EVMAPPM_11):** 000b = GPIOevent trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
43:41	0h RO	**Reserved**
40	0h RW	**Event Trigger Mapping to PMU[10] (EVMAPPM_10):** 000b = GPIOevent trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
39:37	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
36	0h RW	**Event Trigger Mapping to PMU[9] (EVMAPPM_9):** 000b = GPIOevent trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
35:33	0h RO	**Reserved**
32	0h RW	**Event Trigger Mapping to PMU[8] (EVMAPPM_8):** 000b = GPIOevent trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
31:29	0h RO	**Reserved**
28	0h RW	**Event Trigger Mapping to PMU[7] (EVMAPPM_7):** 000b = GPIOevent trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
27:25	0h RO	**Reserved**
24	0h RW	**Event Trigger Mapping to PMU[6] (EVMAPPM_6):** 000b = GPIOevent trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
23:21	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**Event Trigger Mapping to PMU[5] (EVMAPPM_5):** 000b = GPIOevent trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
19:17	0h RO	**Reserved**
16	0h RW	**Event Trigger Mapping to PMU[4] (EVMAPPM_4):** 000b = GPIOevent trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
15:13	0h RO	**Reserved**
12	0h RW	**Event Trigger Mapping to PMU[3] (EVMAPPM_3):** 000b = GPIOevent trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
11:9	0h RO	**Reserved**
8	0h RW	**Event Trigger Mapping to PMU[2] (EVMAPPM_2):** 000b = GPIOevent trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
7:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Event Trigger Mapping to PMU[1] (EVMAPPM_1):** 000b = GPIOevent trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
3:1	0h RO	**Reserved**
0	0h RW	**Event Trigger Mapping to PMU[0] (EVMAPPM_0):** 000b = GPIOevent trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community

20.3.19 Pad Configuration DW0 (PAD_CFG_DW0_GPD_0) - Offset 700h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 700h	04000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RO/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.3.20 Pad Configuration DW1 (PAD_CFG_DW1_GPD_0) - Offset 704h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 704h	00003021h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RO	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Ch RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RO	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	21h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.3.21 Pad Configuration DW0 (PAD_CFG_DW0_GPD_1) - Offset 710h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 710h	04000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.3.22 Pad Configuration DW1 (PAD_CFG_DW1_GPD_1) - Offset 714h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 714h	00003C22h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RO	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Fh RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RO	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	22h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.3.23 Pad Configuration DW0 (PAD_CFG_DW0_GPD_2) - Offset 720h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 720h	04000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.3.24 Pad Configuration DW1 (PAD_CFG_DW1_GPD_2) - Offset 724h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 724h	00003C23h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RO	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Fh RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RO	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	23h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.3.25 Pad Configuration DW0 (PAD_CFG_DW0_GPD_3) - Offset 730h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 730h	04000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.3.26 Pad Configuration DW1 (PAD_CFG_DW1_GPD_3) - Offset 734h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 734h	00003024h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
17:14	0h RO	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Ch RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RO	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	24h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.3.27 Pad Configuration DW0 (PAD_CFG_DW0_GPD_4) - Offset 740h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 740h	04000600h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RO/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.3.28 Pad Configuration DW1 (PAD_CFG_DW1_GPD_4) - Offset 744h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 744h	00000025h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RO	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RO	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	25h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.3.29 Pad Configuration DW0 (PAD_CFG_DW0_GPD_5) - Offset 750h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 750h	04000600h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RO/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.3.30 Pad Configuration DW1 (PAD_CFG_DW1_GPD_5) - Offset 754h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 754h	00000026h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RO	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RO	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	26h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.3.31 Pad Configuration DW0 (PAD_CFG_DW0_GPD_7) - Offset 770h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 770h	04000200h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RO	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.3.32 Pad Configuration DW1 (PAD_CFG_DW1_GPD_7) - Offset 774h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 774h	00000028h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RO	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RO	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	28h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.3.33 Pad Configuration DW0 (PAD_CFG_DW0_GPD_8) - Offset 780h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 780h	04000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.3.34 Pad Configuration DW1 (PAD_CFG_DW1_GPD_8) - Offset 784h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 784h	00000029h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RO	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RO	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	29h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.3.35 Pad Configuration DW0 (PAD_CFG_DW0_GPD_9) - Offset 790h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 790h	04000600h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RO/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.3.36 Pad Configuration DW1 (PAD_CFG_DW1_GPD_9) - Offset 794h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 794h	0000002Ah

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RO	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RO	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	2Ah RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.3.37 Pad Configuration DW0 (PAD_CFG_DW0_GPD_10) - Offset 7A0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 7A0h	04000600h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RO/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.3.38 Pad Configuration DW1 (PAD_CFG_DW1_GPD_10) - Offset 7A4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 7A4h	0000002Bh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RO	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RO	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	2Bh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.3.39 Pad Configuration DW0 (PAD_CFG_DW0_GPD_11) - Offset 7B0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 7B0h	04000600h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RO/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.3.40 Pad Configuration DW1 (PAD_CFG_DW1_GPD_11) - Offset 7B4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 7B4h	0000006Bh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RO	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RO	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	6Bh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4 GPIO Community 3 Registers Summary

This chapter documents GPIO 3 Registers.

Table 20-4. Summary of GPIO 3 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8h	4	Family Base Address (FAMBAR)	00000300h
Ch	4	Pad Base Address (PADBAR)	00000700h
10h	4	Miscellaneous Configuration (MISCCFG)	35043200h
2Ch	4	Pad Ownership (PAD_OWN_GPP_S_0)	00000000h
30h	4	Pad Ownership (PAD_OWN_GPP_A_0)	00000000h
34h	4	Pad Ownership (PAD_OWN_GPP_A_1)	00000000h
38h	4	Pad Ownership (PAD_OWN_GPP_A_2)	00000000h
3Ch	4	Pad Ownership (PAD_OWN_VGPIO_3_0)	00000000h
88h	4	Pad Configuration Lock (PADCFGLOCK_GPP_S_0)	00000000h
8Ch	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_S_0)	00000000h
90h	4	Pad Configuration Lock (PADCFGLOCK_GPP_A_0)	00000000h
94h	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_A_0)	00000000h
98h	4	Pad Configuration Lock (PADCFGLOCK_VGPIO_3_0)	00000000h
9Ch	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_VGPIO_3_0)	00000000h
B4h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_S_0)	00000000h
B8h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_A_0)	00000000h
BCh	4	Host Software Pad Ownership (HOSTSW_OWN_VGPIO_3_0)	00000000h
104h	4	GPI Interrupt Status (GPI_IS_GPP_S_0)	00000000h
108h	4	GPI Interrupt Status (GPI_IS_GPP_A_0)	00000000h
10Ch	4	GPI Interrupt Status (GPI_IS_VGPIO_3_0)	00000000h
124h	4	GPI Interrupt Enable (GPI_IE_GPP_S_0)	00000000h
128h	4	GPI Interrupt Enable (GPI_IE_GPP_A_0)	00000000h
12Ch	4	GPI Interrupt Enable (GPI_IE_VGPIO_3_0)	00000000h
144h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_S_0)	00000000h
148h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_0)	00000000h
14Ch	4	GPI General Purpose Events Status (GPI_GPE_STS_VGPIO_3_0)	00000000h
164h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_S_0)	00000000h
168h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_0)	00000000h
16Ch	4	GPI General Purpose Events Enable (GPI_GPE_EN_VGPIO_3_0)	00000000h
184h	4	SMI Status (GPI_SMI_STS_GPP_S_0)	00000000h
188h	4	SMI Status (GPI_SMI_STS_GPP_A_0)	00000000h
18Ch	4	SMI Status (GPI_SMI_STS_VGPIO_3_0)	00000000h
1A4h	4	SMI Enable (GPI_SMI_EN_GPP_S_0)	00000000h
1A8h	4	SMI Enable (GPI_SMI_EN_GPP_A_0)	00000000h
1ACh	4	SMI Enable (GPI_SMI_EN_VGPIO_3_0)	00000000h
1C4h	4	NMI Status (GPI_NMI_STS_GPP_S_0)	00000000h
1C8h	4	NMI Status (GPI_NMI_STS_GPP_A_0)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1CCh	4	NMI Status (GPI_NMI_STS_VGPIO_3_0)	00000000h
1E4h	4	NMI Enable (GPI_NMI_EN_GPP_S_0)	00000000h
1E8h	4	NMI Enable (GPI_NMI_EN_GPP_A_0)	00000000h
1ECh	4	NMI Enable (GPI_NMI_EN_VGPIO_3_0)	00000000h
810h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_0)	40000700h
814h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_0)	00001000h
820h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_1)	40000700h
824h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_1)	00001000h
830h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_0)	44000300h
834h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_0)	00000040h
840h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_1)	44000300h
844h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_1)	00000041h
850h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_2)	44000300h
854h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_2)	00000042h
860h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_3)	44000300h
864h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_3)	00000043h
870h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_4)	44000300h
874h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_4)	00000044h
880h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_5)	44000300h
884h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_5)	00000045h
890h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_6)	44000300h
894h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_6)	00000046h
8A0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_7)	44000300h
8A4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_7)	00000047h
8B0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_8)	44000300h
8B4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_8)	00000048h
8C0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_9)	44000300h
8C4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_9)	00000049h
8D0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_10)	44000300h
8D4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_10)	0000004Ah
8E0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_11)	44000300h
8E4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_11)	0000004Bh
8F0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_12)	44000300h
8F4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_12)	0000004Ch
900h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_13)	44000300h
904h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_13)	0000004Dh
910h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_14)	44000300h
914h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_14)	0000004Eh
920h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_15)	44000300h
924h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_15)	0000004Fh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
930h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_16)	44000300h
934h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_16)	00000050h
940h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_17)	44000300h
944h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_17)	00000051h
950h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_18)	44000300h
954h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_18)	00000052h
960h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_19)	44000300h
964h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_19)	00000053h
970h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_20)	44000300h
974h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_20)	00000054h
980h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_21)	44000300h
984h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_21)	00000055h
990h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_22)	44000300h
994h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_22)	00000056h
9A0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_23)	44000300h
9A4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_23)	00000057h
9B0h	4	Pad Configuration DW0 (PAD_CFG_DW0_VGPIO_USB_0)	40000400h
9B4h	4	Pad Configuration DW1 (PAD_CFG_DW1_VGPIO_USB_0)	00000000h
9C0h	4	Pad Configuration DW0 (PAD_CFG_DW0_VGPIO_USB_1)	40000400h
9C4h	4	Pad Configuration DW1 (PAD_CFG_DW1_VGPIO_USB_1)	00000000h
9D0h	4	Pad Configuration DW0 (PAD_CFG_DW0_VGPIO_USB_2)	40000400h
9D4h	4	Pad Configuration DW1 (PAD_CFG_DW1_VGPIO_USB_2)	00000000h
9E0h	4	Pad Configuration DW0 (PAD_CFG_DW0_VGPIO_USB_3)	40000400h
9E4h	4	Pad Configuration DW1 (PAD_CFG_DW1_VGPIO_USB_3)	00000000h

20.4.1 Family Base Address (FAMBAR) - Offset 8h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 8h	00000300h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0300h RO	**Family Base Address (FAMBAR):** This field provides the starting byte-align address of Family0 register sets within a Community. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

20.4.2 Pad Base Address (PADBAR) - Offset Ch

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + Ch	00000700h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0700h RO	**Pad Base Address (PADBAR):** This field provides the starting byte-align address of Pad0 register sets within a Community. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

20.4.3 Miscellaneous Configuration (MISCCFG) - Offset 10h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 10h	35043200h

Bit Range	Default & Access	Field Name (ID): Description
31:24	35h RW	**GPIO Driver Mode Interrupt Select (GPDMINTSEL):** IRQ globally for all pads (GPI_IS with corresponding GPI_IE enable). 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255
23:20	0h RO	**Reserved**
19:16	4h RW	**Reserved**
15:12	3h RW	**GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The setting is processor specific.
11:8	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[:0]. The setting is processor specific.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**GPIO IOSF Sideband VNNREQ Enable (GPVNNREQEN):** Specify whether the GPIO Community should take part in IOSFSB VNNREQ/ACK handshake 0 = Disable participation in IOSF SB VNNREQ and VNNACK handshake 1 = Enable participation in IOSF SB VNNREQ and VNNACK handshake When this bit set to 1, GPIO controller will de-assert the VNNREQ when there is no outstanding IOSF SB upstream cycle from GPIO controller. When this bit set to 1 and MISCSECCFG.SBTRIGDIS is 0, GPIO controller will assert the VNNREQ to request for the following list of IOSF-SB Message initiation. Event list: IRQ NMI SMI SSMI Fuse/Soft strap pull VNNREQ shall de-assert when MISCSECCFG.SBTRIGDIS is set to 1. As VNNAON IP, GPIO controller will assert the VNNREQ when in reset. The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pwrgate_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this power gating, this register always default to 1.
6	0h RW	**GPIO PGCB Clock Dynamic Partition Clock Gating Enable (GPPGCBDPCGEN):** Specify whether the GPIO Community PGCB clock should take part in partition clock gating 0 = Disable participation in PGCB clock dynamic partition clock gating 1 = Enable participation in PGCB clock dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
5	0h RW	**GPIO IOSF Sideband Dynamic Partition Clock Gating Enable (GPSIDEDPCGEN):** Specify whether the GPIO Community IOSF sideband clock should take part in partition clock gating 0 = Disable participation in IOSF sideband clock dynamic partition clock gating 1 = Enable participation in IOSF sideband clock dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
4	0h RW	**GPIO RCOMP clock Dynamic Local Clock Gating (GPRCOMPCDLCGEN):** Specify whether the GPIO Community should perform local clock gating on RCOMP clock 0 = Disable dynamic RCOMP clock local clock gating 1 = Enable dynamic RCOMP clock local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GPIO RTC clock Dynamic Local Clock Gating (GPRTCDLCGEN):** Specify whether the GPIO Community should perform local clock gating on RTC clock 0 = Disable dynamic RTC clock local clock gating 1 = Enable dynamic RTC clock local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
2	0h RO	Reserved
1	0h RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN):** Specify whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
0	0h RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN):** Specify whether the GPIO Community should perform local clock gating 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0

20.4.4 Pad Ownership (PAD_OWN_GPP_S_0) - Offset 2Ch

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**Pad Ownership (PAD_OWN_GPP_S_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RO	**Pad Ownership (PAD_OWN_GPP_S_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.4.5 Pad Ownership (PAD_OWN_GPP_A_0) - Offset 30h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_6):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.4.6 Pad Ownership (PAD_OWN_GPP_A_1) - Offset 34h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_15):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_14):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_13):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_12):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_11):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_10):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_9):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h. \
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_8):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.4.7 Pad Ownership (PAD_OWN_GPP_A_2) - Offset 38h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_23):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_22):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_21):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_20):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_19):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_18):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_17):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_16):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.4.8 Pad Ownership (PAD_OWN_VGPIO_3_0) - Offset 3Ch

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:12	0h RO	**Pad Ownership (PAD_OWN_VGPIO_USB_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RO	**Pad Ownership (PAD_OWN_VGPIO_USB_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**Pad Ownership (PAD_OWN_VGPIO_USB_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_VGPIO_USB_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.4.9 Pad Configuration Lock (PADCFGLOCK_GPP_S_0) - Offset 88h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RSV	**Pad Config Lock (PADCFGLOCK_GPP_S_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
0	0h RSV	**Pad Config Lock (PADCFGLOCK_GPP_S_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

20.4.10 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_S_0) - Offset 8Ch

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 8Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_S_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
0	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_S_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

20.4.11 Pad Configuration Lock (PADCFGLOCK_GPP_A_0) - Offset 90h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_23):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
22	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_22):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_21):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
20	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_20):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_19):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
18	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_18):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_17):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
16	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_16):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_15):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_14):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_13):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_12):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_11):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_10):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_9):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_8):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_6):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

20.4.12 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_A_0) - Offset 94h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_23):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
22	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_22):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_21):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
20	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_20):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_19):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
18	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_18):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_17):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
16	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_16):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_15):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_14):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_13):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_12):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_11):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_10):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_9):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_8):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_6):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

20.4.13 Pad Configuration Lock (PADCFGLOCK_VGPIO_3_0) - Offset 98h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RSV	**Pad Config Lock (PADCFGLOCK_VGPIO_USB_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**Pad Config Lock (PADCFGLOCK_VGPIO_USB_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
1	0h RSV	**Pad Config Lock (PADCFGLOCK_VGPIO_USB_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RSV	**Pad Config Lock (PADCFGLOCK_VGPIO_USB_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

20.4.14 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_VGPIO_3_0) - Offset 9Ch

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_VGPIO_USB_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_VGPIO_USB_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
1	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_VGPIO_USB_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_VGPIO_USB_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

20.4.15 Host Software Pad Ownership (HOSTSW_OWN_GPP_S_0) - Offset B4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RSV	**HOSTSW_OWN_GPP_S_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RSV	**HOSTSW_OWN_GPP_S_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

20.4.16 Host Software Pad Ownership (HOSTSW_OWN_GPP_A_0) - Offset B8h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**HOSTSW_OWN_GPPC_A_23:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
22	0h RW	**HOSTSW_OWN_GPPC_A_22:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
21	0h RW	**HOSTSW_OWN_GPPC_A_21:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**HOSTSW_OWN_GPPC_A_20:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
19	0h RW	**HOSTSW_OWN_GPPC_A_19:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
18	0h RW	**HOSTSW_OWN_GPPC_A_18:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**HOSTSW_OWN_GPPC_A_17:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
16	0h RW	**HOSTSW_OWN_GPPC_A_16:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
15	0h RW	**HOSTSW_OWN_GPPC_A_15:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**HOSTSW_OWN_GPPC_A_14:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
13	0h RW	**HOSTSW_OWN_GPPC_A_13:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
12	0h RW	**HOSTSW_OWN_GPPC_A_12:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**HOSTSW_OWN_GPPC_A_11:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
10	0h RW	**HOSTSW_OWN_GPPC_A_10:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
9	0h RW	**HOSTSW_OWN_GPPC_A_9:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**HOSTSW_OWN_GPPC_A_8:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
7	0h RW	**HOSTSW_OWN_GPPC_A_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
6	0h RW	**HOSTSW_OWN_GPPC_A_6:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**HOSTSW_OWN_GPPC_A_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
4	0h RW	**HOSTSW_OWN_GPPC_A_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
3	0h RW	**HOSTSW_OWN_GPPC_A_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPPC_A_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPPC_A_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPPC_A_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

20.4.17 Host Software Pad Ownership (HOSTSW_OWN_VGPIO_3_0) - Offset BCh

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RSV	**HOSTSW_OWN_VGPIO_USB_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**HOSTSW_OWN_VGPIO_USB_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RSV	**HOSTSW_OWN_VGPIO_USB_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RSV	**HOSTSW_OWN_VGPIO_USB_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

20.4.18 GPI Interrupt Status (GPI_IS_GPP_S_0) - Offset 104h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 104h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RSV	**GPI Interrupt Status (GPI_INT_STS_GPP_S_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RSV	**GPI Interrupt Status (GPI_INT_STS_GPP_S_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.4.19 GPI Interrupt Status (GPI_IS_GPP_A_0) - Offset 108h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 108h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_23):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_22):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
21	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_21):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_20):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
19	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_19):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_18):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_17):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
16	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_16):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_15):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_14):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_13):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_12):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_11):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_10):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_9):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_8):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_6):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.4.20 GPI Interrupt Status (GPI_IS_VGPIO_3_0) - Offset 10Ch

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 10Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RSV	**GPI Interrupt Status (GPI_INT_STS_VGPIO_USB_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI Interrupt Status (GPI_INT_STS_VGPIO_USB_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RSV	**GPI Interrupt Status (GPI_INT_STS_VGPIO_USB_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RSV	**GPI Interrupt Status (GPI_INT_STS_VGPIO_USB_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.4.21 GPI Interrupt Enable (GPI_IE_GPP_S_0) - Offset 124h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 124h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_GPP_S_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_GPP_S_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.4.22 GPI Interrupt Enable (GPI_IE_GPP_A_0) - Offset 128h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 128h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_23):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_22):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
21	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_21):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
20	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_20):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_19):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_18):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
17	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_17):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
16	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_16):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_15):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_14):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_13):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_12):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_11):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_10):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_9):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_8):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_6):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.4.23 GPI Interrupt Enable (GPI_IE_VGPIO_3_0) - Offset 12Ch

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 12Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_VGPIO_USB_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_VGPIO_USB_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_VGPIO_USB_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_VGPIO_USB_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.4.24 GPI General Purpose Events Status (GPI_GPE_STS_GPP_S_0) - Offset 144h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 144h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_S_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_S_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.4.25 GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_0) - Offset 148h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 148h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_23):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_22):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
21	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_21):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_20):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
19	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_19):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
18	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_18):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_17):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_16):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
15	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_15):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_14):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_13):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
12	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_12):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_11):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_10):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
9	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_9):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_8):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_6):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.4.26 GPI General Purpose Events Status (GPI_GPE_STS_VGPIO_3_0) - Offset 14Ch

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 14Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_VGPIO_USB_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_VGPIO_USB_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_VGPIO_USB_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_VGPIO_USB_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.4.27 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_S_0) - Offset 164h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 164h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_S_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_S_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.4.28 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_0) - Offset 168h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 168h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_23):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_22):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
21	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_21):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_20):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
19	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_19):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
18	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_18):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
17	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_17):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_16):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_15):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_14):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_13):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_12):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_11):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_10):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_9):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_8):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_6):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.4.29 GPI General Purpose Events Enable (GPI_GPE_EN_VGPIO_3_0) - Offset 16Ch

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 16Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_VGPIO_USB_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_VGPIO_USB_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_VGPIO_USB_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_VGPIO_USB_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.4.30 SMI Status (GPI_SMI_STS_GPP_S_0) - Offset 184h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 184h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_S_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
0	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_S_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

20.4.31 SMI Status (GPI_SMI_STS_GPP_A_0) - Offset 188h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 188h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_23):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
22	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_22):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_21):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
20	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_20):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_19):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
18	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_18):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_17):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
16	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_16):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_15):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
14	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_14):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_13):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
12	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_12):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_11):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
10	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_10):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_9):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
8	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_8):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
6	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_6):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
4	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

20.4.32 SMI Status (GPI_SMI_STS_VGPIO_3_0) - Offset 18Ch

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 18Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RSV	**GPI SMI Status (GPI_SMI_STS_VGPIO_USB_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Status (GPI_SMI_STS_VGPIO_USB_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RSV	**GPI SMI Status (GPI_SMI_STS_VGPIO_USB_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RSV	**GPI SMI Status (GPI_SMI_STS_VGPIO_USB_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

20.4.33 SMI Enable (GPI_SMI_EN_GPP_S_0) - Offset 1A4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 1A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_S_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_S_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

20.4.34 SMI Enable (GPI_SMI_EN_GPP_A_0) - Offset 1A8h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 1A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_23):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
22	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_22):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
21	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_21):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_20):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
19	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_19):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
18	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_18):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_17):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
16	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_16):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
15	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_15):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_14):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
13	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_13):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
12	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_12):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_11):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
10	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_10):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
9	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_9):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_8):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
7	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
6	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_6):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
4	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
3	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

20.4.35 SMI Enable (GPI_SMI_EN_VGPIO_3_0) - Offset 1ACh

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 1ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RSV	**GPI SMI Enable (GPI_SMI_EN_VGPIO_USB_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Enable (GPI_SMI_EN_VGPIO_USB_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RSV	**GPI SMI Enable (GPI_SMI_EN_VGPIO_USB_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RSV	**GPI SMI Enable (GPI_SMI_EN_VGPIO_USB_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

20.4.36 NMI Status (GPI_NMI_STS_GPP_S_0) - Offset 1C4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 1C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_S_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_S_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.4.37 NMI Status (GPI_NMI_STS_GPP_A_0) - Offset 1C8h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 1C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_23):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_22):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
21	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_21):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_20):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
19	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_19):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
18	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_18):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_17):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_16):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
15	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_15):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_14):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_13):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
12	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_12):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_11):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_10):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
9	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_9):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_8):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_6):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.4.38 NMI Status (GPI_NMI_STS_VGPIO_3_0) - Offset 1CCh

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 1CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RSV	**GPI NMI Status (GPI_NMI_STS_VGPIO_USB_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Status (GPI_NMI_STS_VGPIO_USB_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Status (GPI_NMI_STS_VGPIO_USB_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Status (GPI_NMI_STS_VGPIO_USB_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.4.39 NMI Enable (GPI_NMI_EN_GPP_S_0) - Offset 1E4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 1E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_S_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_S_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.4.40 NMI Enable (GPI_NMI_EN_GPP_A_0) - Offset 1E8h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 1E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_23):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_22):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
21	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_21):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_20):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
19	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_19):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
18	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_18):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_17):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_16):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
15	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_15):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_14):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_13):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
12	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_12):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_11):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_10):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
9	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_9):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_8):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_6):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.4.41 NMI Enable (GPI_NMI_EN_VGPIO_3_0) - Offset 1ECh

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 1ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RSV	**GPI NMI Enable (GPI_NMI_EN_VGPIO_USB_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Enable (GPI_NMI_EN_VGPIO_USB_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Enable (GPI_NMI_EN_VGPIO_USB_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Enable (GPI_NMI_EN_VGPIO_USB_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.4.42 Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_0) - Offset 810h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 810h	40000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	0h RO	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RO	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RO	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RO	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIO Own setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.43 Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_0) - Offset 814h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 814h	00001000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	4h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	00h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.44 Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_1) - Offset 820h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 820h	40000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	0h RO	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RO	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RO	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RO	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.45 Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_1) - Offset 824h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 824h	00001000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	4h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	00h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.46 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_0) - Offset 830h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 830h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.47 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_0) - Offset 834h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 834h	00000040h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	40h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.48 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_1) - Offset 840h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 840h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.49 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_1) - Offset 844h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 844h	00000041h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	41h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.50 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_2) - Offset 850h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 850h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.51 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_2) - Offset 854h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 854h	00000042h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	42h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.52 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_3) - Offset 860h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 860h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.53 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_3) - Offset 864h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 864h	00000043h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	43h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.54 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_4) - Offset 870h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 870h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.55 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_4) - Offset 874h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 874h	00000044h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	44h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.56 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_5) - Offset 880h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 880h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.57 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_5) - Offset 884h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 884h	00000045h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	45h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.58 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_6) - Offset 890h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 890h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.59 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_6) - Offset 894h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 894h	00000046h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	46h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.60 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_7) - Offset 8A0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 8A0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.61 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_7) - Offset 8A4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 8A4h	00000047h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	47h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.62 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_8) - Offset 8B0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 8B0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.63 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_8) - Offset 8B4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 8B4h	00000048h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	48h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.64 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_9) - Offset 8C0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 8C0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.65 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_9) - Offset 8C4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 8C4h	00000049h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	49h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.66 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_10) - Offset 8D0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 8D0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.67 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_10) - Offset 8D4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 8D4h	0000004Ah

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	4Ah RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.68 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_11) - Offset 8E0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 8E0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.69 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_11) - Offset 8E4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 8E4h	0000004Bh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behavior of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	4Bh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.70 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_12) - Offset 8F0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 8F0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.71 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_12) - Offset 8F4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 8F4h	0000004Ch

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	4Ch RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.72 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_13) - Offset 900h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 900h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.73 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_13) - Offset 904h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 904h	0000004Dh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	4Dh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.74 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_14) - Offset 910h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 910h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.75 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_14) - Offset 914h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 914h	0000004Eh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	4Eh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.76 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_15) - Offset 920h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 920h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.77 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_15) - Offset 924h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 924h	0000004Fh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	4Fh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.78 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_16) - Offset 930h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 930h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.79 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_16) - Offset 934h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 934h	00000050h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	50h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.80 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_17) - Offset 940h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 940h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.81 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_17) - Offset 944h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 944h	00000051h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	51h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.82 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_18) - Offset 950h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 950h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.83 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_18) - Offset 954h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 954h	00000052h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	52h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.84 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_19) - Offset 960h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 960h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.85 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_19) - Offset 964h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 964h	00000053h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	53h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.86 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_20) - Offset 970h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 970h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.87 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_20) - Offset 974h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 974h	00000054h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	54h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.88 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_21) - Offset 980h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 980h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.89 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_21) - Offset 984h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 984h	00000055h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	55h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.90 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_22) - Offset 990h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 990h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.91 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_22) - Offset 994h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 994h	00000056h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	56h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.92 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_23) - Offset 9A0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 9A0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.93 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_23) - Offset 9A4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 9A4h	00000057h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	57h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.94 Pad Configuration DW0 (PAD_CFG_DW0_VGPIO_USB_0) - Offset 9B0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 9B0h	40000400h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RO	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RO	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RO	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	0h RO	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RO	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RO	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RO	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RO	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	0h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.95 Pad Configuration DW1 (PAD_CFG_DW1_VGPIO_USB_0) - Offset 9B4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 9B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RO	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RO	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	00h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.96 Pad Configuration DW0 (PAD_CFG_DW0_VGPIO_USB_1) - Offset 9C0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 9C0h	40000400h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RO	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RO	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RO	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	0h RO	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RO	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RO	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RO	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RO	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	0h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.97 Pad Configuration DW1 (PAD_CFG_DW1_VGPIO_USB_1) - Offset 9C4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 9C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RO	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RO	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	00h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.98 Pad Configuration DW0 (PAD_CFG_DW0_VGPIO_USB_2) - Offset 9D0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 9D0h	40000400h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RO	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RO	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RO	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	0h RO	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RO	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RO	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RO	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RO	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	0h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.99 Pad Configuration DW1 (PAD_CFG_DW1_VGPIO_USB_2) - Offset 9D4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 9D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RO	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RO	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	00h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.4.100 Pad Configuration DW0 (PAD_CFG_DW0_VGPIO_USB_3) - Offset 9E0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 9E0h	40000400h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RO	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RO	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RO	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	0h RO	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RO	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RO	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RO	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RO	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	0h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.4.101 Pad Configuration DW1 (PAD_CFG_DW1_VGPIO_USB_3) - Offset 9E4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6B0000h + 9E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RO	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RO	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	00h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5 GPIO Community 4 Registers Summary

This chapter documents GPIO 4 Registers.

Table 20-5. Summary of GPIO 4 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8h	4	Family Base Address (FAMBAR)	00000300h
Ch	4	Pad Base Address (PADBAR)	00000700h
10h	4	Miscellaneous Configuration (MISCCFG)	36043200h
20h	4	Pad Ownership (PAD_OWN_GPP_C_0)	00000000h
24h	4	Pad Ownership (PAD_OWN_GPP_C_1)	00000000h
28h	4	Pad Ownership (PAD_OWN_GPP_C_2)	00000000h
2Ch	4	Pad Ownership (PAD_OWN_GPP_F_0)	00000000h
30h	4	Pad Ownership (PAD_OWN_GPP_F_1)	00000000h
34h	4	Pad Ownership (PAD_OWN_GPP_F_2)	00000000h
40h	4	Pad Ownership (PAD_OWN_GPP_E_0)	00000000h
44h	4	Pad Ownership (PAD_OWN_GPP_E_1)	00000000h
48h	4	Pad Ownership (PAD_OWN_GPP_E_2)	00000000h
80h	4	Pad Configuration Lock (PADCFGLOCK_GPP_C_0)	00000000h
84h	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_C_0)	00000000h
88h	4	Pad Configuration Lock (PADCFGLOCK_GPP_F_0)	00000000h
8Ch	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_F_0)	00000000h
98h	4	Pad Configuration Lock (PADCFGLOCK_GPP_E_0)	00000000h
9Ch	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_E_0)	00000000h
B0h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_C_0)	00000000h
B4h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_F_0)	00000000h
BCh	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_E_0)	00000000h
100h	4	GPI Interrupt Status (GPI_IS_GPP_C_0)	00000000h
104h	4	GPI Interrupt Status (GPI_IS_GPP_F_0)	00000000h
10Ch	4	GPI Interrupt Status (GPI_IS_GPP_E_0)	00000000h
120h	4	GPI Interrupt Enable (GPI_IE_GPP_C_0)	00000000h
124h	4	GPI Interrupt Enable (GPI_IE_GPP_F_0)	00000000h
12Ch	4	GPI Interrupt Enable (GPI_IE_GPP_E_0)	00000000h
140h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_0)	00000000h
144h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_0)	00000000h
14Ch	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_E_0)	00000000h
160h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_0)	00000000h
164h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_0)	00000000h
16Ch	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_E_0)	00000000h
180h	4	SMI Status (GPI_SMI_STS_GPP_C_0)	00000000h
184h	4	SMI Status (GPI_SMI_STS_GPP_F_0)	00000000h
18Ch	4	SMI Status (GPI_SMI_STS_GPP_E_0)	00000000h
1A0h	4	SMI Enable (GPI_SMI_EN_GPP_C_0)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1A4h	4	SMI Enable (GPI_SMI_EN_GPP_F_0)	00000000h
1ACh	4	SMI Enable (GPI_SMI_EN_GPP_E_0)	00000000h
1C0h	4	NMI Status (GPI_NMI_STS_GPP_C_0)	00000000h
1C4h	4	NMI Status (GPI_NMI_STS_GPP_F_0)	00000000h
1CCh	4	NMI Status (GPI_NMI_STS_GPP_E_0)	00000000h
1E0h	4	NMI Enable (GPI_NMI_EN_GPP_C_0)	00000000h
1E4h	4	NMI Enable (GPI_NMI_EN_GPP_F_0)	00000000h
1ECh	4	NMI Enable (GPI_NMI_EN_GPP_E_0)	00000000h
700h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_0)	44000700h
704h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_0)	0000006Eh
710h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_1)	44000700h
714h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_1)	0000006Fh
720h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_2)	44000200h
724h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_2)	00000070h
730h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_3)	44000300h
734h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_3)	00000071h
740h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_4)	44000300h
744h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_4)	00000072h
750h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_5)	44000200h
754h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_5)	00000073h
760h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_6)	44000300h
764h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_6)	00000074h
770h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_7)	44000300h
774h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_7)	00000075h
780h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_8)	44000B00h
784h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_8)	00001076h
790h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_9)	44000300h
794h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_9)	00000077h
7A0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_10)	44000300h
7A4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_10)	00000018h
7B0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_11)	44000300h
7B4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_11)	00000019h
7C0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_12)	44000300h
7C4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_12)	0000001Ah
7D0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_13)	44000300h
7D4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_13)	0000001Bh
7E0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_14)	44000300h
7E4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_14)	0000001Ch
7F0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_15)	44000300h
7F4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_15)	0000001Dh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
800h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_16)	44000300h
804h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_16)	0000001Eh
810h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_17)	44000300h
814h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_17)	0000001Fh
820h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_18)	44000300h
824h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_18)	00000020h
830h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_19)	44000300h
834h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_19)	00000021h
840h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_20)	44000300h
844h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_20)	00000022h
850h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_21)	44000300h
854h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_21)	00000023h
860h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_22)	44000300h
864h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_22)	00000024h
870h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_23)	44000300h
874h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_23)	00000025h
880h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_0)	44000700h
884h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_0)	00000056h
890h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_1)	44000700h
894h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_1)	00003057h
8A0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_2)	44000700h
8A4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_2)	00000058h
8B0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_3)	44000700h
8B4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_3)	00003059h
8C0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_4)	44000700h
8C4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_4)	0000005Ah
8D0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_5)	44000B00h
8D4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_5)	0000005Bh
8E0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_6)	44000300h
8E4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_6)	0000005Ch
8F0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_7)	44000200h
8F4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_7)	0000005Dh
900h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_8)	44001700h
904h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_8)	0000005Eh
910h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_9)	44000700h
914h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_9)	0000005Fh
920h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_10)	44000200h
924h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_10)	00000060h
930h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_11)	44001700h
934h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_11)	00000061h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
940h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_12)	44001700h
944h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_12)	00000062h
950h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_13)	44001700h
954h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_13)	00000063h
960h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_14)	44001700h
964h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_14)	00000064h
970h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_15)	44001700h
974h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_15)	00000065h
980h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_16)	44001700h
984h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_16)	00000066h
990h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_17)	44001700h
994h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_17)	00000067h
9A0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_18)	44000300h
9A4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_18)	00000068h
9B0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_19)	44000300h
9B4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_19)	00000069h
9C0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_20)	44000700h
9C4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_20)	0000006Ah
9D0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_21)	44000700h
9D4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_21)	0000006Bh
9E0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_22)	44000300h
9E4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_22)	0000006Ch
9F0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_23)	44000300h
9F4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_23)	0000006Dh
A70h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_0)	44001B00h
A74h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_0)	00000026h
A80h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_1)	44001B00h
A84h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_1)	00000027h
A90h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_2)	44001B00h
A94h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_2)	00000028h
AA0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_3)	44001B00h
AA4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_3)	00000029h
AB0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_4)	44001B00h
AB4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_4)	00000030h
AC0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_5)	44001B00h
AC4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_5)	000000h
AD0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_6)	44001A00h
AD4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_6)	00000032h
AE0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_7)	44001B00h
AE4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_7)	00000033h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
AF0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_8)	44001B00h
AF4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_8)	00000034h
B00h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_9)	44001B00h
B04h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_9)	00000035h
B10h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_10)	44001B00h
B14h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_10)	00000036h
B20h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_11)	44001B00h
B24h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_11)	00000037h
B30h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_12)	44001B00h
B34h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_12)	00000038h
B40h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_13)	44001B00h
B44h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_13)	00000039h
B50h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_14)	44001B00h
B54h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_14)	0000003Ah
B60h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_15)	44000B00h
B64h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_15)	0000003Bh
B70h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_16)	44000B00h
B74h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_16)	0000003Ch
B80h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_17)	44001B00h
B84h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_17)	0000003Dh
B90h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_18)	44001700h
B94h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_18)	00003C3Eh
BA0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_19)	44001600h
BA4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_19)	00003C3Fh
BB0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_20)	44000300h
BB4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_20)	00000040h
BC0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_21)	44000300h
BC4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_21)	00000041h
BD0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_22)	44000300h
BD4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_22)	00000042h
BE0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_23)	44000200h
BE4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_23)	00000043h

20.5.1 Family Base Address (FAMBAR) - Offset 8h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 8h	00000300h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0300h RO	**Family Base Address (FAMBAR):** This field provides the starting byte-align address of Family0 register sets within a Community. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

20.5.2 Pad Base Address (PADBAR) - Offset Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + Ch	00000700h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0700h RO	**Pad Base Address (PADBAR):** This field provides the starting byte-align address of Pad0 register sets within a Community. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

20.5.3 Miscellaneous Configuration (MISCCFG) - Offset 10h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 10h	36043200h

Bit Range	Default & Access	Field Name (ID): Description
31:24	36h RW	**GPIO Driver Mode Interrupt Select (GPDMINTSEL):** IRQ globally for all pads (GPI_IS with corresponding GPI_IE enable). 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255
23:20	0h RO	**Reserved**
19:16	4h RW	**Reserved**
15:12	3h RW	**GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The setting is processor specific.

Bit Range	Default & Access	Field Name (ID): Description
11:8	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[:0]. The setting is processor specific.
7	0h RW	**GPIO IOSF Sideband VNNREQ Enable (GPVNNREQEN):** Specify whether the GPIO Community should take part in IOSFSB VNNREQ/ACK handshake 0 = Disable participation in IOSF SB VNNREQ and VNNACK handshake 1 = Enable participation in IOSF SB VNNREQ and VNNACK handshake When this bit set to 1, GPIO controller will de-assert the VNNREQ when there is no outstanding IOSF SB upstream cycle from GPIO controller. When this bit set to 1 and MISCSECCFG.SBTRIGDIS is 0, GPIO controller will assert the VNNREQ to request for the following list of IOSF-SB Message initiation. Event list: IRQ NMI SMI SSMI Fuse/Soft strap pull VNNREQ shall de-assert when MISCSECCFG.SBTRIGDIS is set to 1. As VNNAON IP, GPIO controller will assert the VNNREQ when in reset. The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pwrgate_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this power gating, this register always default to 1.
6	0h RW	**GPIO PGCB Clock Dynamic Partition Clock Gating Enable (GPPGCBDPCGEN):** Specify whether the GPIO Community PGCB clock should take part in partition clock gating 0 = Disable participation in PGCB clock dynamic partition clock gating 1 = Enable participation in PGCB clock dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
5	0h RW	**GPIO IOSF Sideband Dynamic Partition Clock Gating Enable (GPSIDEDPCGEN):** Specify whether the GPIO Community IOSF sideband clock should take part in partition clock gating 0 = Disable participation in IOSF sideband clock dynamic partition clock gating 1 = Enable participation in IOSF sideband clock dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
4	0h RW	**GPIO RCOMP clock Dynamic Local Clock Gating (GPRCOMPCDLCGEN):** Specify whether the GPIO Community should perform local clock gating on RCOMP clock 0 = Disable dynamic RCOMP clock local clock gating 1 = Enable dynamic RCOMP clock local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GPIO RTC clock Dynamic Local Clock Gating (GPRTCDLCGEN):** Specify whether the GPIO Community should perform local clock gating on RTC clock 0 = Disable dynamic RTC clock local clock gating 1 = Enable dynamic RTC clock local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
2	0h RO	**Reserved**
1	0h RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN):** Specify whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
0	0h RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN):** Specify whether the GPIO Community should perform local clock gating 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0

20.5.4 Pad Ownership (PAD_OWN_GPP_C_0) - Offset 20h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_6):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.5.5 Pad Ownership (PAD_OWN_GPP_C_1) - Offset 24h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 24h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_15):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_14):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_13):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_12):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_11):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_10):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_9):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_8):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.5.6 Pad Ownership (PAD_OWN_GPP_C_2) - Offset 28h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 28h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_23):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_22):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_21):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_20):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_19):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_18):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_17):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_16):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.5.7 Pad Ownership (PAD_OWN_GPP_F_0) - Offset 2Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_6):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.5.8 Pad Ownership (PAD_OWN_GPP_F_1) - Offset 30h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_15):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_14):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_13):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_12):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_11):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_10):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_9):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_8):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.5.9 Pad Ownership (PAD_OWN_GPP_F_2) - Offset 34h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_23):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_22):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_21):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_20):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_19):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_18):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_17):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_16):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.5.10 Pad Ownership (PAD_OWN_GPP_E_0) - Offset 40h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_6):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.5.11 Pad Ownership (PAD_OWN_GPP_E_1) - Offset 44h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 44h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_15):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_14):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_13):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_12):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_11):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_10):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_9):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_8):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.5.12 Pad Ownership (PAD_OWN_GPP_E_2) - Offset 48h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_23):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_22):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_21):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_20):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_19):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_18):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_17):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_16):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.5.13 Pad Configuration Lock (PADCFGLOCK_GPP_C_0) - Offset 80h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_23):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
22	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_22):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_21):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
20	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_20):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_19):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
18	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_18):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_17):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
16	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_16):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_15):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_14):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_13):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_12):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_11):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_10):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_9):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_8):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_6):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

20.5.14 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_C_0) - Offset 84h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_23):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
22	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_22):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_21):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
20	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_20):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_19):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
18	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_18):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_17):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
16	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_16):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_15):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_14):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_13):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_12):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_11):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_10):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_9):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_8):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_6):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

20.5.15 Pad Configuration Lock (PADCFGLOCK_GPP_F_0) - Offset 88h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_23):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
22	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_22):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_21):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
20	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_20):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_19):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
18	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_18):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_17):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
16	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_16):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_15):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_14):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_13):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_12):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_11):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_10):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_9):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_8):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_6):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

20.5.16 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_F_0) - Offset 8Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 8Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_23):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
22	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_22):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_21):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
20	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_20):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_19):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
18	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_18):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_17):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
16	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_16):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_15):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_14):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_13):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_12):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_11):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_10):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_9):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_8):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_6):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

20.5.17 Pad Configuration Lock (PADCFGLOCK_GPP_E_0) - Offset 98h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_23):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
22	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_22):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_21):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
20	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_20):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_19):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
18	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_18):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_17):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
16	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_16):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_15):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_14):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_13):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_12):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_11):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_10):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_9):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_8):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_6):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

20.5.18 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_E_0) - Offset 9Ch

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_23):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
22	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_22):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_21):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
20	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_20):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_19):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
18	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_18):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_17):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
16	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_16):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_15):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_14):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_13):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_12):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_11):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_10):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_9):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_8):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_6):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

20.5.19 Host Software Pad Ownership (HOSTSW_OWN_GPP_C_0) - Offset B0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**HOSTSW_OWN_GPPC_C_23:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
22	0h RW	**HOSTSW_OWN_GPPC_C_22:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
21	0h RW	**HOSTSW_OWN_GPPC_C_21:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**HOSTSW_OWN_GPPC_C_20:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
19	0h RW	**HOSTSW_OWN_GPPC_C_19:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
18	0h RW	**HOSTSW_OWN_GPPC_C_18:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**HOSTSW_OWN_GPPC_C_17:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
16	0h RW	**HOSTSW_OWN_GPPC_C_16:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
15	0h RW	**HOSTSW_OWN_GPPC_C_15:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**HOSTSW_OWN_GPPC_C_14:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
13	0h RW	**HOSTSW_OWN_GPPC_C_13:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
12	0h RW	**HOSTSW_OWN_GPPC_C_12:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**HOSTSW_OWN_GPPC_C_11:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
10	0h RW	**HOSTSW_OWN_GPPC_C_10:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
9	0h RW	**HOSTSW_OWN_GPPC_C_9:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**HOSTSW_OWN_GPPC_C_8:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
7	0h RW	**HOSTSW_OWN_GPPC_C_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
6	0h RW	**HOSTSW_OWN_GPPC_C_6:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**HOSTSW_OWN_GPPC_C_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
4	0h RW	**HOSTSW_OWN_GPPC_C_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
3	0h RW	**HOSTSW_OWN_GPPC_C_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPPC_C_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPPC_C_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPPC_C_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

20.5.20 Host Software Pad Ownership (HOSTSW_OWN_GPP_F_0) - Offset B4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**HOSTSW_OWN_GPPC_F_23:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
22	0h RW	**HOSTSW_OWN_GPPC_F_22:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**HOSTSW_OWN_GPPC_F_21:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
20	0h RW	**HOSTSW_OWN_GPPC_F_20:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
19	0h RW	**HOSTSW_OWN_GPPC_F_19:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**HOSTSW_OWN_GPPC_F_18:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
17	0h RW	**HOSTSW_OWN_GPPC_F_17:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
16	0h RW	**HOSTSW_OWN_GPPC_F_16:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**HOSTSW_OWN_GPPC_F_15:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
14	0h RW	**HOSTSW_OWN_GPPC_F_14:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
13	0h RW	**HOSTSW_OWN_GPPC_F_13:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**HOSTSW_OWN_GPPC_F_12:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
11	0h RW	**HOSTSW_OWN_GPPC_F_11:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
10	0h RW	**HOSTSW_OWN_GPPC_F_10:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**HOSTSW_OWN_GPPC_F_9:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
8	0h RW	**HOSTSW_OWN_GPPC_F_8:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
7	0h RW	**HOSTSW_OWN_GPPC_F_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**HOSTSW_OWN_GPPC_F_6:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
5	0h RW	**HOSTSW_OWN_GPPC_F_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
4	0h RW	**HOSTSW_OWN_GPPC_F_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**HOSTSW_OWN_GPPC_F_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPPC_F_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPPC_F_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPPC_F_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

20.5.21 Host Software Pad Ownership (HOSTSW_OWN_GPP_E_0) - Offset BCh

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**HOSTSW_OWN_GPPC_E_23:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
22	0h RW	**HOSTSW_OWN_GPPC_E_22:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**HOSTSW_OWN_GPPC_E_21:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
20	0h RW	**HOSTSW_OWN_GPPC_E_20:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
19	0h RW	**HOSTSW_OWN_GPPC_E_19:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**HOSTSW_OWN_GPPC_E_18:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
17	0h RW	**HOSTSW_OWN_GPPC_E_17:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
16	0h RW	**HOSTSW_OWN_GPPC_E_16:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**HOSTSW_OWN_GPPC_E_15:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
14	0h RW	**HOSTSW_OWN_GPPC_E_14:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
13	0h RW	**HOSTSW_OWN_GPPC_E_13:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**HOSTSW_OWN_GPPC_E_12:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
11	0h RW	**HOSTSW_OWN_GPPC_E_11:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
10	0h RW	**HOSTSW_OWN_GPPC_E_10:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**HOSTSW_OWN_GPPC_E_9:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
8	0h RW	**HOSTSW_OWN_GPPC_E_8:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
7	0h RW	**HOSTSW_OWN_GPPC_E_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**HOSTSW_OWN_GPPC_E_6:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
5	0h RW	**HOSTSW_OWN_GPPC_E_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
4	0h RW	**HOSTSW_OWN_GPPC_E_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**HOSTSW_OWN_GPPC_E_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPPC_E_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPPC_E_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPPC_E_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

20.5.22 GPI Interrupt Status (GPI_IS_GPP_C_0) - Offset 100h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 100h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_23):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_22):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
21	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_21):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_20):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
19	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_19):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_18):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_17):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
16	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_16):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_15):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_14):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_13):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_12):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_11):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_10):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_9):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_8):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_6):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.5.23 GPI Interrupt Status (GPI_IS_GPP_F_0) - Offset 104h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 104h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_23):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_22):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
21	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_21):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_20):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
19	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_19):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_18):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_17):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
16	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_16):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_15):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_14):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_13):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_12):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_11):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_10):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_9):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_8):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_6):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.5.24 GPI Interrupt Status (GPI_IS_GPP_E_0) - Offset 10Ch

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 10Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_23):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_22):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
21	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_21):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_20):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
19	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_19):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_18):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_17):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
16	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_16):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_15):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_14):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_13):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_12):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_11):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_10):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_9):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_8):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_6):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.5.25 GPI Interrupt Enable (GPI_IE_GPP_C_0) - Offset 120h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 120h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_23):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_22):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
21	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_21):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
20	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_20):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_19):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_18):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
17	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_17):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
16	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_16):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_15):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_14):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_13):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_12):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_11):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_10):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_9):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_8):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_6):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.5.26 GPI Interrupt Enable (GPI_IE_GPP_F_0) - Offset 124h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 124h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_23):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_22):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
21	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_21):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_20):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
19	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_19):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_18):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
17	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_17):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_16):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_15):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_14):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_13):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_12):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_11):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_10):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_9):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_8):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_6):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.5.27 GPI Interrupt Enable (GPI_IE_GPP_E_0) - Offset 12Ch

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 12Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_23):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_22):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
21	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_21):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
20	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_20):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_19):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_18):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
17	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_17):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
16	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_16):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_15):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_14):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_13):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_12):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_11):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_10):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_9):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_8):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_6):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.5.28 GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_0) - Offset 140h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 140h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_23):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_22):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_21):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
20	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_20):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
19	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_19):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_18):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
17	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_17):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_16):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_15):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_14):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_13):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_12):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_11):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_10):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_9):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_8):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_6):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.5.29 GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_0) - Offset 144h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 144h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_23):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_22):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_21):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
20	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_20):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
19	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_19):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_18):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
17	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_17):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_16):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_15):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_14):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_13):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_12):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_11):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_10):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_9):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_8):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_6):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.5.30 GPI General Purpose Events Status (GPI_GPE_STS_GPP_E_0) - Offset 14Ch

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 14Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_23):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_22):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_21):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
20	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_20):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
19	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_19):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_18):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
17	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_17):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_16):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_15):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_14):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_13):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_12):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_11):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_10):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_9):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_8):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_6):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.5.31 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_0) - Offset 160h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 160h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_23):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_22):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
21	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_21):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_20):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
19	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_19):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
18	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_18):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_17):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_16):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_15):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_14):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_13):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_12):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_11):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_10):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_9):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_8):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_6):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.5.32 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_0) - Offset 164h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 164h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_23):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_22):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_21):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
20	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_20):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
19	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_19):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
18	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_18):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_17):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_16):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_15):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_14):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_13):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_12):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_11):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_10):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_9):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_8):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_6):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.5.33 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_E_0) - Offset 16Ch

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 16Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_23):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_22):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
21	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_21):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_20):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
19	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_19):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
18	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_18):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
17	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_17):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_16):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_15):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_14):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_13):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_12):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_11):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_10):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_9):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_8):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_6):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.5.34 SMI Status (GPI_SMI_STS_GPP_C_0) - Offset 180h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 180h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_C_23):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
22	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_C_22):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_21):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
20	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_20):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_19):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
18	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_18):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_17):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
16	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_16):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_15):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
14	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_14):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_13):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
12	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_12):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_11):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
10	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_10):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_9):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
8	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_8):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
6	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_6):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
4	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

20.5.35 SMI Status (GPI_SMI_STS_GPP_F_0) - Offset 184h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 184h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RSV	**Reserved**
23	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_23):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
22	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_22):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_21):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
20	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_20):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_19):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
18	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_18):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_17):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
16	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_16):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_15):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
14	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_14):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_13):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
12	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_12):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_11):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
10	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_10):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_9):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
8	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_8):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
6	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_6):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
4	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_F_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

20.5.36 SMI Status (GPI_SMI_STS_GPP_E_0) - Offset 18Ch

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 18Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_E_23):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
22	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_E_22):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_E_21):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
20	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_E_20):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_E_19):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
18	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_E_18):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_E_17):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
16	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_16):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_15):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
14	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_14):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_13):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
12	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_E_12):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_E_11):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
10	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_E_10):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_E_9):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
8	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_8):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
6	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_6):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
4	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

20.5.37 SMI Enable (GPI_SMI_EN_GPP_C_0) - Offset 1A0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_23):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
22	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_22):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
21	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_21):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_20):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
19	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_19):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
18	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_18):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_17):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
16	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_16):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
15	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_15):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_14):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
13	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_13):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
12	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_12):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_11):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
10	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_10):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
9	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_9):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_8):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
7	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
6	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_6):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
4	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
3	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

20.5.38 SMI Enable (GPI_SMI_EN_GPP_F_0) - Offset 1A4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RSV	**Reserved**
23	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_23):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
22	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_22):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
21	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_21):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
20	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_20):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
19	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_19):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
18	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_18):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
17	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_17):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
16	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_16):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_15):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
14	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_14):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
13	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_13):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_12):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
11	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_11):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
10	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_10):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_9):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
8	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_8):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
7	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_6):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
5	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
4	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

20.5.39 SMI Enable (GPI_SMI_EN_GPP_E_0) - Offset 1ACh

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_23):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
22	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_22):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_21):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
20	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_20):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
19	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_19):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_18):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
17	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_17):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
16	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_16):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_15):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
14	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_14):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
13	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_13):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_12):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
11	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_11):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
10	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_10):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_9):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
8	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_8):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
7	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_6):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
5	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
4	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

20.5.40 NMI Status (GPI_NMI_STS_GPP_C_0) - Offset 1C0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_C_23):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_C_22):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_21):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
20	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_20):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
19	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_19):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_18):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
17	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_17):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_16):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_15):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_14):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_13):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_12):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_11):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_10):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_9):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_8):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_6):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.5.41 NMI Status (GPI_NMI_STS_GPP_F_0) - Offset 1C4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RSV	**Reserved**
23	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_23):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_22):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_21):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
20	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_20):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
19	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_19):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_18):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
17	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_17):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_16):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_15):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_14):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_13):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_12):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_11):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_10):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_9):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_8):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_6):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_F_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.5.42 NMI Status (GPI_NMI_STS_GPP_E_0) - Offset 1CCh

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_E_23):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_E_22):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_E_21):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
20	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_E_20):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
19	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_E_19):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_E_18):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
17	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_E_17):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_16):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_15):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_14):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_13):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_E_12):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_E_11):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_E_10):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_E_9):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_8):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_6):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.5.43 NMI Enable (GPI_NMI_EN_GPP_C_0) - Offset 1E0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_23):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_22):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_21):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
20	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_20):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
19	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_19):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_18):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
17	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_17):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_16):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_15):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_14):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_13):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_12):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_11):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_10):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_9):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_8):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_6):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.5.44 NMI Enable (GPI_NMI_EN_GPP_F_0) - Offset 1E4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RSV	**Reserved**
23	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_23):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_22):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
21	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_21):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_20):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
19	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_19):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
18	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_18):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_17):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_16):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
15	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_15):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_14):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_13):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
12	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_12):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_11):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_10):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
9	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_9):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_8):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_6):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.5.45 NMI Enable (GPI_NMI_EN_GPP_E_0) - Offset 1ECh

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_23):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_22):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
21	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_21):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_20):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
19	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_19):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
18	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_18):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_17):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_16):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
15	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_15):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_14):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_13):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
12	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_12):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_11):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_10):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
9	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_9):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_8):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_6):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.5.46 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_0) - Offset 700h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 700h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.47 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_0) - Offset 704h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 704h	0000006Eh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	6Eh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.48 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_1) - Offset 710h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 710h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.49 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_1) - Offset 714h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 714h	0000006Fh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	6Fh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.50 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_2) - Offset 720h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 720h	44000200h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.51 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_2) - Offset 724h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 724h	00000070h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	70h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.52 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_3) - Offset 730h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 730h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.53 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_3) - Offset 734h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 734h	00000071h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	71h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.54 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_4) - Offset 740h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 740h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.55 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_4) - Offset 744h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 744h	00000072h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	72h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.56 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_5) - Offset 750h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 750h	44000200h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.57 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_5) - Offset 754h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 754h	00000073h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	73h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.58 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_6) - Offset 760h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 760h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.59 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_6) - Offset 764h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 764h	00000074h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	74h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.60 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_7) - Offset 770h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 770h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.61 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_7) - Offset 774h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 774h	00000075h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	75h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.62 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_8) - Offset 780h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 780h	44000B00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	2h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.63 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_8) - Offset 784h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 784h	00001076h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	4h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	76h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.64 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_9) - Offset 790h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 790h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.65 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_9) - Offset 794h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 794h	00000077h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	77h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.66 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_10) - Offset 7A0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 7A0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.67 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_10) - Offset 7A4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 7A4h	00000018h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	18h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.68 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_11) - Offset 7B0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 7B0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.69 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_11) - Offset 7B4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 7B4h	00000019h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	19h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.70 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_12) - Offset 7C0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 7C0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.71 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_12) - Offset 7C4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 7C4h	0000001Ah

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	1Ah RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.72 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_13) - Offset 7D0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 7D0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.73 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_13) - Offset 7D4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 7D4h	0000001Bh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	1Bh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.74 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_14) - Offset 7E0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 7E0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.75 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_14) - Offset 7E4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 7E4h	0000001Ch

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	1Ch RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.76 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_15) - Offset 7F0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 7F0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.77 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_15) - Offset 7F4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 7F4h	0000001Dh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	1Dh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.78 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_16) - Offset 800h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 800h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.79 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_16) - Offset 804h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 804h	0000001Eh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	1Eh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.80 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_17) - Offset 810h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 810h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.81 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_17) - Offset 814h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 814h	0000001Fh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	1Fh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.82 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_18) - Offset 820h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 820h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.83 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_18) - Offset 824h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 824h	00000020h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	20h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.84 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_19) - Offset 830h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 830h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.85 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_19) - Offset 834h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 834h	00000021h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	21h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.86 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_20) - Offset 840h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 840h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.87 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_20) - Offset 844h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 844h	00000022h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	22h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.88 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_21) - Offset 850h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 850h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.89 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_21) - Offset 854h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 854h	00000023h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	23h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.90 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_22) - Offset 860h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 860h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.91 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_22) - Offset 864h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 864h	00000024h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	24h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.92 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_23) - Offset 870h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 870h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.93 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_23) - Offset 874h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 874h	00000025h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	25h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.94 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_0) - Offset 880h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 880h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.95 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_0) - Offset 884h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 884h	00000056h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	56h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.96 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_1) - Offset 890h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 890h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.97 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_1) - Offset 894h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 894h	00003057h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Ch RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	57h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.98 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_2) - Offset 8A0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 8A0h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.99 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_2) - Offset 8A4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 8A4h	00000058h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	58h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.100 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_3) - Offset 8B0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 8B0h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.101 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_3) - Offset 8B4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 8B4h	00003059h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Ch RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	59h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.102 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_4) - Offset 8C0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 8C0h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.103 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_4) - Offset 8C4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 8C4h	0000005Ah

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	5Ah RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.104 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_5) - Offset 8D0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 8D0h	44000B00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	2h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.105 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_5) - Offset 8D4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 8D4h	0000005Bh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	5Bh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.106 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_6) - Offset 8E0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 8E0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.107 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_6) - Offset 8E4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 8E4h	0000005Ch

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	5Ch RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.108 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_7) - Offset 8F0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 8F0h	44000200h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.109 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_7) - Offset 8F4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 8F4h	0000005Dh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behavior of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	5Dh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.110 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_8) - Offset 900h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 900h	44001700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	5h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.111 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_8) - Offset 904h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 904h	0000005Eh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	5Eh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.112 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_9) - Offset 910h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 910h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.113 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_9) - Offset 914h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 914h	0000005Fh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	5Fh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.114 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_10) - Offset 920h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 920h	44000200h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.115 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_10) - Offset 924h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 924h	00000060h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	60h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.116 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_11) - Offset 930h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 930h	44001700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	5h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.117 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_11) - Offset 934h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 934h	00000061h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	61h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.118 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_12) - Offset 940h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 940h	44001700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	5h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.119 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_12) - Offset 944h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 944h	00000062h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	62h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.120 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_13) - Offset 950h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 950h	44001700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	5h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.121 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_13) - Offset 954h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 954h	00000063h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	63h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.122 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_14) - Offset 960h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 960h	44001700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	5h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.123 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_14) - Offset 964h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 964h	00000064h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	64h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.124 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_15) - Offset 970h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 970h	44001700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	5h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.125 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_15) - Offset 974h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 974h	00000065h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	65h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.126 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_16) - Offset 980h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 980h	44001700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	5h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.127 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_16) - Offset 984h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 984h	00000066h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	66h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.128 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_17) - Offset 990h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 990h	44001700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	5h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.129 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_17) - Offset 994h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 994h	00000067h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behavior of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	67h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.130 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_18) - Offset 9A0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 9A0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.131 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_18) - Offset 9A4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 9A4h	00000068h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	68h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.132 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_19) - Offset 9B0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 9B0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.133 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_19) - Offset 9B4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 9B4h	00000069h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	69h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.134 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_20) - Offset 9C0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 9C0h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.135 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_20) - Offset 9C4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 9C4h	0000006Ah

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	6Ah RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.136 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_21) - Offset 9D0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 9D0h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.137 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_21) - Offset 9D4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 9D4h	0000006Bh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	6Bh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.138 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_22) - Offset 9E0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 9E0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.139 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_22) - Offset 9E4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 9E4h	0000006Ch

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	6Ch RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.140 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_23) - Offset 9F0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 9F0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.141 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_23) - Offset 9F4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 9F4h	0000006Dh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	6Dh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.142 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_0) - Offset A70h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + A70h	44001B00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	6h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.143 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_0) - Offset A74h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + A74h	00000026h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	26h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.144 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_1) - Offset A80h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + A80h	44001B00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	6h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.145 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_1) - Offset A84h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + A84h	00000027h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behavior of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	27h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.146 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_2) - Offset A90h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + A90h	44001B00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	6h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.147 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_2) - Offset A94h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + A94h	00000028h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	28h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.148 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_3) - Offset AA0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + AA0h	44001B00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	6h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.149 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_3) - Offset AA4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + AA4h	00000029h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	29h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.150 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_4) - Offset AB0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + AB0h	44001B00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	6h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.151 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_4) - Offset AB4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + AB4h	00000030h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	30h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.152 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_5) - Offset AC0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + AC0h	44001B00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	6h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.153 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_5) - Offset AC4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + AC4h	000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.154 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_6) - Offset AD0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + AD0h	44001A00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	6h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.155 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_6) - Offset AD4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + AD4h	00000032h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	32h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.156 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_7) - Offset AE0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + AE0h	44001B00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	6h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.157 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_7) - Offset AE4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + AE4h	00000033h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	33h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.158 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_8) - Offset AF0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + AF0h	44001B00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	6h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.159 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_8) - Offset AF4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + AF4h	00000034h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	34h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.160 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_9) - Offset B00h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B00h	44001B00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RW	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	6h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.161 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_9) - Offset B04h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B04h	00000035h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	35h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.162 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_10) - Offset B10h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B10h	44001B00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	6h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.163 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_10) - Offset B14h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B14h	00000036h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	36h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.164 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_11) - Offset B20h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B20h	44001B00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	6h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.165 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_11) - Offset B24h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B24h	00000037h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behavior of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	37h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.166 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_12) - Offset B30h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B30h	44001B00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	6h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.167 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_12) - Offset B34h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B34h	00000038h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	38h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.168 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_13) - Offset B40h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B40h	44001B00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	6h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.169 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_13) - Offset B44h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B44h	00000039h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	39h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.170 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_14) - Offset B50h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B50h	44001B00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	6h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.171 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_14) - Offset B54h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B54h	0000003Ah

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	3Ah RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.172 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_15) - Offset B60h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B60h	44000B00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	2h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.173 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_15) - Offset B64h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B64h	0000003Bh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	3Bh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.174 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_16) - Offset B70h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B70h	44000B00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	2h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.175 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_16) - Offset B74h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B74h	0000003Ch

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behavior of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	3Ch RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.176 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_17) - Offset B80h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B80h	44001B00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	6h RW/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.177 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_17) - Offset B84h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B84h	0000003Dh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	3Dh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.178 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_18) - Offset B90h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B90h	44001700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	5h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.179 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_18) - Offset B94h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B94h	00003C3Eh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Fh RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	3Eh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.180 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_19) - Offset BA0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + BA0h	44001600h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	5h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.181 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_19) - Offset BA4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + BA4h	00003C3Fh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Fh RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	3Fh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.182 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_20) - Offset BB0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + BB0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.183 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_20) - Offset BB4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + BB4h	00000040h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	40h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.184 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_21) - Offset BC0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + BC0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.185 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_21) - Offset BC4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + BC4h	00000041h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	41h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.186 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_22) - Offset BD0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + BD0h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.187 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_22) - Offset BD4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + BD4h	00000042h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	42h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.5.188 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_23) - Offset BE0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + BE0h	44000200h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) or Global Reset (i.e global_rst_b) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:14	0h RO	**Reserved**
13:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.5.189 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_23) - Offset BE4h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + BE4h	00000043h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	43h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.6 GPIO Community 5 Registers Summary

This chapter documents GPIO 5 Registers.

Table 20-6. Summary of GPIO 5 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8h	4	Family Base Address (FAMBAR)	00000300h
Ch	4	Pad Base Address (PADBAR)	00000700h
10h	4	Miscellaneous Configuration (MISCCFG)	37043200h
20h	4	Pad Ownership (PAD_OWN_GPP_R_0)	00000000h
80h	4	Pad Configuration Lock (PADCFGLOCK_GPP_R_0)	00000000h
84h	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_R_0)	00000000h
B0h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_R_0)	00000000h
100h	4	GPI Interrupt Status (GPI_IS_GPP_R_0)	00000000h
120h	4	GPI Interrupt Enable (GPI_IE_GPP_R_0)	00000000h
140h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_0)	00000000h
160h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_0)	00000000h
180h	4	SMI Status (GPI_SMI_STS_GPP_R_0)	00000000h
1A0h	4	SMI Enable (GPI_SMI_EN_GPP_R_0)	00000000h
1C0h	4	NMI Status (GPI_NMI_STS_GPP_R_0)	00000000h
1E0h	4	NMI Enable (GPI_NMI_EN_GPP_R_0)	00000000h
700h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_0)	44000700h
704h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_0)	00000070h
710h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_1)	44000700h
714h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_1)	00003C71h
720h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_2)	44000600h
724h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_2)	00003C72h
730h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_3)	44000700h
734h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_3)	00003C73h
740h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_4)	44000700h
74Ch	4	Pad Configuration DW3 (PAD_CFG_DW1_GPP_R_4)	00000000h
750h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_5)	44000300h
754h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_5)	00000075h
760h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_6)	44000300h
764h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_6)	00000076h
770h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_7)	44000300h
774h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_7)	00000077h

20.6.1 Family Base Address (FAMBAR) - Offset 8h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 8h	00000300h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0300h RO	**Family Base Address (FAMBAR):** This field provides the starting byte-align address of Family0 register sets within a Community. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

20.6.2 Pad Base Address (PADBAR) - Offset Ch

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + Ch	00000700h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0700h RO	**Pad Base Address (PADBAR):** This field provides the starting byte-align address of Pad0 register sets within a Community. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

20.6.3 Miscellaneous Configuration (MISCCFG) - Offset 10h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 10h	37043200h

Bit Range	Default & Access	Field Name (ID): Description
31:24	37h RW	**GPIO Driver Mode Interrupt Select (GPDMINTSEL):** IRQ globally for all pads (GPI_IS with corresponding GPI_IE enable). 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255
23:20	0h RO	**Reserved**
19:16	4h RW	**Reserved**
15:12	3h RW	**GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The setting is processor specific.
11:8	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[:0]. The setting is processor specific.
7	0h RW	**GPIO IOSF Sideband VNNREQ Enable (GPVNNREQEN):** Specify whether the GPIO Community should take part in IOSFSB VNNREQ/ACK handshake 0 = Disable participation in IOSF SB VNNREQ and VNNACK handshake 1 = Enable participation in IOSF SB VNNREQ and VNNACK handshake When this bit set to 1, GPIO controller will de-assert the VNNREQ when there is no outstanding IOSF SB upstream cycle from GPIO controller. When this bit set to 1 and MISCSECCFG.SBTRIGDIS is 0, GPIO controller will assert the VNNREQ to request for the following list of IOSF-SB Message initiation. Event list: IRQ NMI SMI SSMI Fuse/Soft strap pull VNNREQ shall de-assert when MISCSECCFG.SBTRIGDIS is set to 1. As VNNAON IP, GPIO controller will assert the VNNREQ when in reset. The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pwrgate_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this power gating, this register always default to 1.
6	0h RW	**GPIO PGCB Clock Dynamic Partition Clock Gating Enable (GPPGCBDPCGEN):** Specify whether the GPIO Community PGCB clock should take part in partition clock gating 0 = Disable participation in PGCB clock dynamic partition clock gating 1 = Enable participation in PGCB clock dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**GPIO IOSF Sideband Dynamic Partition Clock Gating Enable (GPSIDEDPCGEN):** Specify whether the GPIO Community IOSF sideband clock should take part in partition clock gating 0 = Disable participation in IOSF sideband clock dynamic partition clock gating 1 = Enable participation in IOSF sideband clock dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
4	0h RW	**GPIO RCOMP clock Dynamic Local Clock Gating (GPRCOMPCDLCGEN):** Specify whether the GPIO Community should perform local clock gating on RCOMP clock 0 = Disable dynamic RCOMP clock local clock gating 1 = Enable dynamic RCOMP clock local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
3	0h RW	**GPIO RTC clock Dynamic Local Clock Gating (GPRTCDLCGEN):** Specify whether the GPIO Community should perform local clock gating on RTC clock 0 = Disable dynamic RTC clock local clock gating 1 = Enable dynamic RTC clock local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
2	0h RO	**Reserved**
1	0h RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN):** Specify whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0
0	0h RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN):** Specify whether the GPIO Community should perform local clock gating 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For processor that does not have the soft strap defined for this clock gating, this register always default to 0

20.6.4 Pad Ownership (PAD_OWN_GPP_R_0) - Offset 20h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPP_R_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPP_R_6):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPP_R_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPP_R_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPP_R_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPP_R_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPP_R_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPP_R_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, and PSE do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into unsuccessful completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = PSE GPIO Mode. Same description as CSME GPIO Mode above except verifying PSE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the PSE GPIO Function. '11' = Reserved. All other values are reserved. Implementation shall treat reserved values the same as 0h.

20.6.5 Pad Configuration Lock (PADCFGLOCK_GPP_R_0) - Offset 80h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_6):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally.

20.6.6 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_R_0) - Offset 84h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_6):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value.

20.6.7 Host Software Pad Ownership (HOSTSW_OWN_GPP_R_0) - Offset B0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**HOSTSW_OWN_GPP_R_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
6	0h RW	**HOSTSW_OWN_GPP_R_6:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
5	0h RW	**HOSTSW_OWN_GPP_R_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**HOSTSW_OWN_GPP_R_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
3	0h RW	**HOSTSW_OWN_GPP_R_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPP_R_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPP_R_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPP_R_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

20.6.8 GPI Interrupt Status (GPI_IS_GPP_R_0) - Offset 100h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 100h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_6):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.6.9 GPI Interrupt Enable (GPI_IE_GPP_R_0) - Offset 120h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 120h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_6):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

20.6.10 GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_0) - Offset 140h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 140h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_6):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STSbit is set: If the system is in an S3-S5 state, the event will also wake the system. Refer to Cspec Chapter 16 Power Management. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_ENdoes not prevent the setting of GPI_GPE_STS. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.6.11 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_0) - Offset 160h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 160h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_6):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STSbit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

20.6.12 SMI Status (GPI_SMI_STS_GPP_R_0) - Offset 180h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 180h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_R_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
6	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_R_6):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_R_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
4	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_R_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_R_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_R_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_R_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_R_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

20.6.13 SMI Enable (GPI_SMI_EN_GPP_R_0) - Offset 1A0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 1A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_R_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
6	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_R_6):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
5	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_R_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_R_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
3	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_R_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_R_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_R_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_R_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

20.6.14 NMI Status (GPI_NMI_STS_GPP_R_0) - Offset 1C0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 1C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_R_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_R_6):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_R_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_R_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_R_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_R_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_R_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_R_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.6.15 NMI Enable (GPI_NMI_EN_GPP_R_0) - Offset 1E0h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 1E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_R_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_R_6):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_R_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_R_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_R_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_R_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_R_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_R_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

20.6.16 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_0) - Offset 700h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 700h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.6.17 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_0) - Offset 704h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 704h	00000070h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	70h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.6.18 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_1) - Offset 710h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 710h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	**Reserved**
11:10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.6.19 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_1) - Offset 714h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 714h	00003C71h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Fh RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behavior of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	71h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.6.20 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_2) - Offset 720h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 720h	44000600h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.6.21 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_2) - Offset 724h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 724h	00003C72h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions.These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions.These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions.These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions.These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions.These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions.These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions.These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):**See CFIO HIP Interface for details on these control bit descriptions.These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions.These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions.These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Fh RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	72h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.6.22 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_3) - Offset 730h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 730h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.6.23 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_3) - Offset 734h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 734h	00003C73h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions.These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions.These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions.These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Fh RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behavior of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	73h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.6.24 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_4) - Offset 740h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 740h	44000700h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.6.25 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_4) - Offset 744h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 744h	00000074h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	74h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.6.26 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_5) - Offset 750h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 750h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.6.27 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_5) - Offset 754h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 754h	00000075h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	75h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.6.28 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_6) - Offset 760h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 760h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Synchronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.6.29 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_6) - Offset 764h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 764h	00000076h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	76h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

20.6.30 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_7) - Offset 770h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 770h	44000300h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the processor responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

20.6.31 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_7) - Offset 774h

More details to Register Field.

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 774h	00000077h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is processor specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW/FW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily. The recommended settings are [3:0]: 0 000: Disable 0 001: 1k wpd 0 010: 5k wpd 0 100: 20k wpd 1 000: 20k & 5k & 1k wpu 1 001: 1k wpu 1 010: 5k wpu 1 011: 1k & 5k wpu 1 100: 20k wpu 1 101: 20k & 1k wpu 1 110: 20k & 5k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination Note: Not all settings above represent a valid combination. The setting is only applicable if the buffer coupled with the pad has the corresponding weak pull-up and/or pull-down support (e.g. for a buffer that do not implement the 1K wpu, following settings should be treated as Reserved: b'1000, b'1001, b'1011', b'1101'. Hardware must ensure the CFIO wpu/wpd signals do not glitch.
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	77h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

21 8254 Timer

21.1 8254 Timer Registers Summary

Table 21-1. Summary of 8254 Timer Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40h	1	Counter 0_Interval Timer Status Byte Format Register (C0_ITSBFR)	C4h
42h	1	Counter 2_Interval Timer Status Byte Format Register (C2_ITSBFR)	C4h
43h	1	Timer Control Word Register (TCW)	00h

21.1.1 Counter 0_Interval Timer Status Byte Format Register (C0_ITSBFR) - Offset 40h

Each counter's status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for a given counter, the next read from the counter's Counter Access Ports Register (40h for counter 0 and 42h for counter 2) returns the status byte. The status byte returns the following:

Type	Size	Offset	Default
IO	8 bit	40h	C4h

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Counter OUT Pin State (COPS):** When this bit is a 1, the OUT pin of the counter is also a 1. When this bit is a 0, the OUT pin of the counter is also a 0.
6	1h RO	**Count Register Status (CRSTS):** This bit indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the counter mode, but until the count is loaded into the counting element (CE), the count value will be incorrect. 0 Count has been transferred from CR to CE and is available for reading. 1 Null Count. Count has not been transferred from CR to CE and is not yet available for reading.

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**Read/Write Selection Status (RW_SLT_STS):** These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	2h RO	**Mode Selection Status (MD_SLT_STS):** These bits return the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	0h RO	**Countdown Type Status (CDT_STS):** This bit reflects the current countdown type, ether 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.

21.1.2 Counter 2_Interval Timer Status Byte Format Register (C2_ITSBFR) - Offset 42h

Each counter's status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for a given counter, the next read from the counter's Counter Access Ports Register (40h for counter 0 and 42h for counter 2) returns the status byte. The status byte returns the following:

Type	Size	Offset	Default
IO	8 bit	42h	C4h

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Counter OUT Pin State (COPS):** When this bit is a 1, the OUT pin of the counter is also a 1 When this bit is a 0, the OUT pin of the counter is also a 0
6	1h RO	**Count Register Status (CRSTS):** This bit indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the counter mode, but until the count is loaded into the counting element (CE), the count value will be incorrect. 0 Count has been transferred from CR to CE and is available for reading 1 Null Count. Count has not been transferred from CR to CE and is not yet available for reading
5:4	0h RO	**Read/Write Selection Status (RW_SLT_STS):** These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	2h RO	**Mode Selection Status (MD_SLT_STS):** These bits return the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	0h RO	**Countdown Type Status (CDT_STS):** This bit reflects the current countdown type, ether 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.

21.1.3 Timer Control Word Register (TCW) - Offset 43h

This register is programmed prior to any counter being accessed to specify counter modes. Following reset, the control words for each register are undefined and each counter output is 0. Each timer must be programmed to bring it into a known state.

There are two special commands that can be issued to the counters through this register, the Read Back Command and the Counter Latch Command. When these commands are chosen, several bits within this register are redefined.

Type	Size	Offset	Default
IO	8 bit	43h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h WO	**Counter Select (CNT_SLT):** The Counter Selection bits select the counter the control word acts upon as shown below. The Read Back Command is selected when bits[7:6] are both 1 00 Counter 0 select 01 Reserved 10 Counter 2 select 11 Read Back Command
5:4	0h WO	**Read/Write Select: (RW_SLT):** These bits are the read/write control bits. The actual counter programming is done through the counter port (40h for counter 0 and 42h for counter 2) 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	0h WO	**Counter Mode Selection (CNT_MD_SLTN):** These bits select one of six possible modes of operation for the selected counter. 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	0h WO	**Binary/BCD Countdown Select (B_BCD_CNTDWN_SLT):** 0 Binary countdown is used. The largest possible binary count is 2^16 1 Binary coded decimal (BCD) count is used. The largest possible BCD count is 10^4

22 Processor Interface

22.1 Processor Interface Registers Summary

Table 22-1. Summary of Processor Interface Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
61h	1	NMI Status and Control (NMI_STS_CNT)	20h
70h	1	NMI Enable (and Real Time Clock Index) (NMI_EN)	80h
92h	1	Init Register (PORT92)	00h
CF9h	1	Reset Control Register (RST_CNT)	00h

22.1.1 NMI Status and Control (NMI_STS_CNT) - Offset 61h

NMI Status and Control Register.

Type	Size	Offset	Default
IO	8 bit	61h	20h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**SERR NMI Source Status (SERR_NMI_STS):** This bit is set by any of the sources of the internal SERR on the PCH backbone, this includes SERR assertions forwarded from the secondary PCI bus, error from a PCIe port, Do_SERR or standard PCIe error message from DMI, or internal Bus 0 functions that generate SERR#. Bit 2 must be cleared in this register in order for this bit to be set. This interrupt source is enabled by setting bit 2 to 0. To reset the interrupt, set bit 2 to 1 and then set it to 0. This bit is read-only. When writing to port 61h, this bit must be 0.
6	0h RO	**IOCHK NMI Source Status (IOCHK_NMI_STS):** This bit is set if an ISA agent (via SERIRQ) asserts IOCHK# and bit 3 is cleared in this register. This interrupt source is enabled by setting bit 3 to 0. To reset the interrupt, set bit 3 to 1 and then set it to 0. This bit is read-only. When writing to port 61h, this bit must be a 0.
5	1h RO	**Timer Counter 2 OUT Status (TMR2_OUT_STS):** This bit reflects the current state of the 8254 counter 2 output. Counter 2 must be programmed following any PCI reset for this bit to have a determinate value. When writing to port 61h, this bit must be a 0.
4	0h RO/V	**REF_TOGGLE field (REF_TOGGLE):** Refresh Cycle Toggle. This signal toggles from either 0 to 1 or 1 to 0 at a rate approximately to the low and high duty cycle times of the RTC clock operating at 32.5kHz.
3	0h RW	**IOCHK NMI Enable (IOCHK_NMI_EN):** When this bit is a 1, IOCHK# NMIs are disabled and cleared. When this bit is a 0, IOCHK# NMIs are enabled.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**PCI SERR Enable (PCI_SERR_EN):** When this bit is a 1, the SERR# NMIs are disabled and cleared. When this bit is a 0, SERR# NMIs are enabled.
1	0h RW	**Speaker Data Enable (SPKR_DAT_EN):** When this bit is a 0, the SPKR output is a 0. When this bit is a 1, the SPKR output is equivalent to the Counter 2 OUT signal value.
0	0h RW	**Timer Counter 2 Enable (TIM_CNT2_EN):** When this bit is a 0, Counter 2 counting is disabled. Counting is enabled when this bit is 1.

22.1.2 NMI Enable (and Real Time Clock Index) (NMI_EN) - Offset 70h

This register is write-only for normal operation. In Alt-Access mode, this register can be read to find the NMI Enable status and the RTC index value.

*Read/Write (Special), Use RW/V because there is no equivalent register access attribute in RDL.

Type	Size	Offset	Default
IO	8 bit	70h	80h

Bit Range	Default & Access	Field Name (ID): Description
7	1h WO	**NMI_EN field (NMI_EN):** When this bit is a 1, all NMI sources are disabled. When this bit is a 0, NMI source is enabled.
6:0	00h WO	**Real Time Clock Index (Address) (RTC_INDX):** This data goes to the RTC to select which register or CMOS RAM address is being accessed.

22.1.3 Init Register (PORT92) - Offset 92h

Port92 Init register.

Type	Size	Offset	Default
IO	8 bit	92h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	**Reserved**
0	0h RW	**INIT NOW (INIT_NOW):** When this bit transitions from a 0 to a 1, the PCH will force INIT# active for 16 PCI clocks.

22.1.4 Reset Control Register (RST_CNT) - Offset CF9h

Reset Control register.

Type	Size	Offset	Default
IO	8 bit	CF9h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**Reserved**
3	0h RW	**Full Reset (FULL_RST):** When this bit is set to 1 and bit 1 is set to 1 (indicating Hard Reset, not Soft Reset), and the RST_CPU bit (bit 2) is written from 0 to 1, the PCH will do a full reset, including driving SLP_S3#, SLP_S4# and SLP_S5# active (low) for at least 3 (and no more than 5) seconds. When this bit is set, it also causes the full power cycle (SLP_S3/4/5# assertion) in response to SYSRESET#, PWROK#, and Watchdog timer reset sources.
2	0h RW	**Reset CPU (RST_CPU):** This bit will cause either a hard or soft reset to the CPU depending on the state of the SYS_RST bit (bit 1 in this same register). The software will cause the reset by setting bit 2 from a 0 to a 1.
1	0h RW	**System Reset (SYS_RST):** The bit determines the type of reset caused via RST_CPU (bit 2 of this register). If SYS_RST is 0 when RST_CPU goes from 0 to 1, then the PCH will force INIT# active for 16 PCI clocks. If SYS_RST is 1 when RST_CPU goes from 0 to 1, then the PCH will force PCI reset active for about 1 ms, however the SLP_S3#, SLP_S4# and SLP_S5# signals assertion is dependent on the value of the FULL_RST (bit3 of this register).
0	0h RO	**Reserved**

23 Advanced Programmable Interrupt Controller (APIC)

23.1 APIC Indirect Registers Summary

APIC Indirect Registers lists the registers that can be accessed within the APIC using the Index Register. When accessing these registers, accesses must be done one DWord at a time. For example, software should never access byte 2 from the Data register before accessing bytes 0 and 1. The hardware will not attempt to recover from a bad programming model in this case.

Index	Mnemonic	Register Name
10-11h	RTE0	Redirection Table Entry 0
12-13h	RTE1	Redirection Table Entry 1
14-15h	RTE2	Redirection Table Entry 2
...	...	...
3E-3Fh	RTE23	Redirection Table Entry 23
40-41h	RTE24	Redirection Table Entry 24
...	...	...
FE-FFh	RTE119	Redirection Table Entry 119

Table 23-1. Summary of APIC Indirect Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Identification Register (IDR)	00000000h
1h	4	Version Register (VS)	00770020h
10h	8	Redirection Table Entry 0 (RTE0)	0000000000010000h
12h	8	Redirection Table Entry 1 (RTE1)	0000000000010000h
14h	8	Redirection Table Entry 2 (RTE2)	0000000000010000h
16h	8	Redirection Table Entry 3 (RTE3)	0000000000010000h
18h	8	Redirection Table Entry 4 (RTE4)	0000000000010000h
1Ah	8	Redirection Table Entry 5 (RTE5)	0000000000010000h
1Ch	8	Redirection Table Entry 6 (RTE6)	0000000000010000h
1Eh	8	Redirection Table Entry 7 (RTE7)	0000000000010000h
20h	8	Redirection Table Entry 8 (RTE8)	0000000000010000h
22h	8	Redirection Table Entry 9 (RTE9)	0000000000010000h
24h	8	Redirection Table Entry 10 (RTE10)	0000000000010000h
26h	8	Redirection Table Entry 11 (RTE11)	0000000000010000h
28h	8	Redirection Table Entry 12 (RTE12)	0000000000010000h
2Ah	8	Redirection Table Entry 13 (RTE13)	0000000000010000h
2Ch	8	Redirection Table Entry 14 (RTE14)	0000000000010000h
2Eh	8	Redirection Table Entry 15 (RTE15)	0000000000010000h
30h	8	Redirection Table Entry 16 (RTE16)	0000000000010000h

Table 23-1. Summary of APIC Indirect Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
32h	8	Redirection Table Entry 17 (RTE17)	0000000000010000h
34h	8	Redirection Table Entry 18 (RTE18)	0000000000010000h
36h	8	Redirection Table Entry 19 (RTE19)	0000000000010000h
38h	8	Redirection Table Entry 20 (RTE20)	0000000000010000h
3Ah	8	Redirection Table Entry 21 (RTE21)	0000000000010000h
3Ch	8	Redirection Table Entry 22 (RTE22)	0000000000010000h
3Eh	8	Redirection Table Entry 23 (RTE23)	0000000000010000h
40h	8	Redirection Table Entry 24 (RTE24)	0000000000010000h
42h	8	Redirection Table Entry 25 (RTE25)	0000000000010000h
44h	8	Redirection Table Entry 26 (RTE26)	0000000000010000h
46h	8	Redirection Table Entry 27 (RTE27)	0000000000010000h
48h	8	Redirection Table Entry 28 (RTE28)	0000000000010000h
4Ah	8	Redirection Table Entry 29 (RTE29)	0000000000010000h
4Ch	8	Redirection Table Entry 30 (RTE30)	0000000000010000h
4Eh	8	Redirection Table Entry 31 (RTE31)	0000000000010000h
50h	8	Redirection Table Entry 32 (RTE32)	0000000000010000h
52h	8	Redirection Table Entry 33 (RTE33)	0000000000010000h
54h	8	Redirection Table Entry 34 (RTE34)	0000000000010000h
56h	8	Redirection Table Entry 35 (RTE35)	0000000000010000h
58h	8	Redirection Table Entry 36 (RTE36)	0000000000010000h
5Ah	8	Redirection Table Entry 37 (RTE37)	0000000000010000h
5Ch	8	Redirection Table Entry 38 (RTE38)	0000000000010000h
5Eh	8	Redirection Table Entry 39 (RTE39)	0000000000010000h
60h	8	Redirection Table Entry 40 (RTE40)	0000000000010000h
62h	8	Redirection Table Entry 41 (RTE41)	0000000000010000h
64h	8	Redirection Table Entry 42 (RTE42)	0000000000010000h
66h	8	Redirection Table Entry 43 (RTE43)	0000000000010000h
68h	8	Redirection Table Entry 44 (RTE44)	0000000000010000h
6Ah	8	Redirection Table Entry 45 (RTE45)	0000000000010000h
6Ch	8	Redirection Table Entry 46 (RTE46)	0000000000010000h
6Eh	8	Redirection Table Entry 47 (RTE47)	0000000000010000h
70h	8	Redirection Table Entry 48 (RTE48)	0000000000010000h
72h	8	Redirection Table Entry 49 (RTE49)	0000000000010000h
74h	8	Redirection Table Entry 50 (RTE50)	0000000000010000h
76h	8	Redirection Table Entry 51 (RTE51)	0000000000010000h
78h	8	Redirection Table Entry 52 (RTE52)	0000000000010000h
7Ah	8	Redirection Table Entry 53 (RTE53)	0000000000010000h
7Ch	8	Redirection Table Entry 54 (RTE54)	0000000000010000h
7Eh	8	Redirection Table Entry 55 (RTE55)	0000000000010000h

Table 23-1. Summary of APIC Indirect Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
80h	8	Redirection Table Entry 56 (RTE56)	0000000000010000h
82h	8	Redirection Table Entry 57 (RTE57)	0000000000010000h
84h	8	Redirection Table Entry 58 (RTE58)	0000000000010000h
86h	8	Redirection Table Entry 59 (RTE59)	0000000000010000h
88h	8	Redirection Table Entry 60 (RTE60)	0000000000010000h
8Ah	8	Redirection Table Entry 61 (RTE61)	0000000000010000h
8Ch	8	Redirection Table Entry 62 (RTE62)	0000000000010000h
8Eh	8	Redirection Table Entry 63 (RTE63)	0000000000010000h
90h	8	Redirection Table Entry 64 (RTE64)	0000000000010000h
92h	8	Redirection Table Entry 65 (RTE65)	0000000000010000h
94h	8	Redirection Table Entry 66 (RTE66)	0000000000010000h
96h	8	Redirection Table Entry 67 (RTE67)	0000000000010000h
98h	8	Redirection Table Entry 68 (RTE68)	0000000000010000h
9Ah	8	Redirection Table Entry 69 (RTE69)	0000000000010000h
9Ch	8	Redirection Table Entry 70 (RTE70)	0000000000010000h
9Eh	8	Redirection Table Entry 71 (RTE71)	0000000000010000h
A0h	8	Redirection Table Entry 72 (RTE72)	0000000000010000h
A2h	8	Redirection Table Entry 73 (RTE73)	0000000000010000h
A4h	8	Redirection Table Entry 74 (RTE74)	0000000000010000h
A6h	8	Redirection Table Entry 75 (RTE75)	0000000000010000h
A8h	8	Redirection Table Entry 76 (RTE76)	0000000000010000h
AAh	8	Redirection Table Entry 77 (RTE77)	0000000000010000h
ACh	8	Redirection Table Entry 78 (RTE78)	0000000000010000h
AEh	8	Redirection Table Entry 79 (RTE79)	0000000000010000h
B0h	8	Redirection Table Entry 80 (RTE80)	0000000000010000h
B2h	8	Redirection Table Entry 81 (RTE81)	0000000000010000h
B4h	8	Redirection Table Entry 82 (RTE82)	0000000000010000h
B6h	8	Redirection Table Entry 83 (RTE83)	0000000000010000h
B8h	8	Redirection Table Entry 84 (RTE84)	0000000000010000h
BAh	8	Redirection Table Entry 85 (RTE85)	0000000000010000h
BCh	8	Redirection Table Entry 86 (RTE86)	0000000000010000h
BEh	8	Redirection Table Entry 87 (RTE87)	0000000000010000h
C0h	8	Redirection Table Entry 88 (RTE88)	0000000000010000h
C2h	8	Redirection Table Entry 89 (RTE89)	0000000000010000h
C4h	8	Redirection Table Entry 90 (RTE90)	0000000000010000h
C6h	8	Redirection Table Entry 91 (RTE91)	0000000000010000h
C8h	8	Redirection Table Entry 92 (RTE92)	0000000000010000h
CAh	8	Redirection Table Entry 93 (RTE93)	0000000000010000h
CCh	8	Redirection Table Entry 94 (RTE94)	0000000000010000h

Table 23-1. Summary of APIC Indirect Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
CEh	8	Redirection Table Entry 95 (RTE95)	0000000000010000h
D0h	8	Redirection Table Entry 96 (RTE96)	0000000000010000h
D2h	8	Redirection Table Entry 97 (RTE97)	0000000000010000h
D4h	8	Redirection Table Entry 98 (RTE98)	0000000000010000h
D6h	8	Redirection Table Entry 99 (RTE99)	0000000000010000h
D8h	8	Redirection Table Entry 100 (RTE100)	0000000000010000h
DAh	8	Redirection Table Entry 101 (RTE101)	0000000000010000h
DCh	8	Redirection Table Entry 102 (RTE102)	0000000000010000h
DEh	8	Redirection Table Entry 103 (RTE103)	0000000000010000h
E0h	8	Redirection Table Entry 104 (RTE104)	0000000000010000h
E2h	8	Redirection Table Entry 105 (RTE105)	0000000000010000h
E4h	8	Redirection Table Entry 106 (RTE106)	0000000000010000h
E6h	8	Redirection Table Entry 107 (RTE107)	0000000000010000h
E8h	8	Redirection Table Entry 108 (RTE108)	0000000000010000h
EAh	8	Redirection Table Entry 109 (RTE109)	0000000000010000h
ECh	8	Redirection Table Entry 110 (RTE110)	0000000000010000h
EEh	8	Redirection Table Entry 111 (RTE111)	0000000000010000h
F0h	8	Redirection Table Entry 112 (RTE112)	0000000000010000h
F2h	8	Redirection Table Entry 113 (RTE113)	0000000000010000h
F4h	8	Redirection Table Entry 114 (RTE114)	0000000000010000h
F6h	8	Redirection Table Entry 115 (RTE115)	0000000000010000h
F8h	8	Redirection Table Entry 116 (RTE116)	0000000000010000h
FAh	8	Redirection Table Entry 117 (RTE117)	0000000000010000h
FCh	8	Redirection Table Entry 118 (RTE118)	0000000000010000h
FEh	8	Redirection Table Entry 119 (RTE119)	0000000000010000h

23.1.1 Identification Register (IDR) - Offset 0h

Offset 00h - 00h

Type	Size	Offset	Default
MMIO	32 bit	FEC00000h +0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:24	0h RW	**APIC Identification (AID):** Software must program this value before using the APIC.
23:16	0h RO	**Reserved**
15	0h RW	**Scratchpad Field (SPD):** ITSS Scratchpad Field
14:0	0h RO	**Reserved**

23.1.2 Version Register (VS) - Offset 1h

Offset 01h - 01h

Type	Size	Offset	Default
MMIO	32 bit	FEC00000h + 1h	00770020h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	77h RW	**Maximum Redirection Entries (MRE):** This is the entry number (0 being the lowest entry) of the highest entry in the redirection table. In PCH this field is defaulted to 17h to indicate 24 interrupts. This field is Read-Write-Once. BIOS must write to this field after PLTRST# to lockdown the value. This allows BIOS to use some of the entries for its own purpose and thus advertising fewer IOxAPIC Redirection Entries to OS. BIOS may to program this field up to 78h (maximum 120 entries).
15	0h RO	**Pin Assertion Register Supported (PRQ):** Indicate that the IOxAPIC does not implement the Pin Assertion Register.
14:8	0h RO	**Reserved**
7:0	20h RO	**Version field (VS):** Identifies the implementation version as IOxAPIC.

23.1.3 Redirection Table Entry 0 (RTE0) - Offset 10h

Offset 10h - 11h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 10h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.4 Redirection Table Entry 1 (RTE1) - Offset 12h

Offset 12h - 13h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 12h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.5 Redirection Table Entry 2 (RTE2) - Offset 14h

Offset 14h - 15h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 14h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.6 Redirection Table Entry 3 (RTE3) - Offset 16h

Offset 16h - 17h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 16h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.7 Redirection Table Entry 4 (RTE4) - Offset 18h

Offset 18h - 19h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 18h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.8 Redirection Table Entry 5 (RTE5) - Offset 1Ah

Offset 1Ah - 1Bh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 1Ah	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.9 Redirection Table Entry 6 (RTE6) - Offset 1Ch

Offset 1Ch - 1Dh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 1Ch	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.10 Redirection Table Entry 7 (RTE7) - Offset 1Eh

Offset 1Eh - 1Fh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 1Eh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.11 Redirection Table Entry 8 (RTE8) - Offset 20h

Offset 20h - 21h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 20h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.12 Redirection Table Entry 9 (RTE9) - Offset 22h

Offset 22h - 23h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 22h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.13 Redirection Table Entry 10 (RTE10) - Offset 24h

Offset 24h - 25h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 24h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.14 Redirection Table Entry 11 (RTE11) - Offset 26h

Offset 26h - 27h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 26h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.15 Redirection Table Entry 12 (RTE12) - Offset 28h

Offset 28h - 29h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 28h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.16 Redirection Table Entry 13 (RTE13) - Offset 2Ah

Offset 2Ah - 2Bh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 2Ah	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.17 Redirection Table Entry 14 (RTE14) - Offset 2Ch

Offset 2Ch - 2Dh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 2Ch	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.18 Redirection Table Entry 15 (RTE15) - Offset 2Eh

Offset 2Eh - 2Fh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 2Eh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.19 Redirection Table Entry 16 (RTE16) - Offset 30h

Offset 30h - 31h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 30h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.20 Redirection Table Entry 17 (RTE17) - Offset 32h

Offset 32h - 33h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 32h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.21 Redirection Table Entry 18 (RTE18) - Offset 34h

Offset 34h - 35h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 34h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.22 Redirection Table Entry 19 (RTE19) - Offset 36h

Offset 36h - 37h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 36h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.23 Redirection Table Entry 20 (RTE20) - Offset 38h

Offset 38h - 39h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 38h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.24 Redirection Table Entry 21 (RTE21) - Offset 3Ah

Offset 3Ah - 3Bh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 3Ah	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.25 Redirection Table Entry 22 (RTE22) - Offset 3Ch

Offset 3Ch - 3Dh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 3Ch	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.26 Redirection Table Entry 23 (RTE23) - Offset 3Eh

Offset 3Eh - 3Fh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 3Eh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.27 Redirection Table Entry 24 (RTE24) - Offset 40h

Offset 40h - 41h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 40h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.28 Redirection Table Entry 25 (RTE25) - Offset 42h

Offset 42h - 43h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 42h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.29 Redirection Table Entry 26 (RTE26) - Offset 44h

Offset 44h - 45h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 44h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.30 Redirection Table Entry 27 (RTE27) - Offset 46h

Offset 46h - 47h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 46h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.31 Redirection Table Entry 28 (RTE28) - Offset 48h

Offset 48h - 49h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 48h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.32 Redirection Table Entry 29 (RTE29) - Offset 4Ah

Offset 4Ah - 4Bh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 4Ah	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.33 Redirection Table Entry 30 (RTE30) - Offset 4Ch

Offset 4Ch - 4Dh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 4Ch	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.34 Redirection Table Entry 31 (RTE31) - Offset 4Eh

Offset 4Eh - EFh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 4Eh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.35 Redirection Table Entry 32 (RTE32) - Offset 50h

Offset 50h - 51h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 50h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.36 Redirection Table Entry 33 (RTE33) - Offset 52h

Offset 52h - 53h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 52h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.37 Redirection Table Entry 34 (RTE34) - Offset 54h

Offset 54h - 55h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 54h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.38 Redirection Table Entry 35 (RTE35) - Offset 56h

Offset 56h - 57h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 56h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.39 Redirection Table Entry 36 (RTE36) - Offset 58h

Offset 58h - 59h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 58h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.40 Redirection Table Entry 37 (RTE37) - Offset 5Ah

Offset 5Ah - 5Bh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 5Ah	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.41 Redirection Table Entry 38 (RTE38) - Offset 5Ch

Offset 5Ch - 5Dh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 5Ch	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.42 Redirection Table Entry 39 (RTE39) - Offset 5Eh

Offset 5Eh - 5Fh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 5Eh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.43 Redirection Table Entry 40 (RTE40) - Offset 60h

Offset 60h - 61h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 60h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.44 Redirection Table Entry 41 (RTE41) - Offset 62h

Offset 62h - 63h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 62h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.45 Redirection Table Entry 42 (RTE42) - Offset 64h

Offset 64h - 65h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 64h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.46 Redirection Table Entry 43 (RTE43) - Offset 66h

Offset 66h - 67h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 66h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.47 Redirection Table Entry 44 (RTE44) - Offset 68h

Offset 68h - 69h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 68h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.48 Redirection Table Entry 45 (RTE45) - Offset 6Ah

Offset 6Ah - 6Bh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 6Ah	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.49 Redirection Table Entry 46 (RTE46) - Offset 6Ch

Offset 6Ch - 6Dh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 6Ch	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.50 Redirection Table Entry 47 (RTE47) - Offset 6Eh

Offset 6Eh - 6Fh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 6Eh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.51 Redirection Table Entry 48 (RTE48) - Offset 70h

Offset 70h - 71h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 70h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.52 Redirection Table Entry 49 (RTE49) - Offset 72h

Offset 72h - 73h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 72h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.53 Redirection Table Entry 50 (RTE50) - Offset 74h

Offset 74h - 75h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 74h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.54 Redirection Table Entry 51 (RTE51) - Offset 76h

Offset 76h - 77h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 76h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.55 Redirection Table Entry 52 (RTE52) - Offset 78h

Offset 78h - 79h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 78h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.56 Redirection Table Entry 53 (RTE53) - Offset 7Ah

Offset 7Ah - 7Bh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 7Ah	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.57 Redirection Table Entry 54 (RTE54) - Offset 7Ch

Offset 7Ch - 7Dh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 7Ch	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.58 Redirection Table Entry 55 (RTE55) - Offset 7Eh

Offset 7Eh - 7Fh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 7Eh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.59 Redirection Table Entry 56 (RTE56) - Offset 80h

Offset 80h - 81h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 80h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.60 Redirection Table Entry 57 (RTE57) - Offset 82h

Offset 82h - 83h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 82h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.61 Redirection Table Entry 58 (RTE58) - Offset 84h

Offset 84h - 85h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 84h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.62 Redirection Table Entry 59 (RTE59) - Offset 86h

Offset 86h - 87h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 86h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.63 Redirection Table Entry 60 (RTE60) - Offset 88h

Offset 88h - 89h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 88h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.64 Redirection Table Entry 61 (RTE61) - Offset 8Ah

Offset 8Ah - 8Bh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 8Ah	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.65 Redirection Table Entry 62 (RTE62) - Offset 8Ch

Offset 8Ch - 8Dh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 8Ch	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.66 Redirection Table Entry 63 (RTE63) - Offset 8Eh

Offset 8Eh - 8Fh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 8Eh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.67 Redirection Table Entry 64 (RTE64) - Offset 90h

Offset 90h - 91h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 90h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.68 Redirection Table Entry 65 (RTE65) - Offset 92h

Offset 92h - 93h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 92h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.69 Redirection Table Entry 66 (RTE66) - Offset 94h

Offset 94h - 95h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 94h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.70 Redirection Table Entry 67 (RTE67) - Offset 96h

Offset 96h - 97h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 96h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.71 Redirection Table Entry 68 (RTE68) - Offset 98h

Offset 98h - 99h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 98h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.72 Redirection Table Entry 69 (RTE69) - Offset 9Ah

Offset 9Ah - 9Bh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 9Ah	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.73 Redirection Table Entry 70 (RTE70) - Offset 9Ch

Offset 9Ch - 9Dh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 9Ch	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.74 Redirection Table Entry 71 (RTE71) - Offset 9Eh

Offset 9Eh - 9Fh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + 9Eh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.75 Redirection Table Entry 72 (RTE72) - Offset A0h

Offset A0h - A1h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + A0h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.76 Redirection Table Entry 73 (RTE73) - Offset A2h

Offset A2h - A3h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + A2h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.77 Redirection Table Entry 74 (RTE74) - Offset A4h

Offset A4h - A5h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + A4h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.78 Redirection Table Entry 75 (RTE75) - Offset A6h

Offset A6h - A7h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + A6h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.79 Redirection Table Entry 76 (RTE76) - Offset A8h

Offset A8h - A9h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + A8h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.80 Redirection Table Entry 77 (RTE77) - Offset AAh

Offset AAh - ABh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + AAh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.81 Redirection Table Entry 78 (RTE78) - Offset ACh

Offset ACh - ADh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + ACh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.82 Redirection Table Entry 79 (RTE79) - Offset AEh

Offset AEh - AFh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + AEh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.83 Redirection Table Entry 80 (RTE80) - Offset B0h

Offset B0h - B1h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + B0h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.84 Redirection Table Entry 81 (RTE81) - Offset B2h

Offset B2h - B3h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + B2h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.85 Redirection Table Entry 82 (RTE82) - Offset B4h

Offset B4h - B5h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + B4h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.86 Redirection Table Entry 83 (RTE83) - Offset B6h

Offset B6h - B7h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + B6h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.87 Redirection Table Entry 84 (RTE84) - Offset B8h

Offset B8h - B9h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + B8h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.88 Redirection Table Entry 85 (RTE85) - Offset BAh

Offset BAh - BBh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + BAh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.89 Redirection Table Entry 86 (RTE86) - Offset BCh

Offset BCh - BDh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + BCh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.90 Redirection Table Entry 87 (RTE87) - Offset BEh

Offset BEh - BFh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + BEh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.91 Redirection Table Entry 88 (RTE88) - Offset C0h

Offset C0h - C1h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + C0h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.92 Redirection Table Entry 89 (RTE89) - Offset C2h

Offset C2h - C3h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + C2h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.93 Redirection Table Entry 90 (RTE90) - Offset C4h

Offset C4h - C5h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + C4h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.94 Redirection Table Entry 91 (RTE91) - Offset C6h

Offset C6h - C7h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + C6h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.95 Redirection Table Entry 92 (RTE92) - Offset C8h

Offset C8h - C9h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + C8h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.96 Redirection Table Entry 93 (RTE93) - Offset CAh

Offset CAh - CBh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + CAh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.97 Redirection Table Entry 94 (RTE94) - Offset CCh

Offset CCh - CDh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + CCh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.98 Redirection Table Entry 95 (RTE95) - Offset CEh

Offset CEh - CFh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + CEh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.99 Redirection Table Entry 96 (RTE96) - Offset D0h

Offset D0h - D1h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + D0h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.100 Redirection Table Entry 97 (RTE97) - Offset D2h

Offset D2h - D3h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + D2h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.101 Redirection Table Entry 98 (RTE98) - Offset D4h

Offset D4h - D5h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + D4h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.102 Redirection Table Entry 99 (RTE99) - Offset D6h

Offset D6h - D7h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + D6h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.103 Redirection Table Entry 100 (RTE100) - Offset D8h

Offset D8h - D9h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + D8h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.104 Redirection Table Entry 101 (RTE101) - Offset DAh

Offset DAh - DBh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + DAh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.105 Redirection Table Entry 102 (RTE102) - Offset DCh

Offset DCh - DDh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + DCh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.106 Redirection Table Entry 103 (RTE103) - Offset DEh

Offset DEh - DFh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + DEh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.107 Redirection Table Entry 104 (RTE104) - Offset E0h

Offset E0h - E1h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + E0h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.108 Redirection Table Entry 105 (RTE105) - Offset E2h

Offset E2h - E3h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + E2h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.109 Redirection Table Entry 106 (RTE106) - Offset E4h

Offset E4h - E5h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + E4h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.110 Redirection Table Entry 107 (RTE107) - Offset E6h

Offset E6h - E7h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + E6h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.111 Redirection Table Entry 108 (RTE108) - Offset E8h

Offset E8h - E9h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + E8h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.112 Redirection Table Entry 109 (RTE109) - Offset EAh

Offset EAh - EBh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + EAh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.113 Redirection Table Entry 110 (RTE110) - Offset ECh

Offset ECh - EDh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + ECh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.114 Redirection Table Entry 111 (RTE111) - Offset EEh

Offset EEh - EFh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + EEh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.115 Redirection Table Entry 112 (RTE112) - Offset F0h

Offset F0h - F1h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + F0h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.116 Redirection Table Entry 113 (RTE113) - Offset F2h

Offset F2h - F3h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + F2h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.117 Redirection Table Entry 114 (RTE114) - Offset F4h

Offset F4h - F5h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + F4h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.118 Redirection Table Entry 115 (RTE115) - Offset F6h

Offset F6h - F7h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + F6h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.119 Redirection Table Entry 116 (RTE116) - Offset F8h

Offset F8h - F9h

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + F8h	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.120 Redirection Table Entry 117 (RTE117) - Offset FAh

Offset FAh - FBh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + FAh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.121 Redirection Table Entry 118 (RTE118) - Offset FCh

Offset FCh - FDh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + FCh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.1.122 Redirection Table Entry 119 (RTE119) - Offset FEh

Offset FEh - FFh

Type	Size	Offset	Default
MMIO	64 bit	FEC00000h + FEh	0000000000010000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	00h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved**
16	1h RW	**Mask field (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity field (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local APIC to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act on reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (check with 13.2.3 for details). 011 Reserved 100 NMI Not supported (check with 13.2.3 for details). 101 INIT Not supported (check with 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	00h RW	**Vector field (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

23.2 APIC Registers Summary

Table 23-2. Summary of APIC Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
FEC00000h	4	Index Register (IDX)	00000000h
FEC00010h	4	Window Register (WDW)	00000000h
FEC00040h	4	EOI Register (EOI)	00000000h

23.2.1 Index Register (IDX) - Offset FEC00000h

This 8-bit register selects which indirect register appears in the window register to be manipulated by software. Software will program this register to select the desired APIC internal register.

Type	Size	Offset	Default
MMIO	32 bit	FEC00000h + FEC00000h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Index Register (IDX):** Index Register for APIC.

23.2.2 Window Register (WDW) - Offset FEC00010h

This 32-bit register specifies the data to be read or written to the register pointed to by the IDX register. This register can be accessed only in DW quantities.

Type	Size	Offset	Default
MMIO	32 bit	FEC00000h + FEC00010h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Window Register (WDW):** Window Register for APIC.

23.2.3 EOI Register (EOI) - Offset FEC00040h

When a write is issued to this register, the IOxAPIC will check the lower 8 bits written to this register, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, RTE.RIRR for that entry will be cleared. If multiple entries have the same vector, each of those entries will have RTE.RIRR cleared. Only bits 7:0 are used. Bits 31:8 are ignored.

Type	Size	Offset	Default
MMIO	32 bit	FEC00000h + FEC00040h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h WO	**EOI Register (EOI):** EOI Register field.

24 High Precision Event Timer (HPET)

24.1 HPET Memory Mapped Registers Summary

The timer registers are memory mapped directly (rather than indexed) to allow the CPU to access each register without having to use an index register. This ensures accesses are safe for multi-threaded environments. The timer register space is 1024 bytes. The registers are generally aligned on 64-bit boundaries to simplify implementation with IA64 processors. In the PCH, there are 4 possible memory address ranges beginning at 1) FED0_0000h, 2) FED0_1000h, 3) FED0_2000h, 4) FED0_3000h. The choice of address range should be selected by assigning the High Performance Event Timer Configuration (HPTC) register fields in the configuration space of the Primary to Sideband Bridge. All registers are implemented in the Primary power well, and all bits are reset by PLTRST#. Reads to reserved registers or bits will return a value of 0.
Behavioral Rules:
1. Software can read or write the various bytes in these registers using 32-bit or 64-bit accesses. Software must not attempt to read or write across register boundaries. For example, a 32-bit access should be to offset x0h, x4h, x8h, or xCh. 32-bit accesses should not be to 01h, 02h, 03h, 05h, 06h, 07h, 09h, 0Ah, 0Bh, 0Dh, 0Eh, or 0Fh. Any accesses to these offsets will result in an unexpected behavior, and may result in a master abort. However, these accesses should not result in system hangs. 64-bit accesses can only be to x0h and must not cross 64-bit boundaries.
2. Software should not write to read-only registers.
3. Software should not expect any particular or consistent value when reading reserved registers or bits.

Table 24-1. Summary of HPET Memory Mapped Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
FED00000h	8	General Capabilities and ID Register (GEN_CAP_ID)	027BC86B8086A701h
FED00010h	8	General Config Register (GEN_CFG)	0000000000000000h
FED00020h	8	General Interrupt Status Register (GEN_INT_STS)	0000000000000000h
FED000F0h	8	Main Counter Value (MAIN_CNTR)	0000000000000000h
FED00100h	8	Timer 0 Config and Capabilities (TMR0_CNF_CAP)	00F0000000008030h
FED00108h	8	Timer 0 Comparator Value (TMR0_CMP_VAL)	FFFFFFFFFFFFFFFFh

24.1.1 General Capabilities and ID Register (GEN_CAP_ID) - Offset FED00000h

Software can read the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 000h or 004h. 64-bit accesses may only be done to 000h. Writes to this register will have no effect.

Type	Size	Offset	Default
MMIO	64 bit	HPET Base + FED00000h	027BC86B8086A701h

Bit Range	Default & Access	Field Name (ID): Description
63:32	027BC86Bh RO/V	**Main Counter Tick Period (COUNTER_CLK_PER_CAP):** This read-only field indicates the period at which the counter increments in femtoseconds (10^-15 seconds). The PCH HPET timers use a 24 MHz clock, which has a period of 41,666,667 femtoseconds. Therefore this register will always return 027BC86Bh when read. Change by input strap value. If gpcom_strap_xtal_sel=0, then default value will equal to CNTR_CLK_PER_CAP_DEF. If gpcom_strap_xtal_sel=1, then default value will equal to CNTR_CLK_PER_CAP_DEF_CLK1.
31:16	8086h RO	**Vendor ID (VENDOR_ID_CAP):** These bits will return 8086h when read to reflect Intel as the vendor.
15	1h RO	**Legacy Rout Capable (LEG_RT_CAP):** This bit will always be 1 when read, indicating support for the Legacy Interrupt Rout.
14	0h RO	**Reserved**
13	1h RO	**Counter Size (COUNT_SIZE_CAP):** This bit will return 1 when read to indicate support for 64-bit counters allowing 64 or 32-bit mode operation.
12:8	07h RO	**Number of Timers (NUM_TIM_CAP):** This value in this field will be 07h to indicate support for 8 timers in the timer block.
7:0	01h RO	**Revision ID (REV_ID):** The value in this field will be 01h to indicate for revision 1.0 of the HPET specification.

24.1.2 General Configuration Register (GEN_CFG) - Offset FED00010h

Software can read the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 010h or 014h. 64-bit accesses may only be done to 010h.

Type	Size	Offset	Default
MMIO	64 bit	HPET Base + FED00010h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:2	0h RO	**Reserved**
1	0h RW	**Legacy Rout (LEG_RT_CNF):** If the LEG_RT_CNF bit is set, then the interrupts will be routed as follows: Timer 0 will be routed to IRQ0 in 8259 or IRQ2 in the I/O APIC Timer 1 will be routed to IRQ8 in 8259 or IRQ8 in the I/O APIC Timer 2-7 will be routed as per the routing in that timers Configuration register. If the LEG_RT_CNF bit is set, the individual routing bits for timers 0 and 1 (APIC or FSB) will have no impact. Otherwise, if the LEG_RT_CNF bit is not set, the individual routing bits for each of the timers are used. This bit will default to 0. BIOS can set it to 1 to enable the legacy routing, or 0 to disable the legacy routing. When changing other bits in this register, this bit should be left unchanged. Otherwise, a spurious interrupt may occur.
0	0h RW	**Overall Enable (ENABLE_CNF):** This bit must be set to enable any of the timers to generate interrupts. If this bit is 0, then the main counter will halt (will not increment) and no interrupts will be caused by any of these timers. For level-triggered interrupts, if an interrupt is pending when the ENABLE_CNF bit is changed from 1 to 0, the interrupt status indications (in the various Txx_INT_STS bits) will not be cleared. Software must write to the Txx_INT_STS bits to clear the interrupts. Intel Specific: This bit will default to 0. BIOS can set it to 1 or 0.

24.1.3 General Interrupt Status Register (GEN_INT_STS) - Offset FED00020h

Software can read the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 020h or 024h. 64-bit accesses may only be done to 020h.

Type	Size	Offset	Default
MMIO	64 bit	HPET Base + FED00020h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:8	0h RO	**Reserved**
7	0h RW/1C	**Timer 7 Interrupt Active (T07_INT_STS):** The functionality of this bit depends on whether the edge or level-triggered mode is used for this timer: If set to edge triggered mode this bit will always read as 0 and writes will have no effect. If set to level-triggered mode: This bit will be set by hardware if the corresponding timer interrupt is active. Once the bit is set, it can be cleared by software writing a 1 to the same bit position. Writes of 0 to this bit will have no effect. For example if the bit is already set, a write of 0 will not clear the bit. This bit defaults to 0.
6	0h RW/1C	**Timer 6 Interrupt Active (T06_INT_STS):** The functionality of this bit depends on whether the edge or level-triggered mode is used for this timer: If set to edge triggered mode this bit will always read as 0 and writes will have no effect. If set to level-triggered mode: This bit will be set by hardware if the corresponding timer interrupt is active. Once the bit is set, it can be cleared by software writing a 1 to the same bit position. Writes of 0 to this bit will have no effect. For example if the bit is already set, a write of 0 will not clear the bit. This bit defaults to 0.
5	0h RW/1C	**Timer 5 Interrupt Active (T05_INT_STS):** The functionality of this bit depends on whether the edge or level-triggered mode is used for this timer: If set to edge triggered mode this bit will always read as 0 and writes will have no effect. If set to level-triggered mode: This bit will be set by hardware if the corresponding timer interrupt is active. Once the bit is set, it can be cleared by software writing a 1 to the same bit position. Writes of 0 to this bit will have no effect. For example if the bit is already set, a write of 0 will not clear the bit. This bit defaults to 0.
4	0h RW/1C	**Timer 4 Interrupt Active (T04_INT_STS):** The functionality of this bit depends on whether the edge or level-triggered mode is used for this timer: If set to edge triggered mode this bit will always read as 0 and writes will have no effect. If set to level-triggered mode: This bit will be set by hardware if the corresponding timer interrupt is active. Once the bit is set, it can be cleared by software writing a 1 to the same bit position. Writes of 0 to this bit will have no effect. For example if the bit is already set, a write of 0 will not clear the bit. This bit defaults to 0.
3	0h RW/1C	**Timer 3 Interrupt Active (T03_INT_STS):** The functionality of this bit depends on whether the edge or level-triggered mode is used for this timer: If set to edge triggered mode this bit will always read as 0 and writes will have no effect. If set to level-triggered mode: This bit will be set by hardware if the corresponding timer interrupt is active. Once the bit is set, it can be cleared by software writing a 1 to the same bit position. Writes of 0 to this bit will have no effect. For example if the bit is already set, a write of 0 will not clear the bit. This bit defaults to 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**Timer 2 Interrupt Active (T02_INT_STS):** The functionality of this bit depends on whether the edge or level-triggered mode is used for this timer: If set to edge triggered mode this bit will always read as 0 and writes will have no effect. If set to level-triggered mode: This bit will be set by hardware if the corresponding timer interrupt is active. Once the bit is set, it can be cleared by software writing a 1 to the same bit position. Writes of 0 to this bit will have no effect. For example if the bit is already set, a write of 0 will not clear the bit. This bit defaults to 0.
1	0h RW/1C	**Timer 1 Interrupt Active (T01_INT_STS):** The functionality of this bit depends on whether the edge or level-triggered mode is used for this timer: If set to edge triggered mode this bit will always read as 0 and writes will have no effect. If set to level-triggered mode: This bit will be set by hardware if the corresponding timer interrupt is active. Once the bit is set, it can be cleared by software writing a 1 to the same bit position. Writes of 0 to this bit will have no effect. For example if the bit is already set, a write of 0 will not clear the bit. This bit defaults to 0.
0	0h RW/1C	**Timer 0 Interrupt Active (T00_INT_STS):** The functionality of this bit depends on whether the edge or level-triggered mode is used for this timer: If set to edge triggered mode this bit will always read as 0 and writes will have no effect. If set to level-triggered mode: This bit will be set by hardware if the corresponding timer interrupt is active. Once the bit is set, it can be cleared by software writing a 1 to the same bit position. Writes of 0 to this bit will have no effect. For example if the bit is already set, a write of 0 will not clear the bit. This bit defaults to 0.

24.1.4 Main Counter Value (MAIN_CNTR) - Offset FED000F0h

Software can read the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 0F0h or 0F4h. 64-bit accesses may only be done to 0F0h. Writes to this register should only be done while the counter is halted. Reads to this register return the current value of the main counter. If 32-bit software attempts to read a 64-bit counter, it should first halt the counter. Since this will delay the interrupts for all of the timers, this should be done only if the consequences are understood. It is strongly recommended that 32-bit software only operate the timer in 32-bit mode. Reads to this register are monotonic. No two consecutive reads will return the same value. The second of two reads will always return a larger value (unless the timer has rolled over to 0)

Type	Size	Offset	Default
MMIO	64 bit	HPET Base + FED000F0h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:0	0000000000000000h RW/V	**Counter Value (COUNTER_VAL):** Reads return the current value of the counter. Writes load the new value to the counter.

24.1.5 Timer 0 Configuration and Capabilities (TMR0_CNF_CAP) - Offset FED00100h

Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x0h or 1x4h. 64-bit accesses may only be done to 1x0h.

Type	Size	Offset	Default
MMIO	64 bit	HPET Base + FED00100h	00F0000000008030h

Bit Range	Default & Access	Field Name (ID): Description
63:32	00F00000h RO	**Timer 0 Interrupt Rout (TIMER0_INT_ROUT_CAP):** This 32-bit read-only field indicates to which interrupts in the 8259 or I/O (x) APIC this timers interrupt can be routed to. This is used in conjunction with the TIMERn_INT_ROUT_CNF field. Writes to this field will have no effect. Note: If interrupt is handled via 8259, only interrupts 0-15 are applicable and valid. Each bit in this field corresponds to a particular interrupt. For example, if this timers interrupt can be mapped to interrupts 16, 18, 20, 22, or 24, then bits 16, 18, 20, 22, and 24 in this field will be set to 1. All other bits will be 0. Timer 0,1: Bits 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. Timer 2: Bits 11, 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. If IRQ 11 is used, software should ensure IRQ 11 is not shared with any other devices to guarantee the proper operation of this timer. Timer 3: Bits 12, 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. If IRQ 12 is used, software should ensure IRQ 12 is not shared with any other devices to guarantee the proper operation of this timer. Timer 4-7: This field is always 0 as interrupts from these timers can only be delivered via direct FSB interrupt messages.
31:16	0h RO	**Reserved**
15	1h RO	**FSB Interrupt Delivery Capability (TIMER0_FSB_INT_DEL_CAP):** This bit is always read as 1, since the Intel PCH HPET implementation supports the direct FSB interrupt delivery.
14	0h RW	**Timer 0 FSB Interrupt Delivery Enable (TIMER0_FSB_EN_CNF):** When set, this will force the interrupts for Timer n to be delivered directly as FSB messages, rather than using the 8259 or I/O (x) APIC. In this case, the TIMERn_INT_ROUTE_CNF field in this register will be ignored and the TIMERn_FSB_ROUT register will be used instead. Timer 0, 1, 2, 3: This bit is a read/write bit. Timer 4, 5, 6, 7: This bit is always Read-Only 1 as interrupt from these timers can only be delivered via direct FSB interrupt messages.

Bit Range	Default & Access	Field Name (ID): Description
13:9	00h RW	**Interrupt Route (TIMER0_INT_ROUT_CNF):** This 5-bit field indicates the routing for the interrupt to the 8259 or I/O APIC. A maximum of 32 interrupts are supported. Software writes to this field to select which interrupt in the 8259 or I/O (x)APIC will be used for this timers interrupt. The default value for this register is 00h. If the Legacy Rout bit is set, then Timers 0 and 1 will have a different routing, and this bit field has no effect for those two timers. If the TIMERn_FSB_EN_CNF bit is set, then the interrupt will be delivered directly to the FSB, and this bit field has no effect. If interrupt is handled via 8259, only interrupts 0-15 are applicable and valid. Software must not program any value other than 0-15 in this field. Software must ensure that the value is valid for a particular timer as indicated by the TIMERn_INT_ROUTE_CAP field for that timer. The PCH logic does not check the validity of the value written. For Timers 4-7, this field is always Read-Only 0 as interrupts from these timers can only be delivered via direct FSB interrupt messages.
8	0h RW	**Timer 0 32-bit Mode (TIMER0_32_MODE_CNF):** Software can set this bit to force a 64-bit timer to behave as a 32-bit timer. This is typically needed if the software is not willing to halt the main counter to read or write a particular timer, and the software not capable of do an atomic 64-bit read to the timer. When TIMER0_32MODE_CNF is set to '1', the hardware counter will essentially be doing 32-bit operation on comparator match and rollovers. I.e. the upper 32-bit of the Timer 0 Comparator Value register is ignored. The upper 32-bit of the main counter is not involved in any roll over from lower 32-bit of the main counter and becomes all zero's. For timer 0, this bit will be read/write and default to 0. For timers 1-7, this bit will always read as 0 and writes will have no effect (since these seven timers are 32-bits).
7	0h RO	**Reserved**
6	0h WO	**Timer 0 Value Set (TIMER0_VAL_SET_CNF):** Software uses this bit only for timers that have been set to periodic mode. By writing this bit to a 1, the software is then allowed to directly set the timers accumulator. Software does NOT have to write this bit back to 0 (it automatically clears). This bit will return 0 when read. Software should not write a 1 to this bit position if the timer is set to non-periodic mode. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1-7 as they do not support the periodic mode.
5	1h RO	**Timer 0 Size (TIMER0_SIZE_CAP):** Read-only Indicator of the timers size capability. 1: 64-bits 0: 32-bits. The value is 1 (64-bits) for timer 0, and 0 (32-bits) for timers 1-7.
4	1h RO	**Periodic Interrupt Capable (TIMER0_PER_INT_CAP):** If this read-only bit is 1, then the hardware supports a periodic mode for this timers interrupt. The value is 1 (periodic supported) for timer 0, and 0 (not supported) for timers 1-7.
3	0h RW	**Timer 0 Type (TIMER0_TYPE_CNF):** Setting this bit to 1 enables the timer to generate a periodic interrupt if it is capable of doing so. If the TIMERn_PER_INT_CAP bit is 0, then this bit will always return 0 when read and writes will have no impact. For timer 0, this bit will be read/write, with default of 0. For timers 1-7, this bit will be read-only, with a fixed value of 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Timer 0 Interrupt Enable (TIMER0_INT_ENB_CNF):** This bit must be set to 1 to enable timer n to cause an interrupt when it times out. If this bit is 0, the timer can still count and generate appropriate status bits, but will not cause an interrupt. Default value is 0.
1	0h RW	**Timer Interrupt Type (TIMER0_INT_TYPE_CNF):** Determines whether an edge or level interrupt will be used for this timer (when enabled). 0: Edge-triggered. If another interrupt occurs, another edge will be generated. 1: Level-triggered. The interrupt will be held active until it is cleared by writing to the bit in the General Interrupt Status Register. If another interrupt occurs before the interrupt is cleared, the interrupt will remain active. The default value is 0, edge-triggered. The interrupt type for any timer should be set before that timer generates any interrupts. If the interrupt type is changed dynamically, there will be some delay before the new type takes effect. That delay is not specified. Timer 0-3: This bit is a read/write bit as both edge and level triggered modes are supported. Timer 4-7: This bit is always Read-Only 0 as only edge-triggered mode is supported.
0	0h RO	**Reserved**

24.1.6 Timer 0 Comparator Value (TMR0_CMP_VAL) - Offset FED00108h

Timer 0 Comparator Value Register

Type	Size	Offset	Default
MMIO	64 bit	HPET Base + FED00108h	FFFFFFFFFFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
63:0	FFFFFFFFF FFFFFFFh RW/V	**Timer 0 Comparator Value (TMR0_CMP_VAL):** If the timer is configured to non-periodic mode, when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). The value in this register does not change based on the interrupt being generated. If the timer is configured to periodic mode (supported only for Timer 0), when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). When this time out occurs, the value in this register is increased by the value last written to the register. For example, in periodic mode if the value written to the register is 0000123h: 1. An interrupt will be generated when the main counter reaches 00000123h. 2. The value in this register will then be adjusted by the hardware to 00000246h. 3. Another interrupt will be generated when the main counter reaches 00000246h. 4. The value in this register will then be adjusted by the hardware to 00000369h As each periodic interrupt occurs, the value in this register will increment. When the incremented value is greater than the maximum value possible for this register (FFFFFFFFh for a 32-bit timer or FFFFFFFFFFFFFFFFh for a 64-bit timer), the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000, then after the next interrupt the value will change to 00010000h. The default value for each timer is all 1s for the bits that are implemented. For example, a 32-bit timer will have a default value of 00000000FFFFFFFFh. A 64-bit timer will have a default value of FFFFFFFFFFFFFFFFh. Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x8h or 1xCh. 64-bit accesses may only be done to 1x8h. Comparator value. Timer 0 is 64-bits wide. Timers 1-7 are 32-bits wide.

25 Interrupt

25.1 Interrupt Registers Summary

Table 25-1. Summary of Interrupt Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
20h	1	Master Initialization Command Word 1 (MICW1)	11h
21h	1	Master Initialization Command Word 2 (MICW2)	00h
A0h	1	Slave Initialization Command Word 1 (SICW1)	11h
A1h	1	Slave Initialization Command Word 2 (SICW2)	00h
4D0h	1	Master Edge/Level Control (ELCR1)	00h
4D1h	1	Slave Edge/Level Control (ELCR2)	00h

25.1.1 Master Initialization Command Word 1 (MICW1) - Offset 20h

A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs:

1. The Interrupt Mask register is cleared.
2. IRQ7 input is assigned priority 7.
3. The slave mode address is set to 7.
4. Special Mask Mode is cleared and Status Read is set to IRR.

Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Type	Size	Offset	Default
IO	8 bit	20h	11h

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h WO	**ICW/OCW select (ICW_OCW_SLT1):** These bits are MCS-85 specific, and not needed. Should be programmed to 000.
4	1h WO	**ICW/OCW select (ICW_OCW_SLT2):** This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	0h WO	**Edge/Level Bank Select (LTIM):** Disabled. Replaced by the edge/level triggered control registers (ELCR).

Bit Range	Default & Access	Field Name (ID): Description
2	0h WO	**ADI IGNORED (ADI):** Ignored for PCH. Should be programmed to 0.
1	0h WO	**Single or Cascade (SNGL):** Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	1h WO	**ICW4 Write Required (IC4):** This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

25.1.2 Master Initialization Command Word 2 (MICW2) - Offset 21h

ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Type	Size	Offset	Default
IO	8 bit	21h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:3	00h WO	**Interrupt Vector Base Address (IVBA):** Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.
2:0	0h WO	**Interrupt Request Level (IRL):** When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: Code Master Interrupt Slave Interrupt 000 IRQ0 IRQ8 001 IRQ1 IRQ9 010 IRQ2 IRQ10 011 IRQ3 IRQ11 100 IRQ4 IRQ12 101 IRQ5 IRQ13 110 IRQ6 IRQ14 111 IRQ7 IRQ15

25.1.3 Slave Initialization Command Word 1 (SICW1) - Offset A0h

A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs:

1. The Interrupt Mask register is cleared.
2. IRQ7 input is assigned priority 7.
3. The slave mode address is set to 7.
4. Special Mask Mode is cleared and Status Read is set to IRR.

Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Type	Size	Offset	Default
IO	8 bit	A0h	11h

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h WO	**ICW/OCW select (ICW_OCW_SLT1):** These bits are MCS-85 specific, and not needed. Should be programmed to 000.
4	1h WO	**ICW/OCW select (ICW_OCW_SLT2):** This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	0h WO	**Edge/Level Bank Select (LTIM):** Disabled. Replaced by the edge/level triggered control registers (ELCR).
2	0h WO	**ADI IGNORED (ADI):** Ignored for PCH. Should be programmed to 0.
1	0h WO	**Single or Cascade (SNGL):** Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	1h WO	**ICW4 Write Required (IC4):** This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

25.1.4 Slave Initialization Command Word 2 (SICW2) - Offset A1h

ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Type	Size	Offset	Default
IO	8 bit	A1h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:3	00h WO	**Interrupt Vector Base Address (IVBA):** Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.
2:0	0h WO	**Interrupt Request Level (IRL):** When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: Code Master Interrupt Slave Interrupt 000 IRQ0 IRQ8 001 IRQ1 IRQ9 010 IRQ2 IRQ10 011 IRQ3 IRQ11 100 IRQ4 IRQ12 101 IRQ5 IRQ13 110 IRQ6 IRQ14 111 IRQ7 IRQ15

25.1.5 Master Edge/Level Control (ELCR1) - Offset 4D0h

Master Edge/Level Control Register.

Type	Size	Offset	Default
IO	8 bit	4D0h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:3	00h RW	**Edge Level Control (ELC_7_3):** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level.
2:0	0h RO	**Reserved**

25.1.6 Slave Edge/Level Control (ELCR2) - Offset 4D1h

Slave Edge/Level Control Register.

Type	Size	Offset	Default
IO	8 bit	4D1h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RW	**Edge Level Control (ELC_15_14):** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 7 applies to IRQ15, and bit 6 to IRQ14.
5	0h RW	**Edge Level Control (ELC_13):** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. This bit applies to IRQ13.
4:1	0h RW	**Edge Level Control (ELC_12_9):** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 4 applies to IRQ12, bit 3 to IRQ11, bit 2 to IRQ10, and bit 1 to IRQ9.
0	0h RO	**Reserved**

26 Real Time Clock (RTC)

26.1 RTC Indexed Registers Summary

The RTC contains two sets of indexed registers that are accessed using the two separate Index and Target registers (70h/71h or 72h/73h), as shown in the following table:

RTC (Standard) RAM Bank

Index Name
00h Seconds
01h Seconds Alarm
02h Minutes
03h Minutes Alarm
04h Hours
05h Hours Alarm
06h Day of Week
07h Day of Month
08h Month
09h Year
0Ah Register A
0Bh Register Band
0Ch Register D
0Dh Register D
0Bh-7Fh 114 Bytes of User RAM

Table 26-1. Summary of RTC Indexed Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	1	Seconds Value (SEC)	00h
1h	1	Seconds Alarm (SEC_ALARM)	00h
2h	1	Minutes Value (MINUTES)	00h
3h	1	Minutes Alarm (MINUTES_ALARM)	00h
4h	1	Hours Value (HOURS)	00h
5h	1	Hours Alarm (HOURS_ALARM)	00h
6h	1	Day Of Week (DAY_OF_WEEK)	00h
7h	1	Day Of Month (DAY_OF_MONTH)	00h
8h	1	Month Value (MONTH)	00h
9h	1	Year Value (YEAR)	00h
Ah	1	Register A (REGISTER_A)	70h
Bh	1	Register B General Configuration (REGISTER_B)	80h
Ch	1	Register C Flag Register (REGISTER_C)	00h
Dh	1	Register D Flag Register (REGISTER_D)	80h
Eh	1	114 Bytes Of Lower User RAM (REGISTER_E)	00h
80h	1	128 Bytes Of Upper User RAM (REGISTER_80)	00h

26.1.1 Seconds Value (SEC) - Offset 0h

RTC Index: 00h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current time Second

Type	Size	Offset	Default
IO	8 bit	0h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/V	**Seconds Value (SEC):** Time Seconds. The time in seconds can be represented in either BCD or Binary format depending on the value in RegB.Data Mode.

26.1.2 Seconds Alarm (SEC_ALARM) - Offset 1h

RTC Index: 01h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores Seconds Alarm

Type	Size	Offset	Default
IO	8 bit	1h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Seconds Alarm (SEC_ALARM):** Seconds field of the Alarm.

26.1.3 Minutes Value (MINUTES) - Offset 2h

RTC Index: 02h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current time Minutes

Type	Size	Offset	Default
IO	8 bit	2h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/V	**Minutes Value (MINUTES):** Time Minutes. The time in minutes can be represented in either BCD or Binary format depending on the value in RegB.Data Mode.

26.1.4 Minutes Alarm (MINUTES_ALARM) - Offset 3h

RTC Index: 03h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores Alarm Minutes

Type	Size	Offset	Default
IO	8 bit	3h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Minutes Alarm (MINUTES_ALARM):** Minutes field of the Alarm.

26.1.5 Hours Value (HOURS) - Offset 4h

RTC Index: 04h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current time Hours

Type	Size	Offset	Default
IO	8 bit	4h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/V	**Hours Value (HOURS):** Time Hours. The time in hours can be represented in either BCD or Binary format depending on the value in RegB.Data Mode. It can also be represented in either 12-hour mode or 24-hour mode depending on the value in RegB.Hour Format.

26.1.6 Hours Alarm (HOURS_ALARM) - Offset 5h

RTC Index: 05h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores Alarm Hours

Type	Size	Offset	Default
IO	8 bit	5h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Hours Alarm (HOURS_ALARM):** Hours field of the Alarm.

26.1.7 Day Of Week (DAY_OF_WEEK) - Offset 6h

RTC Index: 06h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current Day of Week

Type	Size	Offset	Default
IO	8 bit	6h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/V	**Day of Week (DAY_OF_WEEK):** This field indicates current Day of Week. 1-Sunday 2-Monday 3-Tuesday 4-Wednesday 5-Thursday 6-Friday 7-Saturday. The value is the same regardless of the Data Mode.

26.1.8 Day Of Month (DAY_OF_MONTH) - Offset 7h

RTC Index: 07h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current Day of Month

Type	Size	Offset	Default
IO	8 bit	7h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/V	**Day of Month (DAY_OF_MONTH):** This field indicates current Day of Month. The day of month can be represented in either BCD or Binary format depending on the value in RegB.Data Mode.

26.1.9 Month Value (MONTH) - Offset 8h

RTC Index: 08h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current Month

Type	Size	Offset	Default
IO	8 bit	8h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/V	**Month Value (MONTH):** This field indicates current Month. The month can be represented in either BCD or Binary format depending on the value in RegB.Data Mode.

26.1.10 Year Value (YEAR) - Offset 9h

RTC Index: 09h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current Year

Type	Size	Offset	Default
IO	8 bit	9h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/V	**Year Value (YEAR):** This field indicates current Year. The year can be represented in either BCD or Binary format depending on the value in RegB.Data Mode.

26.1.11 Register A (REGISTER_A) - Offset Ah

RTC Index: 0Ah
Default Value: 0UUUUUUU
Lockable: No Power
Attribute: Read/Write
Size: 8-bit
Well: RTC

This register is used for general configuration of the RTC functions. None of the bits are affected by RSMRST# or any other reset signal.

Type	Size	Offset	Default
IO	8 bit	Ah	70h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO/V	**UPDATE IN PROGRESS (UIP):** This bit may be monitored as a status flag. When asserted as a 1, the update is soon to occur or is in progress. If 0, the update cycle will not start for at least 488 s. The time, calendar, and alarm information in RAM is always available when the UIP bit is 0. The ICH provides the ability to generate SMI# based on either the 0-to-1 or 1-to-0 transition of this bit. This can be useful for work-around and debug in silicon.
6:4	7h RW	**Division Chain Select (DV_2_0):** These three bits control the divider chain for the oscillator, and are not affected by RSMRST# or any other reset signal. DV(2) corresponds to bit 6. DV2 DV1 DV0 Function 0 1 0 Normal Operation 1 1 X Divider Reset 1 0 1 Bypass 15 stages (test mode only) 1 0 0 Bypass 10 stages (test mode only) 0 1 1 Bypass 5 stages (test mode only) 0 0 1 Invalid 0 0 0 Invalid
3:0	0h RW	**Rate Select (RS_3_0):** Selects one of 13 taps of the 15 stage divider chain. The selected tap can generate a periodic interrupt if the PIE bit is set in Register B. Otherwise this tap will set the PF flag of Register C. If the periodic interrupt is not to be used, these bits should all be set to zero. RS3 corresponds to bit 3. RS3 RS2 RS1 RS0 Periodic Rate 0 0 0 0 Interrupt never toggles 0 0 0 1 3.90625 ms 0 0 1 0 7.8125 ms 0 0 1 1 122.070 s 0 1 0 0 244.141 s 0 1 0 1 488.281 s 0 1 1 0 976.5625 s 0 1 1 1 1.953125 ms 1 0 0 0 3.90625 ms 1 0 0 1 7.8125 ms 1 0 1 0 15.625 ms 1 0 1 1 31.25 ms 1 1 0 0 62.5 ms 1 1 0 1 125 ms 1 1 1 0 250 ms 1 1 1 1 500 ms

26.1.12 Register B General Configuration (REGISTER_B) - Offset Bh

RTC Index: 0Bh
Default Value: 10000UUU
Lockable: No

Attribute: Read/Write
Size: 8-bit
Power Well: RTC

Type	Size	Offset	Default
IO	8 bit	Bh	80h

Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**Update Cycle Inhibit (RTC_SET):** Enables/Inhibits the update cycles. When SET is 0, update cycle occurs normally once each second. If set to one, a current update cycle will abort and subsequent update cycles will not occur until SET is returned to zero. When set is one, the BIOS may initialize time and calendar bytes safely. This bit is not affected by RSMRST# nor any other reset signal. Note: Software must ensure this bit is at least transitioned from '1' to '0' once whenever the RTC coin battery is inserted. This is to ensure that the internal RTC time updates occur properly.
6	0h RW	**Periodic Interrupt Enable (PIE):** If set to 1, the Periodic Interrupt Enable (PIE) bit allows an interrupt to occur with a time base set with the RS bits of register A. This bit is cleared by RSMRST#, but not on any other reset.
5	0h RW	**Alarm Interrupt Enable (AIE):** If set to one, the Alarm Interrupt Enable (AIE) bit allows an interrupt to occur when the AF is one as set from an alarm match from the update cycle. An alarm can occur once a second, one an hour, once a day, or once a month. This bit is cleared by RTEST# assertion, but not on any other reset.
4	0h RW	**Update-ended Interrupt Enable: (UIE):** If set to one, the Update-ended Interrupt Enable (UIE) bit allows an interrupt to occur when the update cycle ends. This bit is cleared by RSMRST#, but not on any other reset.
3	0h RW	**Square Wave Enable (SQWE):** The Square Wave Enable bit serves no function in this device, yet is left in this register bank to provide compatibility with the Motorola 146818B. There is not SQW pin on this device. This bit is cleared by RSMRST#, but not on any other reset.
2	0h RW	**Data Mode (DM):** The Data Mode (DM) bit specifies either binary or BCD data representation. A one denotes binary, and zero denotes BCD. This bit is not affected by RSMRST# nor any other reset signal.
1	0h RW	**Hour Format (HOURFORM):** This bit indicates the hour byte format. If one, twenty-four hour mode is selected. If zero, twelve-hour mode is selected. In twelve hour mode, the seventh bit represents AM as zero and PM as one. This bit is not affected by RSMRST# nor any other reset signal.
0	0h RW	**Daylight Savings Enable (DSE):** The Daylight Savings Enable bit triggers two special hour updates per year when set to one. One is on the first Sunday in April, where time increments from 1:59:59 AM to 3:00:00 AM. The other is the last Sunday in October when the time first reaches 1:59:59 AM, it is changed to 1:00:00 AM. The time must increment normally for at least two update cycles (seconds) previous to these conditions for the time change to occur properly. These special update conditions do not occur when the DSE bit is set to zero. The days for the hour adjustment are those specified in United States federal law as of 1987, which is different than previous years. This bit is not affected by RSMRST# nor any other reset signal. If BUC.DSO bit is set, the DSE bit continues to be a R/W bit, but Daylight Saving is disabled regardless of the DSE bit.

26.1.13 Register C Flag Register (REGISTER_C) - Offset Ch

RTC Index: 0Ch
Default Value: 00000000
Lockable: No

Attribute: Read-Only (Writes have no effect).
Size: 8-bit
Power Well: RTC

Type	Size	Offset	Default
IO	8 bit	Ch	00h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO/V	**Interrupt Request Flag (IRQF):** Interrupt Request Flag = PF * PIE + AF * AIE + UF * UFE. This also causes the RTC Interrupt to be asserted. This bit is cleared upon RSMRST# or a read of Register C.
6	0h RO/V	**Periodic Interrupt Flag (PF):** Periodic interrupt Flag will be one when the tap as specified by the RS bits of register A is one. If no taps are specified, this flag bit will remain at zero. This bit is cleared upon RSMRST# or a read of Register C.
5	0h RO/V	**Alarm Flag (AF):** Alarm Flag will be high after all Alarm values match the current time. This bit is cleared upon RTEST# or a read of Register C.
4	0h RO/V	**Update-ended Flag (UF):** Updated-ended flag will be high immediately following an update cycle for each second. The bit is cleared upon RSMRST# or a read of Register C.
3:0	0h RO	**Reserved**

26.1.14 Register D Flag Register (REGISTER_D) - Offset Dh

RTC Index: 0Dh
Default Value: 10UUUUUU
Lockable: No Power

Attribute: Read/Write
Size: 8-bit
Well: RTC

Type	Size	Offset	Default
IO	8 bit	Dh	80h

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Valid RAM and Time Bit (VRT):** This bit is hard-wired to 1 in the RTC power well. This bit should always be written as a 0 for write cycle, however it will return a 1 for read cycles.
6	0h RO	**Reserved**
5:0	00h RW	**Date Alarm (DATE_ALARM):** These bits store the date of month alarm value. If set to 000000, then a don't care state is assumed. The host must configure the dates alarm for these bits to do anything, yet they can be written at any time. If the date alarm is not enabled, these bits will return zeros to mimic the functionality of the Motorola 146818B. These bits are not affected by any reset assertion.

26.1.15 114 Bytes Of Lower User RAM (REGISTER_E) - Offset Eh

Remaining 114 Bytes of Lower User RAM. Each byte in this bank shares the same description as shown below. RAM default values are undetermined and the last written value will be retained until RTC power is removed.

Type	Size	Offset	Default
MMIO	8 bit	+ Eh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Lower User RAM (LOWER_USER_RAM):** RTC RAM lower unused range.

26.1.16 128 Bytes Of Upper User RAM (REGISTER_80) - Offset 80h

128 Bytes of Upper User RAM. Each byte in this bank shares the same description as shown below. RAM default values are undetermined and the last written value will be retained until RTC power is removed.

Type	Size	Offset	Default
IO	8 bit	80h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Upper User RAM (UPPER_USER_RAM):** RTC RAM upper unused range.

26.2 RTC I/O Index Registers Summary

RTC I/O Index Registers Port - 70h and 71h.

Table 26-2. Summary of RTC I/O Index Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
70h	1	RTC Index Register (INDEX)	00h
71h	1	RTC Target Register (TARGET)	00h

26.2.1 RTC Index Register (INDEX) - Offset 70h

This 8-bit register selects which indirect register appears in the target register to be manipulated by software. Software will program this register to select the desired RTC indexed register.

Type	Size	Offset	Default
MMIO	8 bit	FD00000h + 70h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Index Register (INDEX):** Index Register for RTC

26.2.2 RTC Target Register (TARGET) - Offset 71h

This 32-bit register specifies the data to be read or written to the register pointed to by the INDEX register.

Type	Size	Offset	Default
MMIO	8 bit	FD00000h + 71h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/V	**RTC Target Register (TARGET):** RTC Target Register for RTC

26.3 RTC PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 26-3. Summary of RTC PCR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3400h	4	RTC Configuration (RC)	00000000h
3414h	4	Backed Up Control (BUC)	00000000h
3F04h	4	RTC Update In Progress SMI Control (UIPSMI)	00000000h

26.3.1 RTC Configuration (RC) — Offset 3400h

All bits in this register are in the Primary Well and cleared by host_side_rst_b.

Type	Size	Offset	Default
MMIO	32 bit	FDC30000h + 3400h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1L	**BIOS Interface Lock-Down (BILD):** When set, prevents RTC version of TS (BUC.TS) from being changed. This bit can only be written from 0 to 1 once. This BILD bit has different function compared to SPI and eSPI version but BIOS should set all the corresponding bits after reset in order to lock down the BIOS interface correctly.
30:7	0h RO	**Reserved**
6	0h RW	**RTC High Power Mode HW Disable (HPM_HW_DIS):** When set to 1 the internal VRM that generates the RTC Well supply voltage in SUS mode is disabled when SLP_S0# is asserted to '0'. (via irtcdswen pin to RTC EBB). When 0, HW control of the RTC internal VRM is disabled.
5	0h RW	**RTC High Power Mode SW Disable (HPM_SW_DIS):** When set to 1 the internal VRM that generates the rtc well supply voltage in SUS mode is disabled (via irtcdswen pin to RTC EBB). When 0 the internal VRM powers the rtc well when RSMRST# is '1'. (default)
4	0h RW/1L	**Partial Range Lock in Upper 128 Bytes (UL):** When set, bytes 38h-3Fh in the upper 128 byte bank of RTC RAM are locked and cannot be accessed. Writes will be dropped and reads will not return any guaranteed data. Bit reset on system reset.
3	0h RW/1L	**Partial Range Lock in Lower 128 Bytes (LL):** When set, bytes 38h-3Fh in the lower 128 byte bank of RTC RAM are locked and cannot be accessed. Writes will be dropped and reads will not return any guaranteed data. Bit reset on system reset.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Upper 128 Byte Enable (UE):** When set, the upper 128 byte bank of RTC RAM can be accessed.
1:0	0h RO	**Reserved**

26.3.2 Backed Up Control (BUC) — Offset 3414h

All bits in this register are in the RTC well and only cleared by RTEST.

Type	Size	Offset	Default
MMIO	32 bit	FDC30000h + 3414h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	None

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RW	**Daylight Savings Override (SDO):** When this bit is a '1', the DSE bit in the RTC Register B bit(0) is a RW bit but has no effect where daylight savings is hard-disabled internally. When this bit is a '0', the DSE bit in the RTC register B bit(0) is a RW bit that is configurable by software to enable the daylight savings. System BIOS shall configure this bit accordingly during the boot process before RTC time is initialized.
3:1	0h RO	**Reserved**
0	0h RW/L	**Top Swap (TS):** This should be set by BIOS when the corresponding TS bit in the eSPI controller is set in order to properly restore the state of that field after reset since they are not preserved in an RTC well bit in those devices. *If PCH is strapped for Top-Swap (GNT(3)# is low at rising edge of PWROK), then this bit cannot be cleared by software. The strap jumper should be removed and the system rebooted. **Locked by:** RC.BILD

26.3.3 RTC Update In Progress SMI Control (UIPSMI) — Offset 3F04h

This register exists in the Core Well.

Type	Size	Offset	Default
MMIO	32 bit	FDC30000h + 3F04h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	None

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RW/1C/V	**RTC UIP Low-to-High (UIP_L2H):** This sticky status bit is set whenever the RTC Update-In-Progress signal transitions from low to high (i.e., at the start of an update).
16	0h RW/1C/V	**RTC UIP High-to-Low (UIP_H2L):** This sticky status bit is set whenever the RTC Update-In-Progress signal transitions from high to low (i.e., at the start of an update).
15:2	0h RO	**Reserved**
1	0h RW	**RTC UIP Low-to-High SMI Enable (UIP_L2H_SMI_EN):** When this bit is set, a '1' in bit 17 will assert the internal SMI signal to the Power Management SMI logic.
0	0h RW	**RTC UIP High-to-Low SMI Enable (UIP_H2L_SMI_EN):** When this BIOS is set, a '1' in bit 16 will assert the internal SMI signal to the Power Management SMI logic.

27 System Management Bus TCO

27.1 SMBus TCO I/O Registers Summary

The TCO I/O registers reside in a 32-byte range that starts from the IO Base Address described in the TCOBAR register in the SMBus PCI Configuration space.

Table 27-1. Summary of SMBus TCO I/O Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	TCO_RLD Register (TRLD)	0004h
2h	1	TCO_DAT_IN Register (TDI)	00h
3h	1	TCO_DAT_OUT Register (TDO)	00h
4h	2	TCO1_STS Register (TSTS1)	0000h
6h	2	TCO2_STS Register (TSTS2)	0000h
8h	2	TCO1_CNT Register (TCTL1)	0000h
Ah	2	TCO2_CNT Register (TCTL2)	0008h
Ch	2	TCO Message Registers (TMSG)	0000h
Eh	1	TCO_WDSTATUS Register (TWDS)	00h
10h	1	LEGACY_ELIM Register (LE)	03h
12h	2	TCO_TMR Register (TTMR)	0004h

27.1.1 TCO_RLD Register (TRLD) - Offset 0h

TCO_RLD Register

Type	Size	Offset	Default
IO	16 bit	SMBus TCO + 0h	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	**Reserved**
9:0	004h RW	**TCORLD:** Reading this register will return the current count of the TCO timer. Writing any value to this register will reload the timer to prevent the timeout.

27.1.2 TCO_DAT_IN Register (TDI) - Offset 2h

TCO_DAT_IN Register

Type	Size	Offset	Default
IO	8 bit	SMBus TCO + 2h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**TDI:** Data Register for passing commands from the OS to the SMI handler. Writes to this register will cause an SMI and set the OS_TCO_SMI bit in the TCO_STS register.

27.1.3 TCO_DAT_OUT Register (TDO) - Offset 3h

TCO_DAT_OUT Register

Type	Size	Offset	Default
IO	8 bit	SMBus TCO + 3h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**TDO:** Data Register for passing commands from the SMI handler to the OS. Writes to this register will set the TCO_INT_STS bit in the TCO_STS register. It also causes an interrupt, as selected by the TCO_IRQ_SEL bits.

27.1.4 TCO1_STS Register (TSTS1) - Offset 4h

Unless otherwise indicated, these bits are sticky and are cleared by writing a 1 to the corresponding bit position.

Type	Size	Offset	Default
IO	16 bit	SMBus TCO + 4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Reserved**
13	0h RO	**TCO Slave Select (TCO_SLVSEL):** This register bit indicates the value of TCO Slave Select Soft Strap.
12	0h RW/1C	**CPUSERR_STS:** This bit is set to 1 if the CPU complex sends a DMI special cycle message indicating that it wants to cause an SERR#. The software must read the MCH to find out why it wanted the SERR#. Software must write a 1 back to this bit to clear it.
11	0h RO	**Reserved**
10	0h RW/1C	**CPUSMI_STS:** This bit is set to 1 if the CPU complex sends a DMI special cycle message indicating that it wants to cause an SMI. The software must read the CPU to find out why it wanted the SMI. Software must write a 1 back to this bit to clear it.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/1C	**CPUSCI_STS:** This bit is set to 1 if the CPU complex sends a DMI special cycle message indicating that it wants to cause an SCI. The software must read the CPU to find out why it wanted the SCI. Software must write a 1 back to this bit to clear it.
8	0h RW/1C	**BIOSWR_STS:** Intel PCH sets this bit to 1 and generates and SMI# to indicate an illegal attempt to write to the BIOS. (The BIOS write could be either to FirmwareHUB (FWH) or SPI Flash). This occurs when either: a) The WP bit (10.1.7.4 bit 0) is changed from 0 to 1 and the LE bit (10.1.7.4 bit 1) is also set, or b) any write is attempted to the BIOS and the WP bit is also set. Note: On write cycles attempted to the 4MB lower alias to the BIOS space, the BIOSWR_STS bit will not be set.
7	0h RW/1C	**NEWCENTURY_STS:** This bit will be set when the year rolls over from 1999 to 2000. If the bit is already 1, it will remain 1. This bit can be cleared either by software writing a 1 back to the bit position, or by RTEST# going active. When this bit is set, an SMI# will be generated. However, this will not be a wake event (i.e. if the system is in a sleeping state when the NEWCENTURY_STS bit is set, the system will not wake up). Note: This bit 7 is not valid when the RTC battery is first put in (or if the RTC battery does not provide sufficient power when the system is unplugged). Software can determine that the RTC well was not maintained by checking the RTC_PWR_STS bit (GEN_PMCON_3 register in the Power Management Controller, D31:F2:A4, bit 2) or by other means (such as doing a checksum on the RTC RAM array). If the RTC well is determined to not have been maintained, the BIOS should set the time to a legal value and then clear the NEWCENTURY_STS bit. Note: This bit may take up to 3 RTCCLKs for the bit to be cleared when a 1 is written to the bit to clear it. After writing a 1 to the NEWCENTURY_STS bit, software should also not exit the SMI handler until after the bit has been cleared. This is to make sure the SMI is not re-entered. BIOS Assumption: When booting, the BIOS checks the NEWCENTURY_STS bit. If set, the BIOS should increment the value in the RTC RAM register associated with the century. The BIOS should then clear the NEWCENTURY_STS bit. This scenario would occur if the system was asleep when the century rolls over. If the system is in an S0 state (not sleeping) and the SMI# occurs with the NEWCENTURY_STS bit sets, the SMI handler should increment the value in the RTC RAM register and clear the NEWCENTURY_STS bit.
6:4	0h RO	**Reserved**
3	0h RW/1C	**TIMEOUT:** Bit set to 1 by Intel PCH to indicate that the SMI was caused by TCO timer reaching 0. Note: The SMI handler should clear this bit to prevent an immediate re-entry to the SMI handler.
2	0h RW/1C	**TCO_INT_STS:** Bit set to 1 when SMI handler caused the interrupt by writing to the TCO_DAT_OUT register.
1	0h RW/1C	**OS_TCO_SMI:** Bit set to 1 when OS code caused an SMI# by writing to the TCO_DAT_IN register.
0	0h RO/V	**NMI2SMI_STS:** The Intel PCH sets read-only this bit when an SMI# occurs because an event occurred that would otherwise have caused an NMI. The NMI2SMI_STS bit should not be sticky bit. It should be a simple OR gate to indicate that one of the NMI sources has caused the SMI#. Each of the NMI sources already has its own sticky bit feeding the OR gate. Writes to this bit have no effect.

27.1.5 TCO2_STS Register (TSTS2) - Offset 6h

TCO2_STS Register

Type	Size	Offset	Default
IO	16 bit	SMBus TCO + 6h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:5	0h RO	**Reserved**
4	0h RW/1C	**SMLINK_SLAVE_SMI_STS:** Intel PCH will set this bit to 1 when it receives the SMI message (encoding 08h in the command type) on the SMLinks Slave Interface. Software clears the bit by writing a 1 to this bit position. This bit is in the resume well. It is reset by RSMRST#, but not by the PCI Reset associated with exit from S3-S5 states. This allows the software (presumably BIOS) to get the interrupt, see this new bit set, and decidedly go into the pre-determined (by local policy) sleep state. The advantage here is that race conditions are eliminated if the bit is only meant for power-down instead of potentially being meant for power-up or power-down depending on the current state (like the real power button).
3	0h RO	**Reserved**
2	0h RO/V	**NRSTRAP_STS:** This bit reflects the state of the No_Reboot strap that is sampled on PWROK rise.
1	0h RW/1C	**SECOND_TO_STS:** Intel PCH sets this bit to 1 to indicate that the TIMEOUT bit had been (or is currently) set and a second timeout occurred before the TCO_RLD register was written. If this bit is set and the NO_REBOOT configuration bit is 0, then the Intel PCH will reboot the system after the second timeout. The reboot is done by asserting PLTRST#. This bit is only cleared by writing a 1 to this bit or by a RSMRST#.
0	0h RW/1C	**INTRD_DET:** Intruder Detect. Bit set to 1 by the Intel PCH to indicate that an intrusion was detected. This is latched. This bit is cleared by writing a 1 to this bit or by RTEST#. This bit is backed in the RTC Well. Note: This bit has a recovery time. After writing a 1 to this bit position (to clear it), the bit may be read back as a 1 for up 65 microseconds before it is read as a 0. Software must be aware of this recovery time when reading this bit after clearing it. Note: If the INTRUDER# signal is active when the software attempts to clear the INTRD_DET bit, the bit will remain as a 1, and the SMI# will be generated again immediately. The SMI handler can clear the INTRD_SEL bits to avoid further SMIs. However, if the INTRUDER# signals goes inactive and then active again, there will not be further SMIs (because the INTRD_SEL bits would select that no SMI# be generated). If the INTRUDER# signal goes inactive some point after the INTRD_DET bit is written as a 1, then the INTRD_DET signal will go to a 0 when INTRUDER# input signal goes inactive. Note that this is slightly different from a classic sticky bit, since most sticky bits would remain active indefinitely when the signal goes active and would immediately go inactive when a 1 is written to the bit.

27.1.6 TCO1_CNT Register (TCTL1) - Offset 8h

TCO1_CNT Register

Type	Size	Offset	Default
IO	16 bit	SMBus TCO + 8h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**Reserved**
12	0h RW	**TCO_LOCK:** When set to 1, this bit prevents writes from changing the TCO_EN bit (in offset 30h of Power Management I/O space). Once this bit is set to 1, it can not be cleared by software writing a 0 to this bit location. A core-well reset is required to change this bit from 1 to 0. This bit defaults to 0.
11	0h RW	**TCO_TMR_HALT:** 1 = The TCO timer will halt. It will not count, and thus cannot reach a value that would cause an SMI# or to cause the SECOND_TO_STS bit to be set. This will also prevent rebooting 0 = The TCO timer is enabled to count. This is the default
10	0h RO	**Reserved**
9	0h RW	**NMI2SMI_EN:** Setting this bit 1 forces all NMIs to instead cause an SMI#, and will be reported in the TCO1_STS register. NMI2SMI_EN bit is set AND the NMI_EN# bit is set to 0, the NMI# will be routed to cause an SMI#. No NMI will be caused. However, if the GBL_SMI_EN bit is not set, then no SMI# will be generated, either. If NMI2SMI_EN is set but the NMI_EN# bit is set to 1, then no NMI or SMI# will be generated. The following table shows the possible combinations: NMI_EN#, GBL_SMI_EN 00 No SMI# based on NMI events (since no SMI# at all because SMI_EN = 0) 01 SMI# will be caused based on NMI events 10 No SMI# at all because SMI_EN is 0 11 No SMI# based on NMI events because NMI_EN#=1
8	0h RW	**NMI_NOW:** Writing a 1 to this bit causes an NMI. This allows the BIOS or SMI handler to force entry to the NMI handler. The NMI handler is expected to clear this bit. Another NMI will not be generated until the bit is cleared by writing a 1 back to the same bit position.
7:1	0h RO	**Reserved**
0	0h RW	**NR_MSUS:** This bit reflects the No Reboot pin strap state. It is sampled high on PWROK. This bit may be set or cleared by software if the strap is sampled low but may not override the strap when it indicates No Reboot. When set, the TCO timer will count down and generate the SMI# on the first timeout, but will not reboot on the second timeout.

27.1.7 TCO2_CNT Register (TCTL2) - Offset Ah

TCO2_CNT Register

Type	Size	Offset	Default
IO	16 bit	SMBus TCO + Ah	0008h

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5:4	0h RW	**OS_POLICY:** OS-based software writes to these bits to select the policy that the BIOS will use after the platform resets due to the WDT. The following convention is recommended for the BIOS and OS: 00 Boot normally 01 Shut down 10 Do Not Load OS. Hold in pre-boot state and use LAN to determine next step 11 Reserved Implementation note: These are just scratched pad bits. They should not be reset when the TCO logic resets the platform due to Watchdog Timer.
3	1h RW	**SMB_ALERT_DISABLE:** Disables GP/SMBALERT# as an alert source for the heartbeats and the SMBus slave. At reset (RSMRST# pin assertion only), this bit is set and the muxed GP/SMBALERT# are disabled.
2:1	0h RW	**INTRD_SEL:** Selects the action to take if the INTRUDER# signal goes active. 11 Reserved 01 Interrupt (as selected by TCO_INT_SEL) 10 SMI# 00 INTRUDER# does not cause SMI# or interrupt
0	0h RO	**Reserved**

27.1.8 TCO Message Registers (TMSG) - Offset Ch

TCOBASE+0Ch (MSG1) TCOBASE+0Dh (MSG2)

BIOS can write into these registers to indicate its boot progress. The external micro-controller can read these registers to monitor the boot progress.

Type	Size	Offset	Default
IO	16 bit	SMBus TCO + Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RW	**TCO Message2 (MSG2):** TCO Message2
7:0	00h RW	**TCO Message1 (MSG1):** TCO Message1

27.1.9 TCO_WDSTATUS Register (TWDS) - Offset Eh

TCO_WDSTATUS Register

Type	Size	Offset	Default
IO	8 bit	SMBus TCO + Eh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**TCO_WDSTATUS Register (TWDS):** The BIOS or system management software can write into this register to indicate more details on the boot progress. The register will rest to 00h based on a RSMRST# (but not PCI Reset). The external microcontroller can read this register to monitor boot progress.

27.1.10 LEGACY_ELIM Register (LE) - Offset 10h

LEGACY_ELIM Register

Type	Size	Offset	Default
IO	8 bit	SMBus TCO + 10h	03h

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	1h RW	**IRQ12_CAUSE:** When software sets the bit to 1, IRQ12 will be high (asserted). When software sets the bit to 0, IRQ12 will be low (not asserted). Default for this bit is 1.
0	1h RW	**IRQ1_CAUSE:** When software sets the bit to 1, IRQ1 will be high (asserted). When software sets the bit to 0, IRQ1 will be low (not asserted). Default for this bit is 1.

27.1.11 TCO_TMR Register (TTMR) - Offset 12h

TCO_TMR Register

Type	Size	Offset	Default
IO	16 bit	SMBus TCO + 12h	0004h

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	**Reserved**
9:0	004h RW	**TCOTMR:** Value that is loaded into the timer each time the TCO_RLD register is written. Values of 0000h or 0001h will be ignored and should not be attempted. The timer is clocked at approximately 0.6 seconds, and thus allows timeouts ranging from 1.2 seconds to 613.8 seconds. Note: The timer has an error of +/- 1 tick (0.6s).

28 FIA Configuration

28.1 FIA Configuration Registers Summary

Table 28-1. Summary of FIA Configuration Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Common Control (CC)	00000000h
100h	4	PCIe Device Reference Clock Request Enable 1 (PDRCRE1)	00000000h
108h	4	PCIe Device Reference Clock Request Mapping 1 (PDRCRM1)	040C2040h
10Ch	4	PCIe Device Reference Clock Request Mapping 2 (PDRCRM2)	09207185h
110h	4	PCIe Device Reference Clock Request Mapping 3 (PDRCRM3)	00000000h
114h	4	PCIe Device Reference Clock Request Mapping 4 (PDRCRM4)	00000000h
118h	4	PCIe Device Reference Clock Request Mapping 5 (PDRCRM5)	00000000h
11Ch	4	PCIe Device Reference Clock Request Mapping 6 (PDRCRM6)	00000000h
120h	4	PCIe Device Reference Clock Request Mapping 7 (PDRCRM7)	00000000h
124h	4	PCIe Device Reference Clock Request Mapping 8 (PDRCRM8)	00000000h
300h	4	Lane Owner Status 1 (LOS1)	00000000h
304h	4	Lane Owner Status 2 (LOS2)	00000000h
308h	4	Lane Owner Status 3 (LOS3)	00000000h
30Ch	4	Lane Owner Status 4 (LOS4)	00000000h
310h	4	Lane Owner Status 5 (LOS5)	00000000h

28.1.1 Common Control (CC) - Offset 0h

Common Control

Type	Size	Offset	Default
MMIO	32 bit	FDCF0000h + 0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V/L	**Secured Register Lock (SRL):** Secured Register Lock (SRL): When this bit is set, all the secured registers listed down below, including the SRL bit itself, will be locked and will be Read-Only. The lock is only cleared by the reset. Software is expected to program all the registers listed down below then only set this bit to '1'. The following fields are locked by CC.SRL: *DRCRM* *DRCRE* Note: During VNN removal exit flow when register context is restored, this bit shall only be restored after *DRCRM* and *DRCRE* registers are restored. **Locked by:** CC.SRL
30:18	0h RO	**Reserved**
17	0h RO	**Partition/Trunk Oscillator Clock Gating Enable (PTOCGE):** Partition/Trunk Oscillator Clock Gating Enable (PTOCGE): Reserved.
16	0h RW	**Oscillator/Side Clock Dynamic Clock Gating Enable (OSCDCGE):** Oscillator/Side Clock Dynamic Clock Gating Enable (OSCDCGE): When set, the oscillator and Side clock will be dynamically clock gated locally when the conditions to clock gate are met. When clear, the oscillator and Side clock will never be dynamically clock gated. If FC1.CDCGDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. Register Attribute: Static
15	0h RW	**Side Clock Partition/Trunk Clock Gating Enable (SCPTCGE):** Side Clock Partition/Trunk Clock Gating Enable (SCPTCGE): When set, the Side Clock will be clock gated at the partition/trunk level when the conditions to clock gate are met. When clear, the Side Clock will never be clock gated at the partition/trunk level. If FC1.CDCGDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. Register Attribute: Static
14:2	0h RO	**Reserved**
1:0	0h RW	**IOSF Sideband ISM Idle Counter (SBIC):** IOSF Sideband ISM Idle Counter (SBIC): This register provides configuration flexibility to govern when the IOSF sideband ISM transitions to IDLE_REQ state with respect to sideband interface idle. 00b: IOSF sideband ISM will transition to IDLE_REQ after 16 clocks of idle on sideband interface. 01b: IOSF sideband ISM will transition to IDLE_REQ after 31 clocks of idle on sideband interface. 10b: IOSF sideband ISM will transition to IDLE_REQ after 64 clocks of idle on sideband interface. 11b: IOSF sideband ISM will never transition to IDLE_REQ on sideband interface. Register Attribute: Dynamic

28.1.2 PCIe Device Reference Clock Request Enable 1 (PDRCRE1) - Offset 100h

PCIe Device Reference Clock Request Enable 1

Type	Size	Offset	Default
MMIO	32 bit	FDCF0000h + 100h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Express Port 31 CLKREQ Mapping Enable (P31CKRQME):** Express Port 31 CLKREQ Mapping Enable (P31CKRQME): Reserved.
30	0h RO	**Express Port 30 CLKREQ Mapping Enable (P30CKRQME):** Express Port 30 CLKREQ Mapping Enable (P30CKRQME): Reserved.
29	0h RO	**Express Port 29 CLKREQ Mapping Enable (P29CKRQME):** Express Port 29 CLKREQ Mapping Enable (P29CKRQME): Reserved.
28	0h RO	**Express Port 28 CLKREQ Mapping Enable (P28CKRQME):** Express Port 28 CLKREQ Mapping Enable (P28CKRQME): Reserved.
27	0h RO	**Express Port 27 CLKREQ Mapping Enable (P27CKRQME):** Express Port 27 CLKREQ Mapping Enable (P27CKRQME): Reserved.
26	0h RO	**Express Port 26 CLKREQ Mapping Enable (P26CKRQME):** Express Port 26 CLKREQ Mapping Enable (P26CKRQME): Reserved.
25	0h RO	**Express Port 25 CLKREQ Mapping Enable (P25CKRQME):** Express Port 25 CLKREQ Mapping Enable (P25CKRQME): Reserved.
24	0h RO	**Express Port 24 CLKREQ Mapping Enable (P24CKRQME):** Express Port 24 CLKREQ Mapping Enable (P24CKRQME): Reserved.
23	0h RO	**Express Port 23 CLKREQ Mapping Enable (P23CKRQME):** Express Port 23 CLKREQ Mapping Enable (P23CKRQME): Reserved.
22	0h RO	**Express Port 22 CLKREQ Mapping Enable (P22CKRQME):** Express Port 22 CLKREQ Mapping Enable (P22CKRQME): Reserved.
21	0h RO	**Express Port 21 CLKREQ Mapping Enable (P21CKRQME):** Express Port 21 CLKREQ Mapping Enable (P21CKRQME): Reserved.
20	0h RO	**Express Port 20 CLKREQ Mapping Enable (P20CKRQME):** Express Port 20 CLKREQ Mapping Enable (P20CKRQME): Reserved.
19	0h RO	**Express Port 19 CLKREQ Mapping Enable (P19CKRQME):** Express Port 19 CLKREQ Mapping Enable (P19CKRQME): Reserved.
18	0h RO	**Express Port 18 CLKREQ Mapping Enable (P18CKRQME):** Express Port 18 CLKREQ Mapping Enable (P18CKRQME): Reserved.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**Express Port 17 CLKREQ Mapping Enable (P17CKRQME):** Express Port 17 CLKREQ Mapping Enable (P17CKRQME): Reserved.
16	0h RO	**Express Port 16 CLKREQ Mapping Enable (P16CKRQME):** Express Port 16 CLKREQ Mapping Enable (P16CKRQME): Reserved.
15	0h RO	**Express Port 15 CLKREQ Mapping Enable (P15CKRQME):** Express Port 15 CLKREQ Mapping Enable (P15CKRQME): Reserved.
14	0h RO	**Express Port 14 CLKREQ Mapping Enable (P14CKRQME):** Express Port 14 CLKREQ Mapping Enable (P14CKRQME): Reserved.
13	0h RO	**Express Port 13 CLKREQ Mapping Enable (P13CKRQME):** Express Port 13 CLKREQ Mapping Enable (P13CKRQME): Reserved.
12	0h RO	**Express Port 12 CLKREQ Mapping Enable (P12CKRQME):** Express Port 12 CLKREQ Mapping Enable (P12CKRQME): Reserved.
11	0h RO	**Express Port 11 CLKREQ Mapping Enable (P11CKRQME):** Express Port 11 CLKREQ Mapping Enable (P11CKRQME): Reserved.
10	0h RO	**Express Port 10 CLKREQ Mapping Enable (P10CKRQME):** Express Port 10 CLKREQ Mapping Enable (P10CKRQME): Reserved.
9	0h RW/L	**Express Port 9 CLKREQ Mapping Enable (P9CKRQME):** Express Port 9 CLKREQ Mapping Enable (P9CKRQME): Similar to register PDRCRE1.P1CKRQME but this register is for Express Port 9. **Locked by:** CC.SRL
8	0h RW/L	**Express Port 8 CLKREQ Mapping Enable (P8CKRQME):** Express Port 8 CLKREQ Mapping Enable (P8CKRQME): Similar to register PDRCRE1.P1CKRQME but this register is for Express Port 8. **Locked by:** CC.SRL
7	0h RW/L	**Express Port 7 CLKREQ Mapping Enable (P7CKRQME):** Express Port 7 CLKREQ Mapping Enable (P7CKRQME): Similar to register PDRCRE1.P1CKRQME but this register is for Express Port 7. **Locked by:** CC.SRL
6	0h RW/L	**Express Port 6 CLKREQ Mapping Enable (P6CKRQME):** Express Port 6 CLKREQ Mapping Enable (P6CKRQME): Similar to register PDRCRE1.P1CKRQME but this register is for Express Port 6. **Locked by:** CC.SRL
5	0h RW/L	**Express Port 5 CLKREQ Mapping Enable (P5CKRQME):** Express Port 5 CLKREQ Mapping Enable (P5CKRQME): Similar to register PDRCRE1.P1CKRQME but this register is for Express Port 5. **Locked by:** CC.SRL
4	0h RW/L	**Express Port 4 CLKREQ Mapping Enable (P4CKRQME):** Express Port 4 CLKREQ Mapping Enable (P4CKRQME): Similar to register PDRCRE1.P1CKRQME but this register is for Express Port 4. **Locked by:** CC.SRL

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/L	**Express Port 3 CLKREQ Mapping Enable (P3CKRQME):** Express Port 3 CLKREQ Mapping Enable (P3CKRQME): Similar to register PDRCRE1.P1CKRQME but this register is for Express Port 3. **Locked by:** CC.SRL
2	0h RW/L	**Express Port 2 CLKREQ Mapping Enable (P2CKRQME):** Express Port 2 CLKREQ Mapping Enable (P2CKRQME): Similar to register PDRCRE1.P0CKRQME but this register is for Express Port 2. **Locked by:** CC.SRL
1	0h RW/L	**Express Port 1 CLKREQ Mapping Enable (P1CKRQME):** Express Port 1 CLKREQ Mapping Enable (P1CKRQME): The mapping of Express Port 1 to the corresponding CLKREQ# pin is configured by this field. '1' means this Express Port has the CLKREQ pin presence and the corresponding register for Express Port 1, i.e. PDRMCRM*.P1CKRQM will indicates which CLKREQ# pin the Express Port is mapped to, '0' means not presence and will be masked to a de-asserted state. This register bit is Read-Only when the CC.SRL bit is set. **Locked by:** CC.SRL
0	0h RW/L	**Express Port 0 CLKREQ Mapping Enable (P0CKRQME):** Express Port 0 CLKREQ Mapping Enable (P0CKRQME): The mapping of Express Port 0 to the corresponding CLKREQ# pin is configured by this field. '1' means this Express Port has the CLKREQ pin presence and the corresponding register for Express Port 0, i.e. PDRMCRM*.P1CKRQM will indicates which CLKREQ# pin the Express Port is mapped to, '0' means not presence and will be masked to a de-asserted state. This register bit is Read-Only when the CC.SRL bit is set. **Locked by:** CC.SRL

28.1.3 PCIe Device Reference Clock Request Mapping 1 (PDRCRM1) - Offset 108h

PCIe Device Reference Clock Request Mapping 1

Type	Size	Offset	Default
MMIO	32 bit	FDCF0000h + 108h	040C2040h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:24	04h RW/L	**Express Port 4 CLKREQ Mapping (P4CKRQM):** Express Port 4 CLKREQ Mapping (P4CKRQM): Similar to register DRCRM1.P1CKRQM but this register is for Express Port 4. **Locked by:** CC.SRL
23	0h RO	**Reserved**
22:18	03h RW/L	**Express Port 3 CLKREQ Mapping (P3CKRQM):** Express Port 3 CLKREQ Mapping (P3CKRQM): Similar to register DRCRM1.P1CKRQM but this register is for Express Port 3. **Locked by:** CC.SRL

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**Reserved**
16:12	02h RW/L	**Express Port 2 CLKREQ Mapping (P2CKRQM):** Express Port 2 CLKREQ Mapping (P2CKRQM): Similar to register DRCRM1.P0CKRQM but this register is for Express Port 2. **Locked by:** CC.SRL
11	0h RO	**Reserved**
10:6	01h RW/L	**Express Port 1 CLKREQ Mapping (P1CKRQM):** Express Port 1 CLKREQ Mapping (P1CKRQM): The mapping of PCH Express Port 1 to the corresponding CLKREQ# pin is configured by this field. This register is only valid if the corresponding register for Express Port 1, i.e. PDRCRE*.P1CKRQME=1. '00h': Express Port 1 maps to CLKREQ0# pin '01h': Express Port 1 maps to CLKREQ1# pin : : '1Dh': Express Port 1 maps to CLKREQ29# pin '1Eh': Express Port 1 maps to CLKREQ30# pin '1Fh': Express Port 1 maps to CLKREQ31# pin Software must never map multiple PCH Express Ports and CPU Express Ports using PDRCRM* and CPDRCRM* registers to the same CLKREQ# pin. The hardware behavior is undefined if this ever happens. This field must be configured prior to enabling any power management features. For SoC with less than 32 CLKREQ# supported for PCIe, configuring this field to map to any unsupported CLKREQ# pins may result in undefined hardware behavior. This register bit is Read-Only when the CC.SRL bit is set. Register Attribute: Static **Locked by:** CC.SRL
5	0h RO	**Reserved**
4:0	00h RW/L	**Express Port 0 CLKREQ Mapping (P0CKRQM):** Express Port 0 CLKREQ Mapping (P0CKRQM): The mapping of PCH Express Port 0 to the corresponding CLKREQ# pin is configured by this field. This register is only valid if the corresponding register for Express Port 0, i.e. PDRCRE*.P0CKRQME=1. '00h': Express Port 0 maps to CLKREQ0# pin '01h': Express Port 0 maps to CLKREQ1# pin : : '1Dh': Express Port 0 maps to CLKREQ29# pin '1Eh': Express Port 0 maps to CLKREQ30# pin '1Fh': Express Port 0 maps to CLKREQ31# pin Software must never map multiple PCH Express Ports and CPU Express Ports using PDRCRM* and CPDRCRM* registers to the same CLKREQ# pin. The hardware behavior is undefined if this ever happens. This field must be configured prior to enabling any power management features. For SoC with less than 32 CLKREQ# supported for PCIe, configuring this field to map to any unsupported CLKREQ# pins may result in undefined hardware behavior. This register bit is Read-Only when the CC.SRL bit is set. Register Attribute: Static **Locked by:** CC.SRL

28.1.4 PCIe Device Reference Clock Request Mapping 2 (PDRCRM2) - Offset 10Ch

PCIe Device Reference Clock Request Mapping 2

Type	Size	Offset	Default
MMIO	32 bit	FDCF0000h + 10Ch	09207185h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:24	09h RW/L	**Express Port 9 CLKREQ Mapping (P9CKRQM):** Express Port 9 CLKREQ Mapping (P9CKRQM): Similar to register DRCRM1.P1CKRQM but this register is for Express Port 9. **Locked by:** CC.SRL
23	0h RO	**Reserved**
22:18	08h RW/L	**Express Port 8 CLKREQ Mapping (P8CKRQM):** Express Port 8 CLKREQ Mapping (P8CKRQM): Similar to register DRCRM1.P1CKRQM but this register is for Express Port 8. **Locked by:** CC.SRL
17	0h RO	**Reserved**
16:12	07h RW/L	**Express Port 7 CLKREQ Mapping (P7CKRQM):** Express Port 7 CLKREQ Mapping (P7CKRQM): Similar to register DRCRM1.P1CKRQM but this register is for Express Port 7. **Locked by:** CC.SRL
11	0h RO	**Reserved**
10:6	06h RW/L	**Express Port 6 CLKREQ Mapping (P6CKRQM):** Express Port 6 CLKREQ Mapping (P6CKRQM): Similar to register DRCRM1.P1CKRQM but this register is for Express Port 6. **Locked by:** CC.SRL
5	0h RO	**Reserved**
4:0	05h RW/L	**Express Port 5 CLKREQ Mapping (P5CKRQM):** Express Port 5 CLKREQ Mapping (P5CKRQM): Similar to register DRCRM1.P1CKRQM but this register is for Express Port 5. **Locked by:** CC.SRL

28.1.5 PCIe Device Reference Clock Request Mapping 3 (PDRCRM3) - Offset 110h

PCIe Device Reference Clock Request Mapping 3

Type	Size	Offset	Default
MMIO	32 bit	FDCF0000h + 110h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:24	00h RO	**Express Port 14 CLKREQ Mapping (P14CKRQM):** Express Port 14 CLKREQ Mapping (P14CKRQM): Reserved.
23	0h RO	**Reserved**
22:18	00h RO	**Express Port 13 CLKREQ Mapping (P13CKRQM):** Express Port 13 CLKREQ Mapping (P13CKRQM): Reserved.
17	0h RO	**Reserved**
16:12	00h RO	**Express Port 12 CLKREQ Mapping (P12CKRQM):** Express Port 12 CLKREQ Mapping (P12CKRQM): Reserved.
11	0h RO	**Reserved**
10:6	00h RO	**Express Port 11 CLKREQ Mapping (P11CKRQM):** Express Port 11 CLKREQ Mapping (P11CKRQM): Reserved.
5	0h RO	**Reserved**
4:0	00h RO	**Express Port 10 CLKREQ Mapping (P10CKRQM):** Express Port 10 CLKREQ Mapping (P10CKRQM): Reserved.

28.1.6 PCIe Device Reference Clock Request Mapping 4 (PDRCRM4) - Offset 114h

PCIe Device Reference Clock Request Mapping 4

Type	Size	Offset	Default
MMIO	32 bit	FDCF0000h + 114h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:24	00h RO	**Express Port 19 CLKREQ Mapping (P19CKRQM):** Express Port 19 CLKREQ Mapping (P19CKRQM): Reserved.
23	0h RO	**Reserved**
22:18	00h RO	**Express Port 18 CLKREQ Mapping (P18CKRQM):** Express Port 18 CLKREQ Mapping (P18CKRQM): Reserved.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**Reserved**
16:12	00h RO	**Express Port 17 CLKREQ Mapping (P17CKRQM):** Express Port 17 CLKREQ Mapping (P17CKRQM): Reserved.
11	0h RO	**Reserved**
10:6	00h RO	**Express Port 16 CLKREQ Mapping (P16CKRQM):** Express Port 16 CLKREQ Mapping (P16CKRQM): Reserved.
5	0h RO	**Reserved**
4:0	00h RO	**Express Port 15 CLKREQ Mapping (P15CKRQM):** Express Port 15 CLKREQ Mapping (P15CKRQM): Reserved.

28.1.7 PCIe Device Reference Clock Request Mapping 5 (PDRCRM5) - Offset 118h

PCIe Device Reference Clock Request Mapping 5

Type	Size	Offset	Default
MMIO	32 bit	FDCF0000h + 118h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:24	00h RO	**Express Port 24 CLKREQ Mapping (P24CKRQM):** Express Port 24 CLKREQ Mapping (P24CKRQM): Reserved.
23	0h RO	**Reserved**
22:18	00h RO	**Express Port 23 CLKREQ Mapping (P23CKRQM):** Express Port 23 CLKREQ Mapping (P23CKRQM): Reserved.
17	0h RO	**Reserved**
16:12	00h RO	**Express Port 22 CLKREQ Mapping (P22CKRQM):** Express Port 22 CLKREQ Mapping (P22CKRQM): Reserved.
11	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
10:6	00h RO	**Express Port 21 CLKREQ Mapping (P21CKRQM):** Express Port 21 CLKREQ Mapping (P21CKRQM): Reserved.
5	0h RO	**Reserved**
4:0	00h RO	**Express Port 20 CLKREQ Mapping (P20CKRQM):** Express Port 20 CLKREQ Mapping (P20CKRQM): Reserved.

28.1.8 PCIe Device Reference Clock Request Mapping 6 (PDRCRM6) - Offset 11Ch

PCIe Device Reference Clock Request Mapping 6

Type	Size	Offset	Default
MMIO	32 bit	FDCF0000h + 11Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:24	00h RO	**Express Port 29 CLKREQ Mapping (P29CKRQM):** Express Port 29 CLKREQ Mapping (P29CKRQM): Reserved.
23	0h RO	**Reserved**
22:18	00h RO	**Express Port 28 CLKREQ Mapping (P28CKRQM):** Express Port 28 CLKREQ Mapping (P28CKRQM): Reserved.
17	0h RO	**Reserved**
16:12	00h RO	**Express Port 27 CLKREQ Mapping (P27CKRQM):** Express Port 27 CLKREQ Mapping (P27CKRQM): Reserved.
11	0h RO	**Reserved**
10:6	00h RO	**Express Port 26 CLKREQ Mapping (P26CKRQM):** Express Port 26 CLKREQ Mapping (P26CKRQM): Reserved.
5	0h RO	**Reserved**
4:0	00h RO	**Express Port 25 CLKREQ Mapping (P25CKRQM):** Express Port 25 CLKREQ Mapping (P25CKRQM): Reserved.

28.1.9 PCIe Device Reference Clock Request Mapping 7 (PDRCRM7) - Offset 120h

PCIe Device Reference Clock Request Mapping 7

Type	Size	Offset	Default
MMIO	32 bit	FDCF0000h + 120h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:24	00h RO	**Express Port 34 CLKREQ Mapping (P34CKRQM):** Express Port 34 CLKREQ Mapping (P34CKRQM): Reserved.
23	0h RO	**Reserved**
22:18	00h RO	**Express Port 33 CLKREQ Mapping (P33CKRQM):** Express Port 33 CLKREQ Mapping (P33CKRQM): Reserved.
17	0h RO	**Reserved**
16:12	00h RO	**Express Port 32 CLKREQ Mapping (P32CKRQM):** Express Port 32 CLKREQ Mapping (P32CKRQM): Reserved.
11	0h RO	**Reserved**
10:6	00h RO	**Express Port 31 CLKREQ Mapping (P31CKRQM):** Express Port 31 CLKREQ Mapping (P31CKRQM): Reserved.
5	0h RO	**Reserved**
4:0	00h RO	**Express Port 30 CLKREQ Mapping (P30CKRQM):** Express Port 30 CLKREQ Mapping (P30CKRQM): Reserved.

28.1.10 PCIe Device Reference Clock Request Mapping 8 (PDRCRM8) - Offset 124h

PCIe Device Reference Clock Request Mapping 8

Type	Size	Offset	Default
MMIO	32 bit	FDCF0000h + 124h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:24	00h RO	**Express Port 39 CLKREQ Mapping (P39CKRQM):** Express Port 39 CLKREQ Mapping (P39CKRQM): Reserved.
23	0h RO	**Reserved**
22:18	00h RO	**Express Port 38 CLKREQ Mapping (P38CKRQM):** Express Port 38 CLKREQ Mapping (P38CKRQM): Reserved.
17	0h RO	**Reserved**
16:12	00h RO	**Express Port 37 CLKREQ Mapping (P37CKRQM):** Express Port 37 CLKREQ Mapping (P37CKRQM): Reserved.
11	0h RO	**Reserved**
10:6	00h RO	**Express Port 36 CLKREQ Mapping (P36CKRQM):** Express Port 36 CLKREQ Mapping (P36CKRQM): Reserved.
5	0h RO	**Reserved**
4:0	00h RO	**Express Port 35 CLKREQ Mapping (P35CKRQM):** Express Port 35 CLKREQ Mapping (P35CKRQM): Reserved.

28.1.11 Lane Owner Status 1 (LOS1) - Offset 300h

Lane Owner Status 1

Type	Size	Offset	Default
MMIO	32 bit	FDCF0000h + 300h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO/V	**Lane 7 Owner (L7O):** Lane 7 Owner (L7O): Similar to register LOS1.L0O but this register is for PHY Lane 7.
27:24	0h RO/V	**Lane 6 Owner (L6O):** Lane 6 Owner (L6O): Similar to register LOS1.L0O but this register is for PHY Lane 6.
23:20	0h RO/V	**Lane 5 Owner (L5O):** Lane 5 Owner (L5O): Similar to register LOS1.L0O but this register is for PHY Lane 5.

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RO/V	**Lane 4 Owner (L4O):** Lane 4 Owner (L4O): Similar to register LOS1.L0O but this register is for PHY Lane 4.
15:12	0h RO/V	**Lane 3 Owner (L3O):** Lane 3 Owner (L3O): Similar to register LOS1.L0O but this register is for PHY Lane 3.
11:8	0h RO/V	**Lane 2 Owner (L2O):** Lane 2 Owner (L2O): Similar to register LOS1.L0O but this register is for PHY Lane 2.
7:4	0h RO/V	**Lane 1 Owner (L1O):** Lane 1 Owner (L1O): This register indicates the lane owner for PHY Lane 1. 0h: PCIe/DMI 1h: USB3 2h: SATA 3h: GbE 4h: Reserved 5h: Reserved 6h: Reserved 7h: Reserved 8h: Display Port/PCIe4th 9h: Thunderbolt/PCIe3rd Ah: HTI Bh: TSN GbE Ch: PCIe2nd Dh-Eh: Reserved Fh: No Owner (If statically assigned to 'No Owner' then PHY power state is PS2-Reset. If dynamically assigned to 'No Owner' then PHY power state is USB3 Idle state, i.e. PS3) Implementation Note: This register has no hardware functional use for FIA.
3:0	0h RO/V	**Lane 0 Owner (L0O):** Lane 0 Owner (L0O): This register indicates the lane owner for PHY Lane 0. 0h: PCIe/DMI 1h: USB3 2h: SATA 3h: GbE 4h: Reserved 5h: Reserved 6h: Reserved 7h: Reserved 8h: Display Port/PCIe4th 9h: Thunderbolt/PCIe3rd Ah: HTI Bh: TSN GbE Ch: PCIe2nd Dh-Eh: Reserved Fh: No Owner (If statically assigned to 'No Owner' then PHY power state is PS2-Reset. If dynamically assigned to 'No Owner' then PHY power state is USB3 Idle state, i.e. PS3) Implementation Note: This register has no hardware functional use for FIA.

28.1.12 Lane Owner Status 2 (LOS2) - Offset 304h

Lane Owner Status 2

Type	Size	Offset	Default
MMIO	32 bit	FDCF0000h + 304h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Lane 15 Owner (L15O):** Lane 15 Owner (L15O): Reserved.
27:24	0h RO	**Lane 14 Owner (L14O):** Lane 14 Owner (L14O): Reserved.
23:20	0h RO	**Lane 13 Owner (L13O):** Lane 13 Owner (L13O): Reserved.
19:16	0h RO	**Lane 12 Owner (L12O):** Lane 12 Owner (L12O): Reserved.
15:12	0h RO/V	**Lane 11 Owner (L11O):** Lane 11 Owner (L11O): Similar to register LOS1.L0O but this register is for PHY Lane 11.
11:8	0h RO/V	**Lane 10 Owner (L10O):** Lane 10 Owner (L10O): Similar to register LOS1.L0O but this register is for PHY Lane 10.
7:4	0h RO/V	**Lane 9 Owner (L9O):** Lane 9 Owner (L9O): Similar to register LOS1.L0O but this register is for PHY Lane 9.
3:0	0h RO/V	**Lane 8 Owner (L8O):** Lane 8 Owner (L8O): Similar to register LOS1.L0O but this register is for PHY Lane 8.

28.1.13 Lane Owner Status 3 (LOS3) - Offset 308h

Lane Owner Status 3

Type	Size	Offset	Default
MMIO	32 bit	FDCF0000h + 308h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Lane 23 Owner (L23O):** Lane 23 Owner (L23O): Reserved.
27:24	0h RO	**Lane 22 Owner (L22O):** Lane 22 Owner (L22O): Reserved.
23:20	0h RO	**Lane 21 Owner (L21O):** Lane 21 Owner (L21O): Reserved.
19:16	0h RO	**Lane 20 Owner (L20O):** Lane 20 Owner (L20O): Reserved.
15:12	0h RO	**Lane 19 Owner (L19O):** Lane 19 Owner (L19O): Reserved.
11:8	0h RO	**Lane 18 Owner (L18O):** Lane 18 Owner (L18O): Reserved.
7:4	0h RO	**Lane 17 Owner (L17O):** Lane 17 Owner (L17O): Reserved.
3:0	0h RO	**Lane 16 Owner (L16O):** Lane 16 Owner (L16O): Reserved.

28.1.14 Lane Owner Status 4 (LOS4) - Offset 30Ch

Lane Owner Status 4

Type	Size	Offset	Default
MMIO	32 bit	FDCF0000h + 30Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Lane 31 Owner (L31O):** Lane 31 Owner (L31O): Reserved.
27:24	0h RO	**Lane 30 Owner (L30O):** Lane 30 Owner (L30O): Reserved.
23:20	0h RO	**Lane 29 Owner (L29O):** Lane 29 Owner (L29O): Reserved.
19:16	0h RO	**Lane 28 Owner (L28O):** Lane 28 Owner (L28O): Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Lane 27 Owner (L27O):** Lane 27 Owner (L27O): Reserved.
11:8	0h RO	**Lane 26 Owner (L26O):** Lane 26 Owner (L26O): Reserved.
7:4	0h RO	**Lane 25 Owner (L25O):** Lane 25 Owner (L25O): Reserved.
3:0	0h RO	**Lane 24 Owner (L24O):** Lane 24 Owner (L24O): Reserved.

28.1.15 Lane Owner Status 5 (LOS5) - Offset 310h

Lane Owner Status 5

Type	Size	Offset	Default
MMIO	32 bit	FDCF0000h + 310h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Lane 39 Owner (L39O):** Lane 39 Owner (L39O): Reserved.
27:24	0h RO	**Lane 38 Owner (L38O):** Lane 38 Owner (L38O): Reserved.
23:20	0h RO	**Lane 37 Owner (L37O):** Lane 37 Owner (L37O): Reserved.
19:16	0h RO	**Lane 36 Owner (L36O):** Lane 36 Owner (L36O): Reserved.
15:12	0h RO	**Lane 35 Owner (L35O):** Lane 35 Owner (L35O): Reserved.
11:8	0h RO	**Lane 34 Owner (L34O):** Lane 34 Owner (L34O): Reserved.
7:4	0h RO	**Lane 33 Owner (L33O):** Lane 33 Owner (L33O): Reserved.
3:0	0h RO	**Lane 32 Owner (L32O):** Lane 32 Owner (L32O): Reserved.

29 On Package DMI (OPDMI)

This chapter documents OPDMI Registers.

29.1 OPDMI Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 29-1. Summary of OPDMI Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2014h	4	Virtual Channel 0 Resource Control (V0CTL)	80000000h
201Ah	2	Virtual Channel 0 Resource Status (V0STS)	0000h
2020h	4	Virtual Channel 1 Resource Control (V1CTL)	00000000h
2026h	2	Virtual Channel 1 Resource Status (V1STS)	0000h
2040h	4	ME Virtual Channel (VCm) Resource Control (VMCTL)	00000000h
2046h	2	ME Virtual Channel Resource Status (VMSTS)	0000h
2084h	4	Uncorrectable Error Status (UES)	00000000h
2088h	4	Uncorrectable Error Mask (UEM)	00000000h
208Ch	4	Uncorrectable Error Severity (UEV)	00000000h
2090h	4	Correctable Error Status (CES)	00000000h
2094h	4	Correctable Error Mask (CEM)	00002000h
20ACh	4	Root Error Command (REC)	00000000h
20B0h	4	Root Error Status (RES)	00000000h
20B4h	4	Error Source Identification (ESID)	00000000h
2234h	4	DMI Control Register (Common) (DMIC)	08000000h
223Ch	4	IOSF Primary Control And Status (Common) (IPCS_IOSFSBCS)	000C0000h
2608h	4	Target Link Speed (TLS)	00000002h
2618h	4	Link Configuration (LCFG)	00330031h
2730h	4	LPC Generic I/O Range 1 (LPCLGIR1)	00000000h
2734h	4	LPC Generic I/O Range 2 (LPCLGIR2)	00000000h
2738h	4	LPC Generic I/O Range 3 (LPCLGIR3)	00000000h
273Ch	4	LPC Generic I/O Range 4 (LPCLGIR4)	00000000h
2740h	4	LPC Generic Memory Range (LPCGMR)	00000000h
2744h	4	LPC BIOS Decode Enable (LPCBDE)	0000FFCFh
2748h	4	uCode Patch Region (UCPR)	00000001h
274Ch	4	General Control and Status (GCS)	00000000h
2750h	4	I/O Trap Register 1 - Lower DW (IOT1_LOW)	00000000h
2754h	4	I/O Trap Register 1 - Upper DW (IOT1_HIGH)	00000000h
2770h	4	LPC I/O Decode Ranges (LPCIOD)	00000000h
2774h	4	LPC I/O Enables (LPCIOE)	00000000h
2778h	4	TCO Base Address (TCOBASE)	00000001h
277Ch	4	General Purpose Memory Range 1 (GPMR1)	00000000h
2780h	4	General Purpose Memory Range 1 Destination ID (GPMR1DID)	00000000h
27ACh	4	PM Base Address (PMBASEA)	00000000h
27B0h	4	PM Base Control (PMBASEC)	00000000h
27B4h	4	ACPI Base Address (ACPIBA)	00000000h
27B8h	4	ACPI Base Destination ID (ACPIBDID)	00000000h

29.1.1 Virtual Channel 0 Resource Control (V0CTL) — Offset

2014h

Virtual Channel 0 Resource Control

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 2014h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**Virtual Channel Enable (EN):** Enables the VC when set. Disables the VC when cleared.
30:27	0h RO	**Reserved**
26:24	0h RO	**Virtual Channel Identifier (ID):** Indicates the ID to use for this virtual channel
23:16	0h RO	**Reserved**
15:10	00h RW/L	**Extended TC/VC Map (ETVM):** Defines the upper 8-bits of the VC0 16-bit TC/VC mapping registers. These registers use the PCI reserved TC[3] traffic class bit. This register is Read-Only if DMIC.SRL field is set. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
9:7	0h RO	**Reserved**
6:1	00h RW/L	**Transaction Class / Virtual Channel Map (TVM):** Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel. This register is Read-Only if DMIC.SRL field is set. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
0	0h RO	**Reserved**

29.1.2 Virtual Channel 0 Resource Status (V0STS) — Offset 201Ah

Virtual Channel 0 Resource Status

Type	Size	Offset	Default
MMIO	16 bit	FD880000h + 201Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**
1	0h RO/V	**VC Negotiation Pending (NP):** When set, indicates the virtual channel is still being negotiated with ingress ports.
0	0h RO	**Reserved**

29.1.3 Virtual Channel 1 Resource Control (V1CTL) — Offset 2020h

Virtual Channel 1 Resource Control

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 2020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Virtual Channel Enable (EN):** Enables the VC when set. Disables the VC when cleared. This register is Read-Only if the DMIC.SRL field is set. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
30:28	0h RO	**Reserved**
27:24	0h RW/L	**Virtual Channel Identifier (ID):** Indicates the ID to use for this virtual channel BIOS is required to program VCID[3] to 0 when operating at DMI2. This register is Read-Only if the DMIC.SRL field is set. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
23:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15:10	00h RW/L	**Extended TC/VC Map (ETVM):** Defines the upper 8-bits of the VC1 16-bit TC/VC mapping registers These registers use the PCIe reserved TC[3] traffic class bit. This register is Read-Only if the DMIC.SRL field is set. If VC1 is not enabled, the register output sent to the users of this register is forced to 0. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
9:8	0h RO	**Reserved**
7:1	00h RW/L	**Transaction Class / Virtual Channel Map (TVM):** Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel. This register is Read-Only if the DMIC.SRL field is set. If VC1 is not enabled, the register output sent to the users of this register is forced to 0. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
0	0h RO	**Reserved**

29.1.4 Virtual Channel 1 Resource Status (V1STS) — Offset 2026h

Virtual Channel 1 Resource Status

Note: Bit definitions are the same as V0STS, offset 201Ah.

29.1.5 ME Virtual Channel (VCm) Resource Control (VMCTL) — Offset 2040h

ME Virtual Channel (VCm) Resource Control

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 2040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Virtual Channel Enable (EN):** Enables the VC when set. Disables the VC when cleared. This register is Read-Only if the DMIC.SRL field is set. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
30:28	0h RO	**Reserved**
27:24	0h RW/L	**Virtual Channel Identifier (ID):** Indicates the ID to use for this virtual channel BIOS is required to program VCID[3] to 0 when operating at DMI2. This register is Read-Only if the DMIC.SRL field is set. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
23:16	0h RO	**Reserved**
15:10	00h RW/L	**Extended TC/VC Map (ETVM):** Defines the upper 8-bits of the VCm 16-bit TC/VC mapping registers. These registers use the PCIe reserved TC[3] traffic class bit. This register is Read-Only if the DMIC.SRL field is set. If VCm is not enabled, the register output sent to the users of this register is forced to 0. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
9:8	0h RO	**Reserved**
7:1	00h RW/L	**Transaction Class / Virtual Channel Map (TVM):** Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel. This register is Read-Only if the DMIC.SRL field is set. If VCm is not enabled, the register output sent to the users of this register is forced to 0. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
0	0h RO	**Reserved**

29.1.6 ME Virtual Channel Resource Status (VMSTS) — Offset 2046h

ME Virtual Channel Resource Status

Note: Bit definitions are the same as V0STS, offset 201Ah.

29.1.7 Uncorrectable Error Status (UES) — Offset 2084h

Uncorrectable Error Status

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 2084h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RW/1C/V/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received.
19	0h RO	**ECRC Error Status (EE):** ECRC is not supported.
18	0h RW/1C/V/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received.
17	0h RW/1C/V/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred.
16	0h RO	**Unexpected Completion Status (UC):** Reserved
15	0h RW/1C/V/P	**Completer Abort Status (CA):** Indicates a completer abort was received.
14	0h RO	**Completion Timeout Status (CT):** Reserved
13	0h RO	**Flow Control Protocol Error Status (FCPE):** Not supported.
12	0h RW/1C/V/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received.
11:5	0h RO	**Reserved**
4	0h RW/1C/V/P	**Data Link Protocol Error Status (DLPE):** Indicates a data link protocol error occurred.
3:1	0h RO	**Reserved**
0	0h RO	**Training Error Status (TE):** Not supported.

29.1.8 Uncorrectable Error Mask (UEM) — Offset 2088h

Uncorrectable Error Mask

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 2088h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors.
19	0h RO	**ECRC Error Mask (EE):** ECRC is not supported.
18	0h RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs
17	0h RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows.
16	0h RO	**Unexpected Completion Mask (UC):** Reserved
15	0h RW/P	**Completer Abort Mask (CM):** Mask for completer abort.
14	0h RO	**Completion Timeout Mask (CT):** Reserved
13	0h RO	**Flow Control Protocol Error Mask (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs.
11:5	0h RO	**Reserved**
4	0h RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors.
3:1	0h RO	**Reserved**
0	0h RO	**Training Error Mask (TE):** Not supported.

29.1.9 Uncorrectable Error Severity (UEV) — Offset 208Ch

Uncorrectable Error Severity

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 208Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception.
19	0h RO	**ECRC Error Severity (EE):** ECRC is not supported.
18	0h RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception.
17	0h RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences.
16	0h RO	**Unexpected Completion Severity (UC):** Reserved
15	0h RW/P	**Completer Abort Severity (CA):** Severity for completer.
14	0h RO	**Completion Timeout Severity (CT):** Reserved
13	0h RO	**Flow Control Protocol Error Severity (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception.
11:5	0h RO	**Reserved**
4	0h RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors.
3:1	0h RO	**Reserved**
0	0h RW/P	**Training Error Severity (TE):** TE not supported. This bit is RW for ease of implementation.

29.1.10 Correctable Error Status (CES) — Offset 2090h

Correctable Error Status

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 2090h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW/1C/V/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that a Advisory Non-Fatal Error occurred.
12	0h RW/1C/V/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out.
11:9	0h RO	**Reserved**
8	0h RW/1C/V/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over.
7	0h RW/1C/V/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received.
6	0h RW/1C/V/P	**Bad TLP Status (BT):** Indicates a bad TLP was received.
5:1	0h RO	**Reserved**
0	0h RW/1C/V/P	**Receiver Error Status (RE):** Indicates a receiver error occurred.

29.1.11 Correctable Error Mask (CEM) — Offset 2094h

Correctable Error Mask

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 2094h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	1h RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12	0h RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout.
11:9	0h RO	**Reserved**
8	0h RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover.
7	0h RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception.
6	0h RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception.
5:1	0h RO	**Reserved**
0	0h RW/P	**Receiver Error Mask (RE):** Mask for receiver errors.

29.1.12 Root Error Command (REC) — Offset 20ACh

Root Error Command

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 20ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Drop Poisoned Downstream Packets (DPDP):** When set to a '1', if downstream packet on DMI is received with the EP bit set, this packet and all downstream packets with data received on DMI for any VC will have their Unsupported Transaction (UT) attribute set causing them to be forwarded to the fabric Error Handler. When cleared to a '0', downstream packets from DMI with the EP bit set are forwarded onto the downstream backbone normally. This register is Read-Only if DMIC.SRL field is set. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
30	0h RW	**Unsupported Transaction Policy Bit (UTPB):** When set to '1', the Unsupported Transactions detected on DMI will not set the UES.URE bit. This subsequently ensures that SERR will never be signaled in response to Unsupported Transactions regardless of UEV.URE. When set to '0', the Unsupported Transactions detected on DMI will set the UES.URE bit.
29:3	0h RO	**Reserved**
2	0h RO	**Fatal Error Reporting Enable (FERE):** When set, the root port will generate an interrupt when a fatal error is reported by the attached device. Not implemented by PCH.
1	0h RO	**Non-fatal Error Reporting Enable (NERE):** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device. Not implemented in PCH.
0	0h RO	**Correctable Error Reporting Enable (CERE):** When set, the root port will generate an interrupt when a correctable error is reported by the attached device. Not implemented in PCH.

29.1.13 Root Error Status (RES) — Offset 20B0h

Root Error Status

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 20B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**Advanced Error Interrupt Message Number (AEMN):** There is only one error interrupt allocated.
26:4	0h RO	**Reserved**
3	0h RO	**Multiple ERR_FATAL/NONFATAL Recvieved (MENR):** Set when either a fatal or a non-fatal error is received and the ENR bit is already set. This is not supported in PCH.
2	0h RW/1C/V	**ERR_FATAL/NONFATAL Received (ENR):** Set when either a fatal or a non-fatal error message is received or an internal fatal error is detected (all internal uncorrectable errors are fatal).
1	0h RO	**Multiple ERR_COR Received (MCR):** Set when a correctable error message is received and the CR bit is already set. This is not supported in PCH
0	0h RW/1C/V	**ERR_COR Received (CR):** Set when a correctable error message is received or an internal correctable error is detected.

29.1.14 Error Source Identification (ESID) — Offset 20B4h

Error Source Identification

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 20B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO/V	**ERR_FATAL/NONFATAL Source Identification (ENSID):** Loaded with the requester ID indicated in the received ERR_FATAL or ERR_NONFATAL message when RES.ENR is first set, or the internal requestor ID if an internally detected error.
15:0	0000h RO/V	**ERR_COR Source Identification (CSID):** Loaded with the requester ID indicated in the received ERR_COR message when RES.CR is first set, or the internal requester ID if an internally detected error.

29.1.15 DMI Control Register (Common) (DMIC) — Offset 2234h

DMI Control Register (Common)

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 2234h	08000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Secured Register Lock (SRL):** When this bit is set, all the secured registers will be locked and will be Read-Only. The following fields are locked by DMIC.SRL: V0CTL.ETVM and V0CTL.TVM. V1CTL.ETVM and V1CTL.TVM. VMCTL.ETVM and VMCTL.TVM. REC.DPDP. LCTL.LD. DMIEIN.EPT. DMIC.TIOCTPD. DMIC.TXTPCE. DMIC.CPUSEL. DMIC.TXTPCRP. DMIHBP. DMI Source Decode Registers (except IO Trap). DMIDBG.ATE. DMIDBG.NEDLBE. DMIDBG.LBTE. DMICMMPC.START. PCE.SE. DMIEEPPES.PSSSGE. DMIEEPEG.PEG. DMPCHK. RXHALEP DMPCHK.MRSCDIS This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
30	0h RO	**Reserved**
29	0h RW/L	**Trusted I/O Context TLP Prefix Disable (TIOCTPD):** When set, disables the TIO Context TLP prefix support. On the transmit side, the TIO Context TLP prefix will not be forwarded to the other side of the link. On the receive side, the cycle with TIO Context TLP prefix will be handled as malformed. When clear, TIO Context TLP Prefix will be sent, subjected to DMIC.LTLPPDIS. This register is Read-Only if DMIC.SRL field is set. Register Attribute: Dynamic. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL

Bit Range	Default & Access	Field Name (ID): Description
28	0h RW/L	**Transmit TLP Prefix Caching Enable (TXTPCE):** When set, enables Transmit TLP Prefix Caching. This register is Read-Only if the DMIC.SRL field is set. Receive TLP Prefix Caching logic is not affected by this config bit. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
27	1h RW/L	**CPU Select (CPUSEL):** Indicates which CPU, DMI is paired with. '0': Compute Die '1': Reserved This register is expected to be programmed by PMC FW in between host_side_rst_b deassertion and host_prim_rst_b deassertion window. This register is Read-Only if DMIC.SRL field is set. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
26	0h RO/V	**Local TLP Prefix Disable (LTLPPDIS):** Disable Local TLP Prefix on transmit and receive path of the PCIe TLP formatter. '0': Enabled '1': Disabled The value of this field is defined by soft strap unless when DMIC.CPUSEL is '1'. When DMIC.CPUSEL is '1', this field will have a value of '1' also.
25:24	0h RW	**Offset Re-Calibration Enable (ORCE):** Enable offset re-calibration mechanism to cater for temperature variation during run-time. Offset re-calibration is triggered on entry to the following states: Polling.Active, Recovery.RcvrLock and Configuration.LinkwidthStart, qualified with the data rate configured in this field. '00b': Disable offset re-calibration. '01b': Enable offset re-calibration for Gen 2 and Gen 3 data rate only. '10b': Reserved. '11b': Enable offset re-calibration for all data rates. Note: This register is not applicable to OP-DMI. Register Attribute: Dynamic.
23	0h RW	**Offset Re-Calibration Request (ORCR):** When this bit is set followed by a link retrain, offset recalibration will be performed on entry to Recovery state. This bit cleared by hardware upon the completion of offset re-calibration in Recovery.RcvrLock state Note: When offset re-calibration request bit is set followed by a link retrain, hardware may truncate the received TLP/DLLP. Note: This register is not applicable to OP-DMI. Register Attribute: Static.
22:20	0h RW	**Flow Control Update Policy (FCP):** Indicates how long a flow control update should wait for transmit in the presence of TLPs to transmit. When the link is idle, a flow control update will occur immediately when it becomes available. Additionally, if a 2nd update becomes available, the flow control update will occur next, regardless of the clock count. Encodings are: Bits Encoding 101 Wait 128-160 link clocks before sending the update 100 Wait 96-128 link clocks before sending the update 011 Wait 64-96 link clocks before sending the update 010 Wait 32-64 link clocks before sending the update 000 Never wait, send flow control update immediately All values other than the ones specified will alias to '000'. Register Attribute: Static.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Downstream Non-Posted Request Limit (DNPRL):** When set, limits the number of downstream non-posted request towards PSF to just one outstanding. Register Attribute: Static.
18	0h RW	**IOSF Transaction Credit Update Mode (ITCUM):** When set, the credit update to the IOSF Fabric will occur on the clock the command is transferred to the retry buffer, ahead of the data transfer. When cleared, the credit update will not occur until the end of the data transfer. This register can only be set to '1' in OP-DMI x8 or DMI x4 GEN3 configuration.
17	0h RO/V	**Transaction Layer Packet Fast Transmit Mode (TLPF):** When set, the DMI transmit block will transmit the packet header in the upstream command queue without waiting for the corresponding data to be available. When cleared, the TLP transfer will not occur until the upstream data queue has the entire data phase available.
16	0h RO/V	**DMI Credit Allocated Update Mode (CAM):** When set, the credit update to the DMI transmit block will occur when the command is granted on the IOSF downstream backbone, ahead of the data transfer. When cleared, the credit update will not occur until the last data phase o the IOSF transaction.
15:8	0h RO	**Reserved**
7:5	0h RW/L	**Transmit TLP Prefix Cache Replacement Policy (TXTPCRP):** Indicates the number of times a unique set of TLP Prefix attributes are sampled before the cache is replaced. '000' - 1 time '001' - 2 times ... '110' - 7 times '111' - 8 times This register is Read-Only if the DMIC.SRL field is set. This register should be programmed to the desired value before enabling DMIC.TXTPCE Register Attribute: Static This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
4	0h RW	**Partition/Trunk Oscillator Clock Gate Enable (PTOCGE):** When set, this bit allows the oscillator clock to be gated at the partition/trunk level when the conditions are met. When cleared, the oscillator clock gating at the partition/trunk level is disabled. Note: If Core Dynamic Clock Gating Disable fuse is '1', hardware will always see 0 as an output from this register. BIOS reading this register should always return the correct value. Register Attribute: Static
3	0h RW	**DMI Link CLKREQ Enable (DMILCLKREQEN):** When set, this bit enables DMI to de-assert the DMI link CLKREQ. When cleared, DMI link CLKREQ is not allowed to de-assert. Note: If Link Trunk Clock Gating Disable fuse is '1', hardware will always see 0 as an output from this register. BIOS reading this register should always return the correct value.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**DMI Backbone CLKREQ Enable (DMIBBCLKREQEN):** When set, this bit enables DMI to de-assert the IOSF Primary backbone CLKREQ. When cleared, DMI IOSF Primary backbone CLKREQ is not allowed to de-assert.
1	0h RW	**DMI Link Dynamic Clock Gate Enable (DMILCGEN):** When set, this bit enables dynamic clock gating on the DMI Link clock domain logic. When cleared, dynamic clock gating on the DMI Link clock domain is disabled. Note: If Link Dynamic Clock Gating Disable fuse is '1', hardware will always see 0 as an output from this register. BIOS reading this register should always return the correct value.
0	0h RW	**DMI Backbone Dynamic Clock Gate Enable (DMIBCGEN):** When set, this bit enables dynamic clock gating on the DMI Backbone clock domain logic. When cleared, dynamic clock gating on the DMI backbone clock domain is disabled. Note: If Core Dynamic Clock Gating Disable fuse is '1', hardware will always see 0 as an output from this register. BIOS reading this register should always return the correct value.

29.1.16 IOSF Primary Control And Status (Common) (IPCS_IOSFSBCS) — Offset 223Ch

IOSF Primary Control And Status (Common)

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 223Ch	000C0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22	0h RW	**Side Clock Partition/Trunk Clock Gating Enable (SCPTCGE):** When set, the Side Clock will be clock gated at the partition/trunk level when the conditions to clock gate are met. When clear, the Side Clock will never be clock gated at the partition/trunk level. Note: If 'Core Dynamic Clock Gate Disable' fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. Register Attribute: Static.
21	0h RW	**Sideband Endpoint Oscillator/Side Dynamic Clock Gating Enable (SEOSCGE):** When set, the oscillator and Side clock used within the Sideband Endpoint will be dynamically gated when the condition permits. When cleared, the dynamic oscillator and Side clock gating mechanism is disabled. Note: If 'Core Dynamic Clock Gating Disable' fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. Register Attribute: Static.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**Reserved**
19:18	3h RW	**IOSF Sideband Interface Idle Counter (SIID):** This register provides configuration flexibility to govern when the trunk clock can be gated from the time the sideband interface is idle. 00: Wait for 32 idle clocks before allowing trunk clock gating. 01: Wait for 64 idle clocks before allowing trunk clock gating. 10: Wait for 128 idle clocks before allowing trunk clock gating. 11: Wait for 256 idle clocks before allowing trunk clock gating.
17:16	0h RW	**IOSF Sideband ISM Idle Counter (SBIC):** This register provides configuration flexibility to govern when the IOSF sideband ISM transitions to IDLE_REQ state with respect to sideband interface idle. 00: IOSF sideband ISM will transition to IDLE_REQ after 16 clocks of idle on sideband interface. 01: IOSF sideband ISM will transition to IDLE_REQ after 31 clocks of idle on sideband interface. 10: IOSF sideband ISM will transition to IDLE_REQ after 64 clocks of idle on sideband interface. 11: IOSF sideband ISM will never transition to IDLE_REQ on sideband interface. Note: Controller Power Gating will be blocked if this field is programmed to '11'
15	0h RO	**Reserved**
14:12	0h RW	**IOSF Primary ISM Idle Counter (PRIC):** This register provides configuration flexibility to govern when the IOSF primary ISM transitions to IDLE_REQ state with respect to primary interface idle. 000: IOSF primary ISM will transition to IDLE_REQ after 16 clocks of idle on primary interface. 001: IOSF primary ISM will transition to IDLE_REQ after 31 clocks of idle on primary interface. 010: IOSF primary ISM will transition to IDLE_REQ after 64 clocks of idle on primary interface. 011: IOSF primary ISM will transition to IDLE_REQ after 128 clocks of idle on primary interface. 100: IOSF primary ISM will transition to IDLE_REQ after 256 clocks of idle on primary interface. 101: IOSF primary ISM will transition to IDLE_REQ after 512 clocks of idle on primary interface. 110: IOSF primary ISM will transition to IDLE_REQ after 1024 clocks of idle on primary interface. 111: IOSF primary ISM will never transition to IDLE_REQ on primary interface. Note: Controller Power Gating will be blocked if this field is programmed to '111' Register Attribute: Dynamic.
11:0	0h RO	**Reserved**

29.1.17 Target Link Speed (TLS) — Offset 2608h

Target Link Speed

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 2608h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	2h RO/V	**Target Link Speed (TLS):** Specifies the Target link speed that should be used if speed change is supported. Bit | Description 0000 | SPEED0: 100 Mb/s per-lane 0001 | SPEED1: 1 Gb/s per-lane 0010 | SPEED2: 2 Gb/s per-lane 0011 | SPEED3: 4 GT/s per-lane 0100-1111 | Reserved Note: The default value of bit[1:0] is defined by soft strap. Bit[3:2] are hardwired to '00'. This field is Read-only (RO) in with TLS value defined by soft-strap. Only static speed configuration is supported.

29.1.18 Link Configuration (LCFG) — Offset 2618h

Link Configuration

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 2618h	00330031h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RO/V	**OPI PHY Low Voltage Operation Soft Strap (OPIPLVOSS):** This field reflects the status of the OPI PHY Low Voltage Operation soft-strap.
27	0h RW	**Aging Mitigation Enable (AME):** When set, Aging Mitigation logic will be enabled each time IDLE_L1 state is entered. Note: This bit is expected to be set before Hardware-Autonomous IDLE_L1 Enable (LCTL.HAIE) is set.

Bit Range	Default & Access	Field Name (ID): Description
26	0h RW	**Loopback Operational Mode (LOM):** 0': LOOPBACK operates as defined in the OPI spec rev 0.8. It is considered a Link Down condition with an extended sideband handshake exit to RESET. '1': LOOPBACK operates as defined in the OPI 'LOOPBACK to ACTIVE' ECN to the 0.8 spec. It is considered a Link Up condition if entered from ACTIVE, and will return to ACTIVE on an extended sideband handshake if entered from ACTIVE.
25	0h RW/L	**Secure Register Lock (SRL):** When set, locks the following registers: OPI Error Injection Control (EIC) register. LCTL.FLME. LCTL.LTE. LCTL.DNELBE. LCFG.DFELBE. LCFG.NESLE. OPIHBPC. Once this bit is written to '1', it cannot be changed until a PLTRST# occurs. This register is Read-Only if LCFG.SRL field is set **Locked by:** LCFG.SRL
24	0h RW/L	**Digital Far-End Loopback Enable (DFELBE):** When set, the Link Layer loops back the Receive data from the RXFIFO to the TXFIFO. This register is Read-Only if LCFG.SRL field is set. Note: This bit is expected to be set when the link is in ACTIVE state and the interface is in Transmit Idle/ Transmit Quiet state. This register is Read-Only if LCFG.SRL field is set **Locked by:** LCFG.SRL
23	0h RW/L	**Near-End Sideband Loopback Enable (NESLE):** When set, the TXSB will be loopback to RXSB in the Link Layer. None of the other OPI pins are impacted by this bit except for TXSB and RXSB. This bit is expected to be set when running in ANELB (master) and AFELB (master). The intention is to supplement the PHY loopback since TXSB and RXSB do not have abutment for loopback. This register is Read-Only if LCFG.SRL field is set. This register is Read-Only if LCFG.SRL field is set **Locked by:** LCFG.SRL
22:20	3h RO/V	**Transmit Link Width (TXLW):** This field specifies the number of transmit lanes. Bit | Description 000 | 1 lane 001 | 2 lanes 010 | 4 lanes 011 | 8 lanes 100 | 12 lanes (not supported) 101 | 16 lanes (not supported) 110 | 32 lanes (not supported) 111 | Reserved Note: Not all the link width is supported in PCH. The value of this field is defined by soft strap.
19	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18:16	3h RO/V	**Receive Link Width (RXLW):** This field specifies the number of receive lanes. Bit | Description 000 | 1 lane 001 | 2 lanes 010 | 4 lanes 011 | 8 lanes 100 | 12 lanes (not supported) 101 | 16 lanes (not supported) 110 | 32 lanes (not supported) 111 | Reserved Note: Not all the link width is supported in PCH. The value of this field is defined by soft strap.
15:12	0h RO	**Reserved**
11:10	0h RO	**ACTIVE State Link Reset Timer (ASLRT):** In any state other than SLEEP_L2.READY, LOOPBACK and DISABLED state, once the Secondary Bus Reset or Link Reset register is set, a timer will be kicked off. If the timer expires prior to the Sideband signal assertion on both sides of the link, acknowledging LINKRESET entry, the extended Sideband handshake is performed. Bit | Description 00 | 5 ms 01 | 10 ms 10 | 20 ms 11 | 30 ms This field is only used by the upstream component. The field is Read-only (RO) '0' in PCH. It is not applicable for PCH as the OPI downstream device.
9:8	0h RO	**Unsuccessful Speed Change Timer (USCT):** This is the timer value for the component to wait for the Ping LLP after a speed change. The timer starts from the time the LSM enters ACTIVE_L0 state with the Speed Change Flag set from SPEED state. Bit | Description 00 | Disabled 01 | 50 us 10 | 100 us 11 | 1 ms The field is Read-only (RO) '0' in PCH. It is not applicable for PCH as only static speed configuration is supported.
7	0h RO	**Reserved**
6:4	3h RW	**TLCP Grant Count (TLCPGC):** Sets the grant count for FCPs in the link arbiter. The counter is decremented each time a TLCP request is granted. In the absence of higher priority requests, the FCP requests will continue to be granted until the counter reaches 0. The counter is reset when all grant counters are 0 or, no requests are asserted.
3	0h RO	**Reserved**
2:0	1h RW	**TLP Grant Count (TLPGC):** Sets the grant count for TLP in the link arbiter. The counter is decremented each time a TLP request is granted. In the absence of higher priority requests, the TLP requests will continue to be granted until the counter reaches 0. The counter is reset when all grant counters are 0 or, no requests are asserted.

29.1.19 LPC Generic I/O Range 1 (LPCLGIR1) — Offset 2730h

LPC Generic I/O Range 1

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 2730h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:18	00h RW/L	**Address[7:2] Mask (ADDRMASK):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
17:16	0h RO	**Reserved**
15:2	0000h RW/L	**Address[15:2] DWord-aligned address (ADDR):** Address[15:2]: DWord-aligned address. PCH does not provide decode down to the word or byte level. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
1	0h RW/L	**ISH Decode Enable (ISHDE):** When this bit is set to '1', then the range specified in this register is enabled for decoding to ISH. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
0	0h RW/L	**LPC Decode Enable (LPCDEN):** When this bit is set to '1' and ISHDE==0, then the range specified in this register is enabled for decoding to LPC. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL

29.1.20 LPC Generic I/O Range 2 (LPCLGIR2) — Offset 2734h

LPC Generic I/O Range 2

Note: Bit definitions are the same as LPCLGIR1, offset 2730h.

29.1.21 LPC Generic I/O Range 3 (LPCLGIR3) — Offset 2738h

LPC Generic I/O Range 3

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 2738h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:18	00h RW/L	**Address[7:2] Mask (ADDRMASK):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
17:16	0h RO	**Reserved**
15:2	0000h RW/L	**Address[15:2] DWord-aligned address (ADDR):** Address[15:2]: DWord-aligned address. Note that PCH does not provide decode down to the word or byte level. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
1	0h RW/L	**ISH Decode Enable (ISHDE):** When this bit is set to '1', then the range specified in this register is enabled for decoding to ISH. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
0	0h RW/L	**LPC Decode Enable (LPCDEN):** When this bit is set to '1' and ISHDE==0, then the range specified in this register is enabled for decoding to LPC. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL

29.1.22 LPC Generic I/O Range 4 (LPCLGIR4) — Offset 273Ch

LPC Generic I/O Range 4

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 273Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:18	00h RW/L	**Address[7:2] Mask (ADDRMASK):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
17:16	0h RO	**Reserved**
15:2	0000h RW/L	**Address[15:2] DWord-aligned address (ADDR):** Address[15:2]: DWord-aligned address. CH does not provide decode down to the word or byte level. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
1	0h RW/L	**ISH Decode Enable (ISHDE):** When this bit is set to '1', then the range specified in this register is enabled for decoding to ISH. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
0	0h RW/L	**LPC Decode Enable (LPCDEN):** When this bit is set to '1' and ISHDE==0, then the range specified in this register is enabled for decoding to LPC. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL

29.1.23 LPC Generic Memory Range (LPCGMR) — Offset 2740h

LPC Generic Memory Range

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 2740h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/L	**Memory Address[31:16] (MEMADDR):** Memory Address[31:16]: This field specifies a 64KB memory block anywhere in the 4GB memory space that will be decoded to LPC as standard LPC Memory Cycle if enabled. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
15:1	0h RO	**Reserved**
0	0h RW/L	**LPC Memory Range Decode Enable (LPCMRDEN):** When this bit is set to '1', then the range specified in this register is enabled for decoding to LPC. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL

29.1.24 LPC BIOS Decode Enable (LPCBDE) — Offset 2744h

LPC BIOS Decode Enable

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 2744h	0000FFCFh

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	1h RO	**F8-FF Enable (EF8):** Enables decoding of 512K of the following BIOS range: Data space: FFF80000h FFFFFFFFh Feature space: FFB80000h FFBFFFFFh Register Attribute: Static.
14	1h RW/L	**F0-F8 Enable (EF0):** Enables decoding of 512K of the following BIOS range: Data space: FFF00000h FFF7FFFFh Feature space: FFB00000h FFB7FFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
13	1h RW/L	**E8-EF Enable (EE8):** Enables decoding of 512K of the following BIOS range: Data space: FFE80000h FFEFFFFFh Feature space: FFA80000h FFAFFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
12	1h RW/L	**E0-E8 Enable (EE0):** Enables decoding of 512K of the following BIOS range: Data space: FFE00000h FFE7FFFFh Feature Space: FFA00000h FFA7FFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
11	1h RW/L	**D8-DF Enable (ED8):** Enables decoding of 512K of the following BIOS range: Data space: FFD80000h FFDFFFFFh Feature space: FF980000h FF9FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL

Bit Range	Default & Access	Field Name (ID): Description
10	1h RW/L	**D0-D7 Enable (ED0):** Enables decoding of 512K of the following BIOS range: Data space: FFD00000h FFD7FFFFh Feature space: FF900000h FF97FFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
9	1h RW/L	**C8-CF Enable (EC8):** Enables decoding of 512K of the following BIOS range: Data space: FFC80000h FFCFFFFFh Feature space: FF880000h FF8FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
8	1h RW/L	**C0-C7 Enable (EC0):** Enables decoding of 512K of the following BIOS range: Data space: FFC00000h FFC7FFFFh Feature space: FF800000h FF87FFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
7	1h RW/L	**Legacy F Segment Enable (LFE):** This enables the decoding of the legacy 64KB range at F0000h FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
6	1h RW/L	**Legacy E Segment Enable (LEE):** This enables the decoding of the legacy 64KB range at E0000h EFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
5:4	0h RO	**Reserved**
3	1h RW/L	**70-7F Enable (E70):** Enables decoding of 1MB of the following BIOS range: Data space: FF700000h FF7FFFFFh Feature space: FF300000h FF3FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL

Bit Range	Default & Access	Field Name (ID): Description
2	1h RW/L	**60-6F Enable (E60):** Enables decoding of 1MB of the following BIOS range: Data space: FF600000h FF6FFFFFh Feature Space: FF200000h FF2FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
1	1h RW/L	**50-5F Enable (E50):** Enables decoding of 1MB of the following BIOS range: Data space: FF500000h FF5FFFFFh Feature Space: FF100000h FF1FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
0	1h RW/L	**40-4F Enable (E40):** Enables decoding of 1MB of the following BIOS range: Data space: FF400000h FF4FFFFFh Feature space: FF000000h FF0FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL

29.1.25 uCode Patch Region (UCPR) — Offset 2748h

uCode Patch Region

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 2748h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	1h RW/L	**uCode Patch Region Enable (UPRE):** When set, enables memory access targeting the uCode patch region (0xFEF00000 to 0xFEFFFFFF) to be forwarded to SPI Flash. This register is Read-Only if the DMIC.SRL field is set. Note: This bit should never be set if the boot flash is on LPC. This bit can only be set if the boot flash is on SPI. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL

29.1.26 General Control and Status (GCS) — Offset 274Ch

General Control and Status

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 274Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/L	**RPR Destination ID (RPRDID):** This field specifies the PCIe port Destination ID that is the target of the I/O ranges specified in the RPR field. Only one PCIe root port at a time can be enabled for Port 8xh support. This field is only valid when GCS.RPR field is set. BIOS must program the bits which are not used to zeros. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
15:11	0h RO	**Reserved**
10	0h RW/V/L	**Boot BIOS Strap (BBS):** This field determines the destination of accesses to the BIOS memory range. Bits Description 0b: SPI 1b: LPC/eSPI When SPI or LPC/eSPI is selected, the range that is decoded is further qualified by other configuration bits described in the respective sections. The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down (bit 0) and DMIC.SRL are not set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
9:1	0h RO	**Reserved**
0	0h RW/O	**BIOS Interface Lock-Down (BILD):** When set, prevents GCS.BBS from being changed. This bit can only be written from 0 to 1 once. Register Attribute: Static.

29.1.27 I/O Trap Register 1 - Lower DW (IOT1_LOW) — Offset 2750h

I/O Trap Register 1 - Lower DW

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 2750h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:18	00h RW	**Address[7:2] Mask (ADDRMASK):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size. Register Attribute: Static.
17:16	0h RO	**Reserved**
15:2	0000h RW	**Address[15:2] DWord-aligned address (ADDR):** Address[15:2]: DWord-aligned address. Register Attribute: Static.
1	0h RO	**Reserved**
0	0h RW	**Trap Enable (TNSMIEN):** When this bit is set to '1', then the trapping logic specified in this register is enabled. Register Attribute: Static.

29.1.28 I/O Trap Register 1 - Upper DW (IOT1_HIGH) — Offset 2754h

I/O Trap Register 1 - Upper DW

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 2754h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RW	**Read/Write Mask (RWMASK):** When this bit is '1', the trapping logic will operate on both read and write cycles. When this bit is '0', the cycle must match the type specified in bit IOT1.RWB. Register Attribute: Static.
16	0h RW	**RW:** 1 = Read, 0 = Write - the value in this field does not matter if bit IOT1.RWM is set. Register Attribute: Static.
15:8	0h RO	**Reserved**
7:4	0h RW	**Byte Enable Mask (BEMASK):** A '1' in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored. Register Attribute: Static.
3:0	0h RW	**Byte Enable (BE):** Active-high, DWord-aligned byte enables. Register Attribute: Static.

29.1.29 LPC I/O Decode Ranges (LPCIOD) — Offset 2770h

LPC I/O Decode Ranges

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 2770h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RW/L	**FDD Range (FDD):** The following table describes which range to decode for the FDD Port. Bits | Decode Range 0 | 3F0h 3F5h, 3F7h | (Primary) 1 | 370h 375h, 377h (Secondary) This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
11:10	0h RO	**Reserved**
9:8	0h RW/L	**LPT Range (LPT):** The following table describes which range to decode for the LPT Port. Bits | Decode Range 00 | 378h 37Fh and 778h 77Fh 01 | 278h 27Fh (port 279h is read only) and 678h 67Fh 10 | 3BCh 3BEh and 7BCh 7BEh 11 | Reserved. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6:4	0h RW/L	**ComB Range (CB):** The following table describes which range to decode for the COMB Port. Bits | Decode Range 000 | 3F8h 3FFh (COM1) 001 | 2F8h 2FFh (COM2) 010 | 220h 227h 011 | 228h 22Fh 100 | 238h 23Fh 101 | 2E8h 2EFh | (COM 4) 110 | 338h 33Fh 111 | 3E8h 3EFh (COM 3) This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
3	0h RO	**Reserved**
2:0	0h RW/L	**ComA Range (CA):** The following table describes which range to decode for the COMA Port. Bits | Decode Range 000 | 3F8h 3FFh (COM1) 001 | 2F8h 2FFh (COM2) 010 | 220h 227h 011 | 228h 22Fh 100 | 238h 23Fh 101 | 2E8h 2EFh (COM 4) 110 | 338h 33Fh 111 | 3E8h 3EFh (COM 3) This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL

29.1.30 LPC I/O Enables (LPCIOE) — Offset 2774h

LPC I/O Enables

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 2774h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9	0h RW/L	**High Gameport Enable (HGE):** Enables decoding of the I/O locations 208h to 20Fh to LPC. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
8	0h RW/L	**Low Gameport Enable (LGE):** Enables decoding of the I/O locations 200h to 207h to LPC. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
7:4	0h RO	**Reserved**
3	0h RW/L	**Floppy Drive Enable (FDE):** Enables decoding of the FDD range to LPC. Range is selected by LIOD.FDE. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
2	0h RW/L	**Parallel Port Enable (PPE):** Enables decoding of the LPT range to LPC. Range is selected by LIOD.LPT. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
1	0h RW/L	**Com Port B Enable (CBE):** Enables decoding of the COMB range to LPC. Range is selected LIOD.CB. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
0	0h RW/L	**Com Port A Enable (CAE):** Enables decoding of the COMA range to LPC. Range is selected LIOD.CA. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL

29.1.31 TCO Base Address (TCOBASE) — Offset 2778h

TCO Base Address

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 2778h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:5	000h RW/L	**TCO Base Address (TCOBA):** Provides the 32 bytes of I/O space for TCO logic, that can be map anywhere in the 64k I/O space on 32-byte boundaries. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
4:2	0h RO	**Reserved**
1	0h RW/L	**TCO Enable (TCOEN):** When set, decode of the I/O range specified by the TCO base address. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
0	1h RO	**Always 1 (A1IOS):** Always 1 to indicate I/O space.

29.1.32 General Purpose Memory Range 1 (GPMR1) — Offset 277Ch

General Purpose Memory Range 1

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 277Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/L	**General Purpose Memory Range Limit 1 (GPMRL1):** This field specifies limit address bits[31:16] for the General Purpose Memory Range 1. Bits [15:0] are assumed to be 'FFFFh'. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
15:0	0000h RW/L	**General Purpose Memory Range Base 1 (GPMRB1):** This field specifies base address bits[31:16] for the General Purpose Memory Range 1. Bits [15:0] are assumed to be '0000h'. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL

29.1.33 General Purpose Memory Range 1 Destination ID (GPMR1DID) — Offset 2780h

General Purpose Memory Range 1 Destination ID

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 2780h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**General Purpose Memory Range 1 Decode Enable (GPMR1DE):** When enabled, memory cycles that falls within the GPMR1.GPMRL1 and GPMR1.GPMRB1 range inclusive will be forwarded using source decode to the destination ID specified in GPMR1DID.GPMR1DID field. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
30:0	00000000h RW/L	**General Purpose Memory Range 1 Destination ID (GPMR1DID):** The destination ID to be used to forward the cycle decoded to hit the General Purpose Memory Range 1. BIOS must program the bits which are not used to zeros. Hardware will ignore the unused bits. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL

29.1.34 PM Base Address (PMBASEA) — Offset 27ACh

PM Base Address

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 27ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/L	**PM Base Address Memory Range Limit (PMBAMRL):** This field specifies limit address bits[31:16] for the PM Base Address memory range. Bits [15:0] are assumed to be 'FFFFh'. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
15:0	0000h RW/L	**PM Base Address Memory Range Base (PMBAMRB):** This field specifies base address bits[31:16] for the PM Base Address memory range. Bits [15:0] are assumed to be '0000h'. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL

29.1.35 PM Base Control (PMBASEC) — Offset 27B0h

PM Base Control

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 27B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**PM Base Address Memory Range Decode Enable (PMBAMRDE):** When enabled, memory cycles that falls within the PMBASEADDR.PMBAMRB and PMBASEADDR.PMBAMRL range inclusive will be forwarded using source decode to the destination ID specified in PMBASEC.PMBDID field. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
30:0	00000000h RW/L	**PM Base Destination ID (PMBDID):** The destination ID to be used to forward the cycle decoded to hit the PM Base Address range. BIOS must program the bits which are not used to zeros. Hardware will ignore the unused bits. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL

29.1.36 ACPI Base Address (ACPIBA) — Offset 27B4h

ACPI Base Address

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 27B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:18	00h RW/L	**Address[7:2] Mask (ADDR72MASK):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
17:16	0h RO	**Reserved**
15:2	0000h RW/L	**Address[15:2] DWord-aligned address (ADDR):** Address[15:2]: DWord-aligned address. PCH does not provide decode down to the word or byte level. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL
1	0h RO	**Reserved**
0	0h RW/L	**ACPI I/O Base Address Decode Enable (ACPIBADE):** When this bit is set to '1', then the range specified in this register is enabled for decoding to the destination ID specified in ACPIBDID register. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL

29.1.37 ACPI Base Destination ID (ACPIBDID) — Offset 27B8h

ACPI Base Destination ID

Type	Size	Offset	Default
MMIO	32 bit	FD880000h + 27B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**ACPI Base Destination ID (ACPIBDID):** The destination ID to be used to forward the cycle decoded to hit the ACPI Base Address range. BIOS must program the bits which are not used to zeros. Hardware will ignore the unused bits. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set **Locked by:** DMIC.SRL

30 I/O Trap

30.1 I/O Trap Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 30-1. Summary of I/O Trap Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1D00h	4	PSTH Control Register (PSTHCTL)	00000000h
1E00h	4	Trap Status Register (TRPSTS)	00000000h
1E10h	4	Trapped Cycle Register (TRPCYC1)	00000000h
1E18h	4	Trapped Write Data Register (TRPWRDATA1)	00000000h
1E80h	4	I/O Trap Registers 1 (IOTRP1_1)	00000000h
1E84h	4	I/O Trap Registers 1 (IOTRP1_2)	00000000h
1E88h	4	I/O Trap Registers 2 (IOTRP2_1)	00000000h
1E8Ch	4	I/O Trap Registers 2 (IOTRP2_2)	00000000h
1E90h	4	I/O Trap Registers 3 (IOTRP3_1)	00000000h
1E94h	4	I/O Trap Registers 3 (IOTRP3_2)	00000000h
1E98h	4	I/O Trap Registers 4 (IOTRP4_1)	00000000h
1E9Ch	4	I/O Trap Registers 4 (IOTRP4_2)	00000000h

30.1.1 PSTH Control Register (PSTHCTL) - Offset 1D00h

PSTH Control Register

Type	Size	Offset	Default
MMIO	32 bit	FD890000h + 1D00h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**PSTH IOSF Primary Trunk Clock Gating Enable (PSTHIOSFPTCGE):** When set, the IOSF Primary CLKREQ for PSTH will de-assert when the conditions to clock gate are met. When clear, the IOSF Primary CLKREQ for PSTH will never de-assert, preventing IOSF Primary trunk clock gating.
1	0h RW	**PSTH IOSF Sideband Trunk Clock Gating Enable (PSTHIOSFSTCGE):** When set, the IOSF Sideband CLKREQ for PSTH will de-assert when the conditions to clock gate are met. When clear, the IOSF Sideband CLKREQ for PSTH will never de-assert, preventing IOSF Sideband trunk clock gating.
0	0h RW	**PSTH Dynamic Clock Gating Enable (PSTHDCGE):** When set, the clocks used within the PSTH block will be dynamically gated when the condition permits. When cleared, the dynamic clock gating mechanism is disabled.

30.1.2 Trap Status Register (TRPSTS) - Offset 1E00h

Trap Status Register

Type	Size	Offset	Default
MMIO	32 bit	FD890000h + 1E00h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW/1C/V	**Cycle Trap SMI# Status (SMISTAT):** These bits are set by hardware when the corresponding Cycle Trap register is enabled and a matching cycle is received (and trapped). These bits are OR'ed together to create a single status bit in the Power Management register space. Note that the SMI# and trapping must be enabled in order to set these bits. This is because, in order to do the cycle comparison, packets must be delayed by several clocks from the DMI pins to the internal receiver. This delay is only enabled when at least one of the trap ranges is enabled. These bits are set before the completion is generated for the trapped cycle, thereby guaranteeing that the processor can enter the SMI# handler when the instruction completes. Each status bit is cleared by writing a '1' to the corresponding bit location in this register.

30.1.3 Trapped Cycle Register (TRPCYC1) - Offset 1E10h

This register saves information about the I/O Cycle that was trapped and generated the SMI# for software to read.

Type	Size	Offset	Default
MMIO	32 bit	FD890000h + 1E10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO/V	**TRPRWR:** 1 = Read, 0 = Write
23:20	0h RO	**Reserved**
19:16	0h RO/V	**Active-High Byte Enables (TRPBE):** This is the DWord-aligned byte enables associated with the trapped cycle. A 1 in any bit location indicates that the corresponding byte is enabled in the cycle.
15:2	0000h RO/V	**IO Address (TRPADDR):** This is the DWord-aligned address of the trapped cycle.
1:0	0h RO	**Reserved**

30.1.4 Trapped Write Data Register (TRPWRDATA1) - Offset 1E18h

This register saves the data from I/O write cycles that are trapped for software to read

Type	Size	Offset	Default
MMIO	32 bit	FD890000h + 1E18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TRPDATA:** DWord of I/O write data. This field is undefined after trapping a read cycle.

30.1.5 I/O Trap Registers 1 (IOTRP1_1) - Offset 1E80h

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Type	Size	Offset	Default
MMIO	32 bit	FD890000h + 1E80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:18	00h RW	**Address Mask (TRP1ADDRM):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	0h RO	**Reserved**
15:2	0000h RW	**TRP1ADDR:** DWord-aligned address.
1	0h RO	**Reserved**
0	0h RW	**Trap and SMI Enable (TRP1EN):** When this bit is set to '1', then the trapping logic specified in this register is enabled.

30.1.6 I/O Trap Registers 1 (IOTRP1_2) - Offset 1E84h

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Type	Size	Offset	Default
MMIO	32 bit	FD890000h + 1E84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RW	**Read-Write Mask (TRP1RWM):** When this bit is '1', the trapping logic will operate on both read and write cycles. When this bit is '0', the cycle must match the type specified in bit 48.
16	0h RW	**TRP1RW:** 1 = Read, 0 = Write, the value in this field does not matter if bit 49 is set.
15:8	0h RO	**Reserved**
7:4	0h RW	**Byte Enable Mask (TRP1BEM):** A '1' in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h RW	**Byte Enables (TRP1BE):** Active-high, DWord-aligned byte enables.

30.1.7 I/O Trap Registers 2 (IOTRP2_1) - Offset 1E88h

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Type	Size	Offset	Default
MMIO	32 bit	FD890000h + 1E88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:18	00h RW	**Address Mask (TRP2ADDRM):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	0h RO	**Reserved**
15:2	0000h RW	**TRP2ADDR:** DWord-aligned address.
1	0h RO	**Reserved**
0	0h RW	**Trap and SMI Enable (TRP2EN):** When this bit is set to '1', then the trapping logic specified in this register is enabled.

30.1.8 I/O Trap Registers 2 (IOTRP2_2) - Offset 1E8Ch

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Type	Size	Offset	Default
MMIO	32 bit	FD890000h + 1E8Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RW	**Read-Write Mask (TRP2RWM):** When this bit is '1', the trapping logic will operate on both read and write cycles. When this bit is '0', the cycle must match the type specified in bit 48.
16	0h RW	**TRP2RW:** 1 = Read, 0 = Write, the value in this field does not matter if bit 49 is set.
15:8	0h RO	**Reserved**
7:4	0h RW	**Byte Enable Mask (TRP2BEM):** A '1' in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h RW	**Byte Enables (TRP2BE):** Active-high, DWord-aligned byte enables.

30.1.9 I/O Trap Registers 3 (IOTRP3_1) - Offset 1E90h

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Type	Size	Offset	Default
MMIO	32 bit	FD890000h + 1E90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:18	00h RW	**Address Mask (TRP3ADDRM):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	0h RO	**Reserved**
15:2	0000h RW	**TRP3ADDR:** DWord-aligned address.
1	0h RO	**Reserved**
0	0h RW	**Trap and SMI Enable (TRP3EN):** When this bit is set to '1', then the trapping logic specified in this register is enabled.

30.1.10 I/O Trap Registers 3 (IOTRP3_2) - Offset 1E94h

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Type	Size	Offset	Default
MMIO	32 bit	FD890000h + 1E94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RW	**Read-Write Mask (TRP3RWM):** When this bit is '1', the trapping logic will operate on both read and write cycles. When this bit is '0', the cycle must match the type specified in bit 48.
16	0h RW	**TRP3RW:** 1 = Read, 0 = Write, the value in this field does not matter if bit 49 is set.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:4	0h RW	**Byte Enable Mask (TRP3BEM):** A '1' in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h RW	**Byte Enables (TRP3BE):** Active-high, DWord-aligned byte enables.

30.1.11 I/O Trap Registers 4 (IOTRP4_1) - Offset 1E98h

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Type	Size	Offset	Default
MMIO	32 bit	FD890000h + 1E98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:18	00h RW	**Address Mask (TRP4ADDRM):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:1	0h RO	**Reserved**
0	0h RW	**Trap and SMI Enable (TRP4EN):** When this bit is set to '1', then the trapping logic specified in this register is enabled.

30.1.12 I/O Trap Registers 4 (IOTRP4_2) - Offset 1E9Ch

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Type	Size	Offset	Default
MMIO	32 bit	FD890000h + 1E9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RW	**Read-Write Mask (TRP4RWM):** When this bit is '1', the trapping logic will operate on both read and write cycles. When this bit is '0', the cycle must match the type specified in bit 48.
16	0h RW	**TRP4RW:** 1 = Read, 0 = Write, the value in this field does not matter if bit 49 is set.
15:8	0h RO	**Reserved**
7:4	0h RW	**Byte Enable Mask (TRP4BEM):** A '1' in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h RW	**Byte Enables (TRP4BE):** Active-high, DWord-aligned byte enables.

31 ModPHY Configuration

31.1 ModPHY Configuration Registers Summary

Table 31-1. Summary of ModPHY Configuration Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8188h	4	PLL_DWORD2 (PLL_DWORD2)	00000125h
818Ch	4	PLL_DWORD3 (PLL_DWORD3)	00000000h

31.1.1 PLL_DWORD2 (PLL_DWORD2) - Offset 8188h

This register configures the ModPHY PLL used for USB 3.1 and PCIe Gen 1 & 2.

Type	Size	Offset	Default
MMIO	32 bit	FDAB0000h + 8188h	00000125h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:24	0h RW	**i_sscstepsize_9_8:** RET Fractional value for one SSC frequency step. Effected by i_ssc_propagate_h
23:16	0h RW	**i_sscstepsize_7_0:** RET Fractional value for one SSC frequency step. Effected by i_ssc_propagate_h
15:11	0h RO	**Reserved**
10	0h RW	**i_sscen_h:** RET Enables SSC modulator. Used for dynamically controlling SSC modulator. SSC profile shuts off after reaching neutral point.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**i_feedfwrdcal_pause_h:** RET This bit is for dynamically turning on and off feed forward gain calibration, when i_feedfwrdcal_en_h is enabled to take care of dynamic feedfwrdgain calculation during SSC mode
8	1h RW	**i_feedfwrdcal_en_h:** RET Background feedfward gain calibration enable signal This is meant for PVT coverage. During PLL ramping this need to be disabled. It is taken care by dynamically changing i_feedfwrdcal_pause_h
7:0	25h RW	**i_feedfwrdgain_7_0:** RET Feedforwad gain for fractional mode/SSC mode PLL This setting is needed whenever PLL is configured in fractional mode or configured for SSC clock generation. use 34 as default @ 5.4GHz Effected by i_fbdiv_propagate_h

31.1.2 PLL_DWORD3 (PLL_DWORD3) - Offset 818Ch

This register configures the ModPHY PLL used for USB 3.1 and PCIe Gen 1 & 2.

Type	Size	Offset	Default
MMIO	32 bit	FDAB0000h + 818Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved**
23:17	0h RO	**Reserved**
16	00h RO	**Reserved**
15:9	00h RO	**Reserved**
8	0h RW	**i_rampafc_sscen_h:** RET 0: Disables changing of AFC during SSC 1: Enables AFC changes during SSC to take care PLL ramping and SSC simultaneously This need to be high only for 2-3% SSC spread cases.
7:1	0h RO	**Reserved**
0	0h WO	**i_ssc_propagate_h:** RETCLR Propagate bit for LCPLL to capture SSC stepsize This bit is automatically cleared after sscstepsize settings captured. (HW Clear)

31.2 ModPHY Configuration Registers

Table 33: ModPHY Register Address Details

Flex Lane #	Interface Lane #			HSIO RX/TX ModPHY Registers Address Detail							
	USB	PCIe	SATA	RX_ DWORD21	RX_ DWORD25	RX_ DWORD51	RX_ DWORD5	RX_ DWORD6	RX_ DWORD8	RX_ DWORD9	RX_ DWORD19
0	0	0	0		0xFDAB0264	0xFDAB02CC	0xFDAB0154		0xFDAB0160	0xFDAB0164	0xFDAB018C
1	1				0xFDAB0664	0xFDAB06CC	0xFDAB0554		0xFDAB0560	0xFDAB0564	0xFDAB058C
2	2	0			0xFDAB0A64	0xFDAB0ACC	0xFDAB0954	0xFDAB0958	0xFDAB0960	0xFDAB0964	0xFDAB098C
3	3	1			0xFDAB0E64	0xFDAB0ECC	0xFDAB0D54	0xFDAB0D58	0xFDAB0D60	0xFDAB0D64	0xFDAB0D8C
4		2					0xFDAA0154	0xFDAA0158	0xFDAA0160		0xFDAA018C
5		3					0xFDAA0554	0xFDAA0558	0xFDAA0560		0xFDAA058C
6		4					0xFDAA0954	0xFDAA0958	0xFDAA0960		0xFDAA098C
7		5					0xFDAA0D54	0xFDAA0D58	0xFDAA0D60		0xFDAA0D8C
8		6					0xFDA90154	0xFDA90158	0xFDA90160		0xFDA9018C
9		7					0xFDA90554	0xFDA90558	0xFDA90560		0xFDA9058C
10		8	0	0xFDA90A54			0xFDA90954	0xFDA90958	0xFDA90960		0xFDA9098C
11		9	1	0xFDA90E54			0xFDA90D54	0xFDA90D58	0xFDA90D60		0xFDA90D8C

31.2.1 HSIO_RX_SATA_DWORD21 – High Speed I/O Receive SATA Control Register 21

Address: Refer to Table 33

BIOS Reference Code Platform Configuration PCH Policy Details:

SATA 1.5 GT/s Parameters

PchSataHsioRxGen1EqBoostMagEnable = 1 (Enable)

PchSataHsioRxGen1EqBoostMag = Bits[13:8]

SATA 3.0 GT/s Parameters

PchSataHsioRxGen2EqBoostMagEnable = 1 (Enable)

PchSataHsioRxGen2EqBoostMag = Bits[5:0]

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>31:14</td><td>Reserved</td></tr>
<tr><td rowspan="6">13:8</td><td>SATA 1.5 GT/s
Receiver Equalization Boost Magnitude Adjustment (icfgctledatatap_quatrate) - R/W
These bits can be used to set the Receiver Equalization Boost Magnitude (ratio of low frequency to high frequency gain) applied to input signals to compensate for channel losses and open the input receive signal eye. The recommended topology-based values for this bit field are detailed in the table below.
• Value = ~ (Bit Decimal Value * 0.8) dB
<table>
<tr><td rowspan="2">Trace Length (mm)</td><td colspan="2">Recommended Cable Topology Based Values</td><td colspan="3">Recommended Non- Cable Topology Based Values</td></tr>
<tr><td>Internal SATA (Cable Connector)</td><td>Flex Connector</td><td>mSATA</td><td>Direct SATA</td><td>M.2 (NGFF)</td></tr>
<tr><td>50.8 – 101.6</td><td>000001b</td><td>000001b</td><td>000001b</td><td>000001b</td><td>000001b</td></tr>
<tr><td>101.6 – 152.4</td><td>000001b</td><td>000001b</td><td>000001b</td><td>000001b</td><td>000001b</td></tr>
<tr><td>152.4 – 177.8</td><td>NA</td><td>NA</td><td>000001b</td><td>000001b</td><td>000001b</td></tr>
<tr><td>177.8 – 203.2</td><td>NA</td><td>NA</td><td>000001b</td><td>000001b</td><td>000001b</td></tr>
</table></td></tr>
<tr><td>7:6</td><td>Reserved</td></tr>
<tr><td rowspan="6">5:0</td><td>SATA 1.5 GT/s
Receiver Equalization Boost Magnitude Adjustment (icfgctledatatap_halfrate) - R/W
These bits can be used to set the Receiver Equalization Boost Magnitude (ratio of low frequency to high frequency gain) applied to input signals to compensate for channel losses and open the input receive signal eye. The recommended topology-based values for this bit field are detailed in the table below.
• Value = ~ (Bit Decimal Value * 0.8) dB
<table>
<tr><td rowspan="2">Trace Length (mm)</td><td colspan="2">Recommended Cable Topology Based Values</td><td colspan="3">Recommended Non- Cable Topology Based Values</td></tr>
<tr><td>Internal SATA (Cable Connector)</td><td>Flex Connector</td><td>mSATA</td><td>Direct SATA</td><td>M.2 (NGFF)</td></tr>
<tr><td>50.8 – 101.6</td><td>000010b</td><td>000010b</td><td>000010b</td><td>000010b</td><td>000010b</td></tr>
<tr><td>101.6 – 152.4</td><td>000010b</td><td>000010b</td><td>000010b</td><td>000010b</td><td>000010b</td></tr>
<tr><td>152.4 – 177.8</td><td>NA</td><td>NA</td><td>000010b</td><td>000010b</td><td>000010b</td></tr>
<tr><td>177.8 – 203.2</td><td>NA</td><td>NA</td><td>000010b</td><td>000010b</td><td>NA</td></tr>
</table></td></tr>
</table>

31.2.2 HSIO_RX_USB3p1_DWORD25 - High Speed I/O Receive USB 3.1 Control Register 25

Address: Refer to Table 33

BIOS Reference Code Platform Configuration PCH Policy Details:

USB 3.1 Gen2 Parameters

PchUsb3HsioCtrlAdaptOffsetCfgEnable = 1 (Enable)

PchUsb3HsioCtrlAdaptOffsetCfg = Bits[20:16]

Bit	Description
31:21	**Reserved**
20:16	**USB 3.1 Gen2** **Receiver Continuous Time Linear Equalization (CTLE) Adaptation Offset Value (ctle_adapt_offset_cfg_4_0) - R/W** These bits can be adjusted, if needed to improve Receiver Jitter Tolerance (JTOL). 00000b = Minimum Level 00001b 00010b = PCH Default 00011b 01000b = Maximum Level 01001b to 11111b = Reserved **Note**: If manually changed the USB 3.1 Gen2 Link must be retrained for it to take effect. This can be done by unplugging the USB 3.1 Gen2 device and then plugging it back in.
15:0	**Reserved**

31.2.3 HSIO_RX_USB3p1_DWORD51 - High Speed I/O Receive USB 3.1 Control Register 51

Address: Refer to Table 33

BIOS Reference Code Platform Configuration PCH Policy Details:

- USB 3.1 Gen2 Parameters
  - PchUsb3HsioFilterSelNEnable = 1 (Enable)
  - PchUsb3HsioFilterSelN = Bits[29:27]
  - PchUsb3HsioFilterSelPEnable = 1 (Enable)
  - PchUsb3HsioFilterSelP = Bits[26:24]
  - PchUsb3HsioOlfpsCfgPullUpDwnResEnable = 1 (Enable)

— PchUsb3HsioOlfpsCfgPullUpDwnRes = Bits[2:0]

Bit	Description
31:30	**Reserved**
29:27	**USB 3.1 Gen2** **Receiver Low Frequency Periodic Signaling (LFPS) Filter N Select (filter_sel_n) - R/W** These bits can be adjusted, if needed to adjust the N side input LFPS sensitivity levels, which may be needed for Receiver Compliance RX Loopback test. 000b to 010b = Reserved 011b 100b = PCH Default 101b = Maximum Level • 110b and 111b = Reserved **Notes:** 1. filter_sel_n[29:27] and filter_sel_p[26:24] must both be set to the same exact Bit values. 2. If manually changed the USB 3.1 Gen2 Link must be retrained for it to take effect. This can be done by unplugging the USB 3.1 Gen2 device and then plugging it back in.
	USB 3.1 Gen2 **Receiver Low Frequency Periodic Signaling (LFPS) Filter P Select (filter_sel_p) - R/W** These bits can be adjusted, if needed to adjust the P side input LFPS sensitivity levels, which may be needed for Receiver Compliance RX Loopback test. 000b to 010b = Reserved 011b 100b = PCH Default 101b = Maximum Level • 110b and 111b = Reserved **Notes**: 1. filter_sel_p[26:24] and filter_sel_n[29:27] must both be set to the same exact Bit values. 2. If manually changed the USB 3.1 Gen2 Link must be retrained for it to take effect. This can be done by unplugging the USB 3.1 Gen2 device and then plugging it back in.
23:3	**Reserved**
2:0	**USB 3.1 Gen2** **Receiver Low Frequency Periodic Signaling (LFPS) Filter Bias Resistor Configuration (olfpscfgpullupdwnres_sus_usb) - R/W** These bits can be adjusted, if needed, to adjust the input LFPS Bias Resistor sensitivity levels, which may be needed for Receiver Compliance RX Loopback test. 000b to 011b = Reserved 100b 101b = PCH Default 110b and 111b = Reserved **Note**: If manually changed the USB 3.1 Gen2 Link must be retrained for it to take effect. This can be done by unplugging the USB 3.1 Gen2 device and then plugging it back in.

31.2.4 HSIO_TX_DWORD5 - High Speed I/O Transmit Control Register 5

Address: Refer to Table 33

BIOS Reference Code Platform Configuration PCH Policy Details:

- PCIe* Gen1 Parameters
  - — PchPcieHsioTxGen1DeEmphEnable = 1 (Enable)
  - — PchPcieHsioTxGen1DeEmph = Bits[13:8]
- PCIe* Gen2 Parameters
  - — PchPcieHsioTxGen2DeEmph3p5Enable = 1 (Enable)

— PchPcieHsioTxGen2DeEmph3p5 = Bits[21:16]

- USB 3.1 Gen1 Parameters
  - — HsioTxDeEmphEnable = 1 (Enable)
  - — HsioTxDeEmph = Bits[21:16]

Bit	Description
31:22	**Reserved**
21:16	**PCIe* Gen2 and USB 3.1 Gen1** **TX Output -3.5dB Mode De-Emphasis Adjustment Setting (ow2tapgen2deemph3p5) - R/W** These bits can be used to adjust or fine-tune the amount by which the output is de- emphasized. De-Emphasis = 20*Log([21:16]Decimal / 64) dB Where 111111b --> Min Level, 000001b --> Max Level, 000000 --> Reserved **Note**: Larger value generates a smaller De-Emphasis level.
15:14	**Reserved**
13:8	**PCIe* Gen1** **TX Output -3.5 dB Mode De-Emphasis Adjustment Setting (ow2tapgen1deemph3p5) - R/W** These bits can be used to adjust or fine-tune the amount by which the output is de- emphasized. De-Emphasis = 20*Log([13:8]Decimal / 64) dB Where 111111b --> Min Level, 000001b --> Max Level, 000000 --> Reserved **Note**: Larger value generates a smaller De-Emphasis level.
7:0	**Reserved**

31.2.5 HSIO_TX_DWORD6 - High Speed I/O Transmit Control Register 6

Address: Refer to Table 33

BIOS Reference Code Platform Configuration PCH Policy Details:

PCIe* Gen2 Parameters

PchPcieHsioTxGen2DeEmph6p0Enable = 1 (Enable)

PchPcieHsioTxGen2DeEmph6p0 = Bits[13:8]

SATA 1.5 GT/s Parameters

PchSataHsioTxGen1DeEmphEnable = 1 (Enable)

PchSataHsioTxGen1DeEmph = Bits[5:0]

SATA 3.0 GT/s Parameters

PchSataHsioTxGen2DeEmphEnable = 1 (Enable)

PchSataHsioTxGen2DeEmph = Bits[13:8]

SATA 6.0 GT/s Parameters

PchSataHsioTxGen3DeEmphEnable = 1 (Enable)

PchSataHsioTxGen3DeEmph = Bits[21:16]

Bit	Description
31:22	**Reserved**
21:16	**SATA 6.0 GT/s** **TX Output -6.0dB Mode De-Emphasis Adjustment Setting (ow2tapgen3deemph6p0) - R/W** These bits can be used to adjust or fine-tune the amount by which the output is de- emphasized De-Emphasis = 20*Log([21:16]Decimal / 64) dB Where 111111b --> Min Level, 000001b --> Max Level, 000000 --> Reserved **Note**: Larger value generates a smaller De-Emphasis level.
15:14	**Reserved**
13:8	**PCIe* Gen2 and SATA 3.0 GT/s** **TX Output -6.0 dB Mode De-Emphasis Adjustment Setting (ow2tapgen2deemph6p0) - R/W** These bits can be used to adjust or fine-tune the amount by which the output is de- emphasized De-Emphasis = 20*Log([13:8]Decimal / 64) dB Where 111111b --> Min Level, 000001b --> Max Level, 000000 --> Reserved **Note**: Larger value generates a smaller De-Emphasis level.
7:6	**Reserved**
5:0	**SATA 1.5 GT/s** **TX Output -6.0 dB Mode De-Emphasis Adjustment Setting (ow2tapgen1deemph6p0) - R/W** These bits can be used to adjust or fine-tune the amount by which the output is de- emphasized. De-Emphasis = 20*Log([5:0]Decimal / 64) dB Where 111111b --> Min Level, 000001b --> Max Level, 000000 --> Reserved **Note**: Larger value generates a smaller De-Emphasis level

31.2.6 HSIO_TX_DWORD8 - High Speed I/O Transmit Control Register 8

Address: Refer to Table 33

BIOS Reference Code Platform Configuration PCH Policy Details:

PCIe* Gen1 Parameters

PchPcieHsioTxGen1DownscaleAmpEnable = 1 (Enable)

PchPcieHsioTxGen1DownscaleAmp = Bits[13:8]

PCIe* Gen2 Parameters

PchPcieHsioTxGen2DownscaleAmpEnable = 1 (Enable)

PchPcieHsioTxGen2DownscaleAmp = Bits[21:16]

PCIe* Gen3 Parameters

PchPcieHsioTxGen3DownscaleAmpEnable = 1 (Enable)

PchPcieHsioTxGen3DownscaleAmp = Bits[29:24]

SATA 1.5 GT/s Parameters

PchSataHsioTxGen1DownscaleAmpEnable = 1 (Enable)

PchSataHsioTxGen1DownscaleAmp = Bits[13:8]

SATA 3.0 GT/s Parameters

PchSataHsioTxGen2DownscaleAmpEnable = 1 (Enable)

PchSataHsioTxGen2DownscaleAmp = Bits[21:16]

SATA 6.0 GT/s Parameters

PchSataHsioTxGen3DownscaleAmpEnable = 1 (Enable)

PchSataHsioTxGen3DownscaleAmp = Bits[29:24]

USB 3.1 Gen1 Parameters

HsioTxDownscaleAmpEnable = 1 (Enable)

HsioTxDownscaleAmp = Bits[21:16]

Bit	Description
31:30	**Reserved**
29:24	**PCIe* Gen3 and SATA 6.0 GT/s** **TX Output Downscale Amplitude Adjustment (orate10margin) - R/W**p These bits can be used to adjust the transmitter driver strength and its output swing Amplitude = Full Swing Voltage Level * (Bits[29:24]decimal / 64) - Where 000000b/111111b --> Max Level, 000001b --> Min Level
23:22	**Reserved**
21:16	**PCIe* Gen2, SATA 3.0 GT/s, and USB 3.1 Gen1** **TX Output Downscale Amplitude Adjustment (orate01margin) - R/W** These bits can be used to adjust the transmitter driver strength and its output swing Amplitude = Full Swing Voltage Level * (Bits[21:16]decimal / 64) - Where 000000b/111111b --> Max Level, 000001b --> Min Level
15:14	**Reserved**
13:8	**PCIe* Gen1 and SATA 1.5 GT/s** **TX Output Downscale Amplitude Adjustment (orate00margin) - R/W** These bits can be used to adjust the transmitter driver strength and its output swing Amplitude = Full Swing Voltage Level * (Bits[13:8]decimal / 64) - Where 000000b/111111b --> Max Level, 000001b --> Min Level
7:0	**Reserved**

31.2.7 HSIO_TX_DWORD9 - High Speed I/O Transmit Control Register 9

Address: Refer to Table 33

BIOS Reference Code Platform Configuration PCH Policy Details:

USB 3.1 Gen2 Parameters

HsioTxRate2UniqTranEnable = 1 (Enable)

Rate2UniqTranScale = Bits[14:8]

Bit	Description
31:15	**Reserved**
14:8	**USB 3.1 Gen2** **TX Output Downscale Amplitude Adjustment (rate2UniqTranScale) - R/W** These bits can be used to adjust the transmitter driver strength and its output swing Amplitude = Full Swing Voltage Level * (Bits[14:8]decimal / 64) - Where 0000000b/1111111b --> Max Level, 0000001b --> Min Level
7:0	**Reserved**

31.2.8 HSIO_TX_DWORD19 - High Speed I/O Transmit Control Register 19

Address: Refer to Table 33

Bit Range	Description
31:2	**Reserved**
1	**TX ModPHY Register Initiate Calculation (o_calcinit) - R/W** 0 = Disable 1 = Initiate **Note**: Refer to Section 4.3.1 for additional details. This bit is only needed, when dynamically (manually) writing and adjusting any of the TX ModPHY Registers.
0	**Reserved**